# GROWTH AND CHARACTERIZATION OF TWO-DIMENSIONAL III-V SEMICONDUCTOR PLATFORMS FOR MESOSCOPIC PHYSICS AND QUANTUM DEVICES

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# ABSTRACT

Saeed Fallahi Ph.D., Purdue University, August 2019. Growth and Characterization of Two-Dimensional III-V Semiconductor Platforms for Mesoscopic Physics and Quantum Devices. Major Professor: Michael J. Manfra.

Achievements in the growth of ultra-pure III-V semiconductor materials using state of the art molecular beam epitaxy (MBE) machine has led to the discovery of new physics and technological innovations. High mobility two-dimensional electron gas (2DEG) embedded in GaAs/$Al_xGa_{1-x}$As heterostructures provides an unparalleled platform for many-body physics including fractional quantum Hall effect. On the other hand, single electron devices fabricated on modulation doped GaAs/$Al_xGa_{1-x}$As heterostructures have been extensively used for fabrication of quantum devices such as spin qubit with application in quantum computing. Furthermore, epitaxial hybrid superconductor-semiconductor heterostructures with ultra clean superconductor-semiconductor interface have been grown using MBE technique to explore rare physical quantum state of the matter namely Majorana zero modes with non-abelian exchange statistics.

Chapter 1 in the manuscript starts with description of GaAs MBE system at Purdue University and continues with the modifications have been made to MBE hardware and growth conditions for growing heterostrcutures with 2DEG mobility exceeding $35 \times 10^6 cm^{-2}/Vs$. Utilizing an ultra-high pure Ga source material and its further purification by thermal evaporation in the vacuum are determined to have major impact on growth of high mobility GaAs/$Al_xGa_{1-x}$As heterostructures.

Chapter 2 reports a systematic study on the effect of silicon doping density on low frequency charge noise and conductance drift in laterally gated nanostructures fabricated on modulation doped GaAs/$Al_xGa_{1-x}$As heterostructures grown by Molecular

Beam Epitaxy (MBE). The primary result of this study is that both charge noise and conductance drift are strongly impacted by the silicon doping used to create the two-dimensional electron gas. These findings shed light on the physical origin of the defect states responsible for charge noise and conductance drift. This is especially significant for spin qubit devices, which require minimization of conductance drift and charge noise for stable operation and good coherence.

Chapter 3 demonstrates measurements of the induced superconducting gap in 2D hybrid Al/$Al_{0.15}In_{0.85}As$/InAs heterostructures which is a promising platform for scaling topological qubits based on Majorana zero modes. The 2DEG lies in an InAs quantum well and is separated from the epitaxial Al layer by a barrier of $Al_{0.15}In_{0.85}As$ with thickness d. Due to hybridization between the wave functions of 2DEG and superconductor, the strength of induced gap in the 2DEG largely depends on the barrier thickness. This chapter presents a systematic study of the strength of the induced gap in hybrid Al/$Al_{0.15}In_{0.85}As$/InAs superconductor/semiconductor heterostructures as a function of barrier thickness.

# 1. MOLECULAR BEAM EPITAXY OF ULTRA PURE GAAS AND $AL_XGA_{1-X}AS$ [1]

## 1.1 Introduction

Molecular beam epitaxy (MBE) is a state of the art material growth technique to grow advanced heterostructures with composition and doping profiles controlled on a nanometer scale. The growth of materials takes place under ultra-high vacuum (UHV) conditions on a heated crystalline substrate by the interaction of adsorbed species supplied by atomic or molecular beams. The main focus of this chapter is devoted to MBE growth of high-purity GaAs/$Al_xGa_{1-x}As$ heterostructures embedding two-dimensional electron gas (2DEG). The lattice-matched crystalline material in GaAs-$Al_xGa_{1-x}As$ system (lattice mismatch between GaAs and the AlAs is $\sim$ 0.1%) enables growing heterostructures with negligible mechanical stresses and with very few interface states.

High purity semiconductor materials are necessary for the fabrication of various state of the art quantum devices, such as spin-qubits and investigation of many body effects, such as those leading to fractional quantum Hall effect. The development of high purity GaAs and $Al_xGa_{1-x}As$ is closely related to the identification of residual impurities in these materials and the utilization of various tools and techniques to purify the source materials. The most commonly employed characterization of material quality is the electron mobility i.e. how fast the electrons move when an electric field is applied, in 2DEG embedded in the GaAs/$Al_xGa_{1-x}As$ heterojunction. Crudely speaking, mobility measures an electrons ability to carry current without undergoing

[1] THIS CHAPTER IS ADAPTED FROM J. CRYST. GROWTH, VOL. 441, G. C. GARDNER, S. FALLAHI, J. D. WATSON, AND M. J. MANFRA, 'MODIFIED MBE HARDWARE AND TECHNIQUES AND ROLE OF GALLIUM PURITY FOR ATTAINMENT OF TWO DIMENSIONAL ELECTRON GAS MOBILITY $> 35 \times 10^6 CM^2/VS$ IN ALGAAS/GAAS QUANTUM WELLS GROWN BY MBE', 71-77, COPYRIGHT 2016, WITH PERMISSION FROM ELSEVIER.

large-angle scattering. Mobility is related to the momentum relaxation time $\tau$ via $\mu = e\tau/m^*$, where e and $m^*$ are the charge and the effective mass of electron respectively. In the systems with sufficiently small remote ionized scattering, the mobility is known to be limited by residual background charged impurities at temperatures below 1K where the phonon scattering vanishes [1–3]. Decades of technological innovation made it possible to reach low-temperature mobility $\sim 31 \times 10^6 cm^2/Vs$ at Bell Laboratories [4] via utilizing symmetric auxiliary doping wells above and below the primary quantum well embedding the 2DEG. These results have been confirmed later by Umansky and coworkers [5]. The upward mobility history of GaAs is shown in Fig 1.1 indicating the steps leading to the improvement of 2DEG quality.

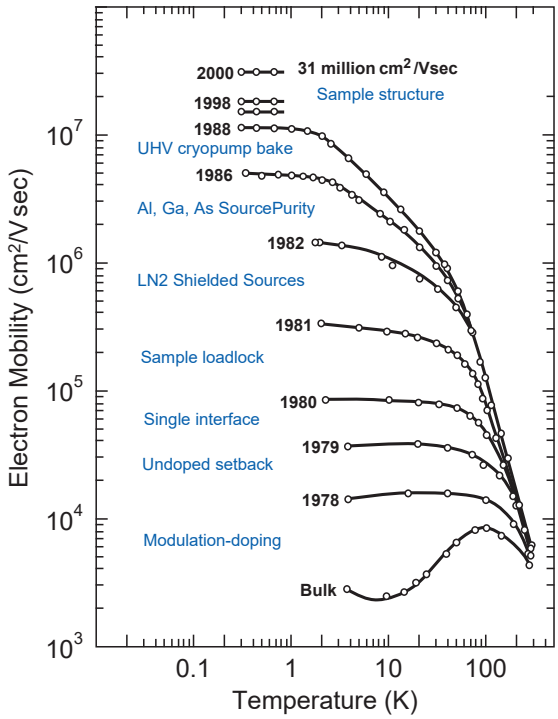


Fig. 1.1. A historical view of the upward electron mobility in GaAs heterostructures and the steps leading to this improvement. Reprinted from Physica E, vol. 20, L. Pfeiffer, and K. W. West, 'The role of MBE in recent quantum Hall effect physics discoveries', 5764, Copyright 2013, with permission from Elsevier.

Many useful textbooks have been published on the subject of MBE growth technique, historical review of MBE growth, UHV systems and MBE components and Materials. [6–12]. In this chapter, a compact description of GaAs MBE system at Purdue University is presented and modification to MBE hardware and growth conditions to attain 2DEG mobility exceeding $\sim 35 \times 10^6 cm^2/Vs$ is explained. More detailed information on MBE growth technique can be found in well written thesis by my colleagues Dr. John Watson [13] and Dr. Geoff Gardner [14] .

## 1.2 High Mobility GaAs MBE System

GaAs MBE system at Purdue University is a modified Veeco Gen II MBE system specifically designed to produce ultra-high quality 2DEG. As it is shown in Fig. 1.2, it consists of a growth chamber, a buffer chamber and an introduction chamber (load-lock), with the vacuum level improving progressively towards the growth chamber.

The quick-entry load-lock chamber is used to transfer wafers into and out of the growth chamber without breaking the UHV conditions, which would otherwise require days or weeks to recondition the growth chamber. Load-lock chamber is equipped with a heating filament to outgass (desorb) most of the water vapor and other gases which are loosely bonded to the GaAs substrate and the Ta-block that the substrate is mounted on. A CT-8 cryopump pumps the load-lock space down to $\sim 5 \times 10^{-9}$ Torr and the wafer outgasses at 120 °C for 10h.

The substrates are then transferred to the buffer chamber for additional outgassing at 350 °C for 3.5h to further remove water vapor and other gasses as well as $As_2O_3$ which presents in native oxide. A CT-8 cryopump pumps the buffer chamber down to $\sim 2 \times 10^{-11}$ Torr. The buffer chamber is equipped with SRS residual gas analyzer (RGA) to perform gas analysis, leak detection and vacuum processing such as Ta block outgassing at elevated temperatures. RGA is an extremely useful tool to probe the cleanness of the outgassed wafer by acquiring live spectra of the species partial pressure coming off the wafer/Block during the outgass in a range from 1 to 200

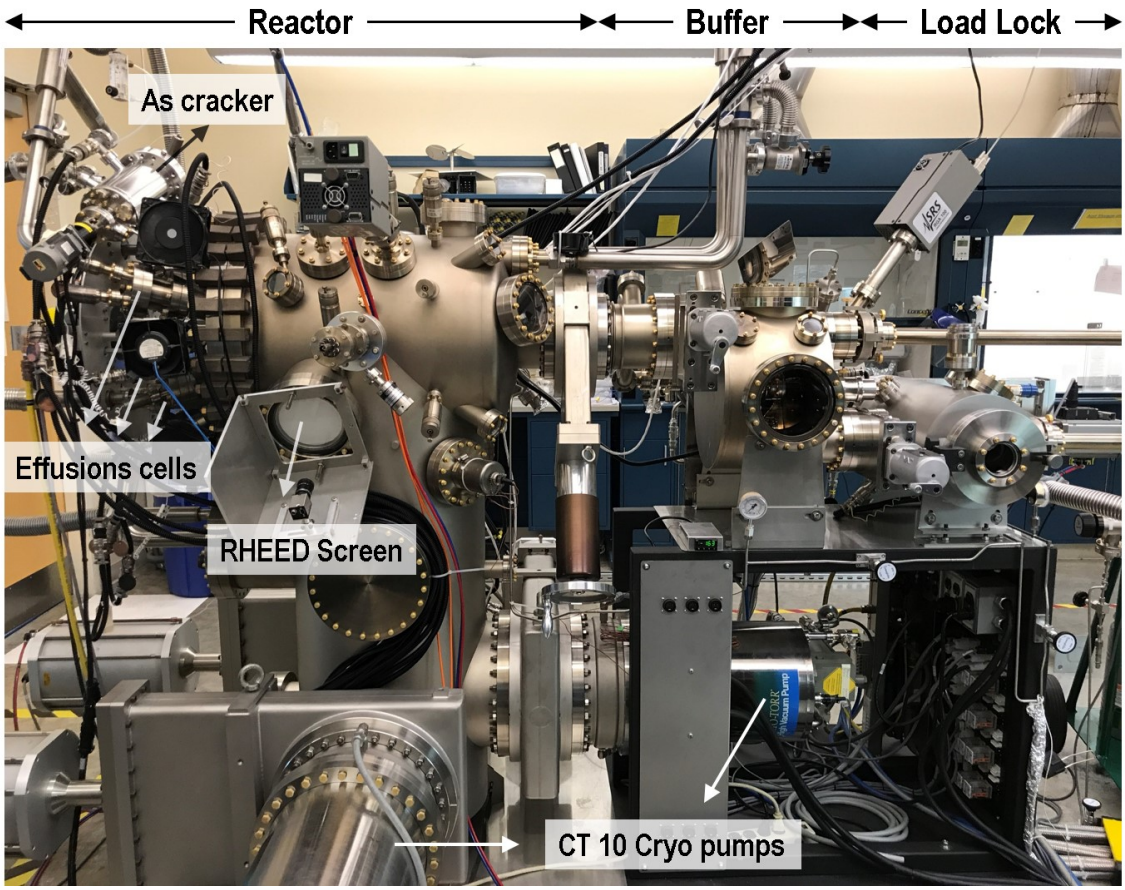


Fig. 1.2. Modified Veeco Gen II MBE system at Purdue University.

AMU. In the next section, an example of RGA spectra is shown during the standard wafer outgass in buffer chamber (i.e. 3.5h at 380 °C) before transferring to growth chamber.

The growth chamber is pumped through custom all-metal gate valves by 3 Brooks CT-10 cryopumps which each has a pumping speed of 3000 l/s for air. Growth chamber also contains an additional titanium sublimation pump which can effectively reduce the hydrogen partial pressure by an order of magnitude from $\sim 1 \times 10^{-11}$ Torr to $1 \times 10^{-12}$ Torr. The Growth chamber contains of hollow-walled internal liquid-nitrogen-filled cyropanel which is cooled to 77K to help in reducing the base pressure

and to serve as thermal isolation between cells from cross talk and is maintained in this condition for several years with proper planning and good fortune. The base pressure of growth chambers reaches $< 2 \times 10^{-11}$ Torr when the system in idle condition and no growth is happening. All effusion cells and large capacity arsenic cell are custom designed to reduce thermal load into the growth chamber during the crystal growth. Consumption power of the Ga source to grow GaAs with 1 monolayer/s growth rate is determined to be $\sim$ 120 W and the Al cell the power output to grow $Al_{0.24}Ga_{0.76}As$ is found to be $\sim$ 180 W. For both n-type and p-type doping we utilized home-built Si and C filament sources with power consumption of 70 W and 280 W respectively during the deposition. The MBE growth chamber is also equipped with large area shutter (main shutter) which is placed between the sources and the substrate manipulator to shield the substrate and manipulator from all source fluxes. The growth chamber also includes a 200 AMU SRS RGA and AMETEK Dycor RGA to monitor the residual gas partial pressure and cleanness of the UHV environment. Last but not least, the MBE growth chamber has equipped with growth rate characterization tool namely reflection high-energy electron diffraction (RHEED) to calibrate the growth rates for each heterostruture growth.

## 1.3 RGA spectra in MBE system

As mentioned in the previous section, the buffer and growth chambers in MBE system are equipped with RGA to probe and monitor the partial pressure of species and prevent growth chamber contamination by stopping transfer of blocks with a suspicious looking RGA spectra during the buffer outgass into the growth chamber.

Figure 1.3 shows a clean RGA spectra from growth chamber at MBE idle condition with reactor pressure $\sim 2 \times 10^{-11}$ Torr. Dominant species include Water, Nitrogen Carbon Dioxide, and Arsenic. The amount of C and AsO species which are dominant source of electron trap in the bulk of GaAs is minimal with their partial pressures below $1 \times 10^{-12}$ Torr and are close to the noise floor of RGA spectra. This prototype

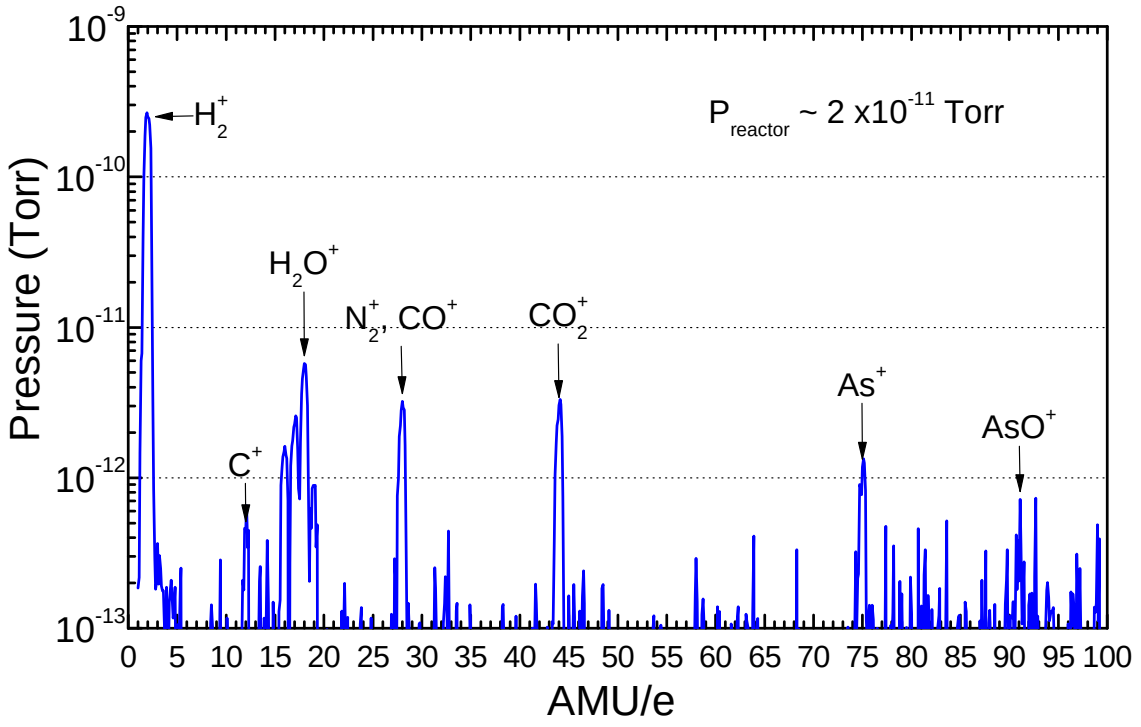


Fig. 1.3. Clean RGA spectra from Reactor at idle condition with $P_{reactor} \sim 2 \times 10^{-11}$ Torr. The dominant species are labeled which all have partial pressures below $1 \times 10^{-11}$ Torr

RGA spectra serves as a reference to compare with situations in which the quality of grown wafers degrades (as determined by low-temperature electron mobility) and it is used to troubleshoot the source of contamination.

The source of contamination is always external and is related to the cleanness of the substrates that are loaded into the MBE system and extra care should be taken during mounting new wafers on Ta block. The possible contamination are rooted in the tools that have been used for mounting new wafer. These tools include tweezers, Ga melt that is used to stick the substrate on Ta block, Ga container and the glove. Previously a Teflon applier were used to apply Ga on the Ta block to wet the surface and it is found to be a source of Fluorine (F) contamination with 19 AMU/e which is extremely hard to remove from the vacuum chamber. A custom applier from Ta

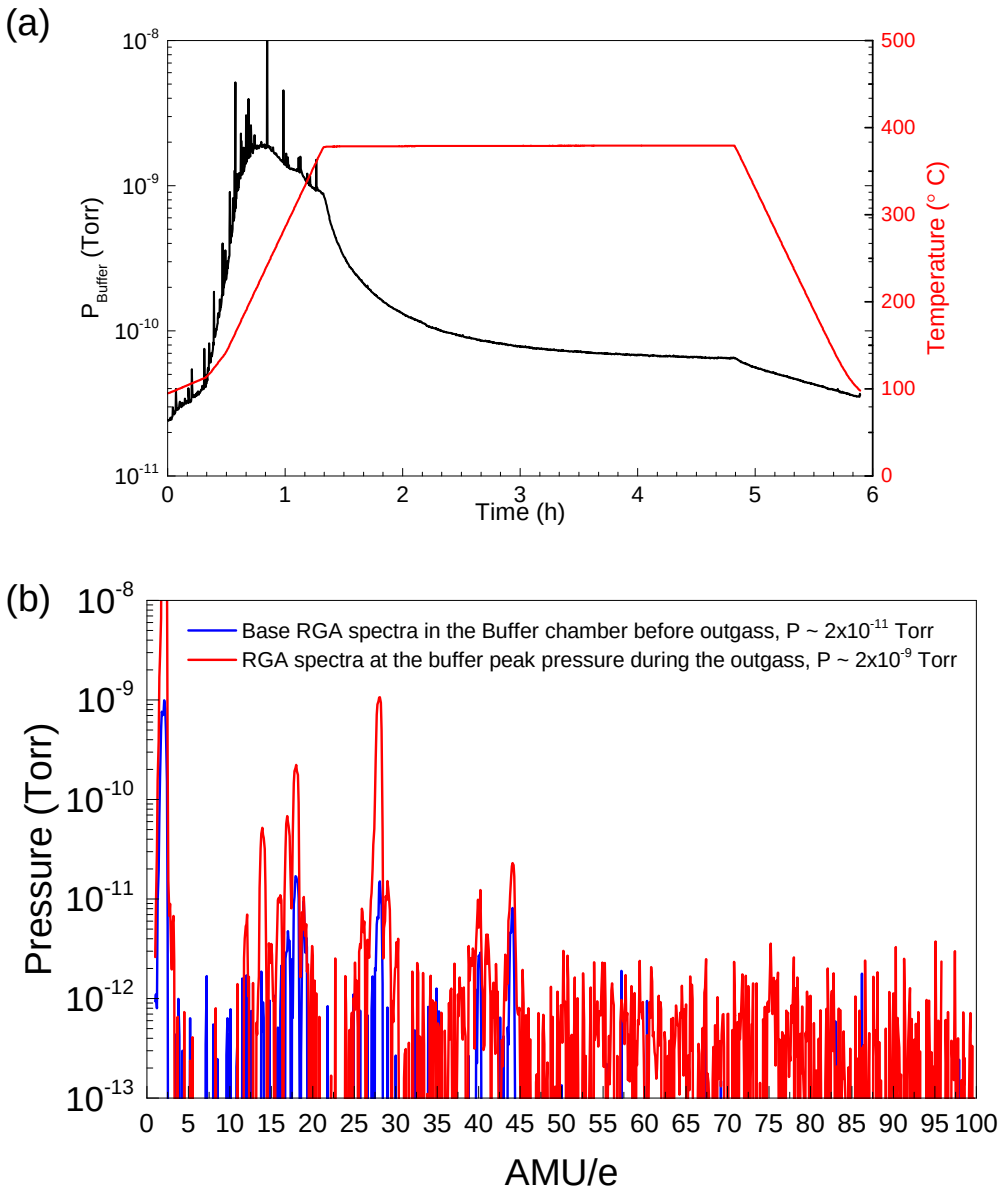


Fig. 1.4. New GaAs wafer outgass in the buffer chamber. (a) Buffer chamber pressure (black solid line) and thermal treatment profile (red solid line) during wafer outgass at 380 °C for $\sim$ 5h. (b) An overlay of base RGA spectra in the buffer chamber with RGA spectra at the buffer chamber peak pressure during during wafer outgass.

sheet is made to replace Teflon spatula for applying Ga melt on the blocks. During the substrate mount process, a clean lab coat should be worn and head net should be

put on to prevent falling any dust or hair on the substrate. After following all of these hygiene protocols, there is still a chance that the loaded wafer is contaminated from unknown source and one should always monitor the RGA spectra during the block outass in the buffer chamber to give it a green pass to enter the growth chamber.

A characteristic RGA spectra for a clean outgassed wafer in the buffer chamber is shown in Fig. 1.4. Figure 1.4(a) shows temperature profile and buffer chamber pressure trend during wafer outgass at 380 °C. Buffer chamber base pressure is $\sim 2 \times 10^{-11}$ Torr before starting the wafer outgass and it peaks at $\sim 2 \times 10^{-9}$ Torr before temperature reaches 380 °C and the pressure falls down during 3.5h sitting at 380 °C and reaches $\sim 4 \times 10^{-11}$ Torr at the end of the outgass. RGA spectra at the buffer peak pressure is shown in Fig. 1.4(b) (red solid line) indicating that the major species that come off the wafer are Nitrogen (mass 28) and water (mass 18). These species might also be trapped between the wafer and the block that has been mounted on with Ga glue and they get a chance to be release during the outgass as visible with pressure spikes in Fig. 1.4(a). This RGA spectra at peak pressure is characteristics of a clean wafer outgass in the buffer chamber and has green pass permit to enter the growth chamber.

## 1.4 High mobility heterostructure design and growth campaigns

The high mobility heterostructure consists of a 30 nm GaAs quantum well surrounded by AlAs/GaAsSi delta-doped/AlAs (3nm/2nm/3nm) doping wells which symmetrically located at 75nm above and below the main 30nm quantum well. This doping scheme was first proposed by Baba in 1983 [15] and modified by Friedland in 1996 [16] to reduce impurity scattering in remotely doped GaAs single quantum wells due to accumulation of heavy-mass X electrons within the AlAs layers. This doping scheme also prevents the formation of DX centers and enhances doping efficiency. DX centers are deep level traps associated with donors in IIIV semiconductors. Formation of DX centers in $Al_xGa_{1-x}As$ with x0.22 is responsible for the reduced conductivity

as well as the persistent photoconductivity observed in this material at low temperatures [17, 18]. Confining the electrons in a thin 3 nm GaAs well raises the quantized electron energy level in the well and allows charge transfer to the main 30 nm GaAs quantum well embedding 2DEG. Fig. 1 shows the layer stack of active region and simulated band profile for high mobility 2DEG heterostructure using the nextnano$^3$ software package [19].

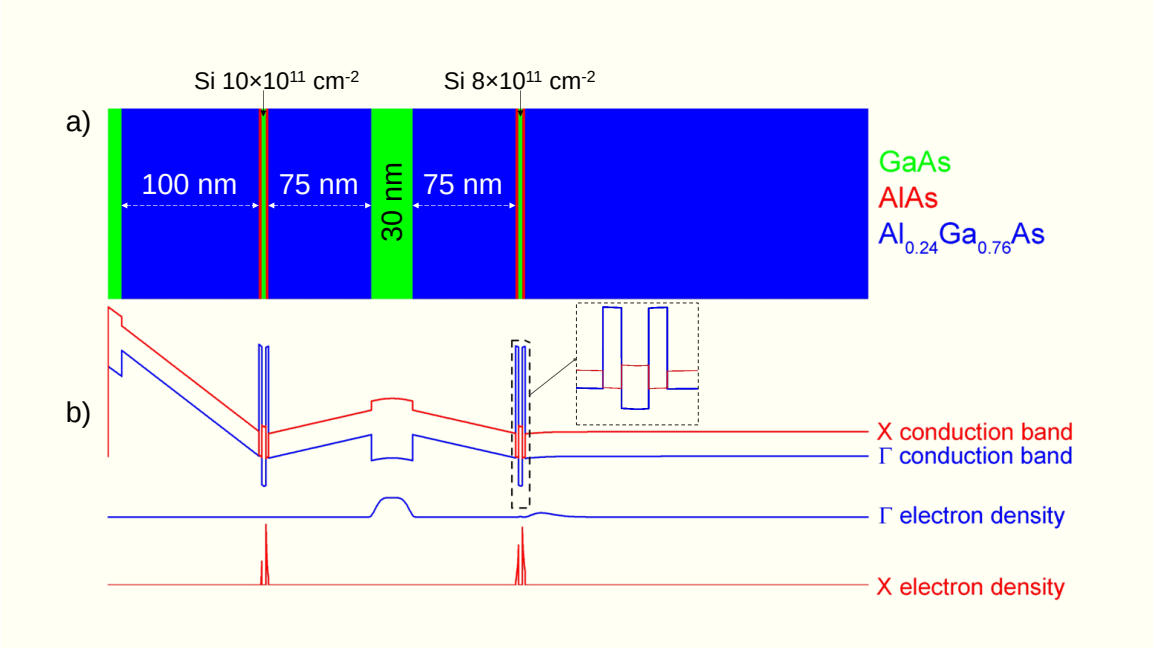


Fig. 1.5. (a) The active region layer stack used to grow a high mobility 2DEG with electron density $n = 3.0 \times 10^{11} cm^{-2}$.; and (b) Γ and X conduction band minimum along the growth direction. Electron density in the main GaAs quantum well (Γ band) and electron density in the screening AlAs layers (X band) are shown accordingly. Reprinted from J. Cryst. Growth, vol. 441, G. C. Gardner, S. Fallahi, J. D. Watson, and M. J. Manfra, 'Modified MBE hardware and techniques and role of gallium purity for attainment of two dimensional electron gas mobility $> 35 \times 10^6 cm^2/Vs$ in AlGaAs/GaAs quantum wells grown by MBE', 71-77, Copyright 2016, with permission from Elsevier.

The main GaAs quantum well is separated by 75nm $Al_{0.24}Ga_{0.76}As$ spacer layer from doping regions at the top and the bottom. The 24% Al mole fraction with 200 meV conduction band offset relative to GaAs QW is sufficient to confine electrons in the main quantum well before populating higher sub-bands at $n > 3.0 \times 10^{11} cm^{-2}$. At the same time, 24% Al content of AlGaAs layer reduces interface roughness and incorporation of unintentional impurities associated with higher mole fraction barriers. The Si doping density is $1 \times 10^{12} cm^{-2}$ in the top doping well and $0.8 \times 10^{12} cm^{-2}$ in the lower doping well which results in total charge transfer of $n = 3.0 \times 10^{11} cm^{-2}$ into the main 30nm GaAs quantum well. Approximately $6 \times 10^{11} cm^{-2}$ electron density transfer to the GaAs surface to compensate the surface states. A significant fraction (approximately 50%) of the electrons resides in the X-band of the AlAs layers flanking the narrow GaAs doping wells. These residual electrons screen the disorder potential created by the ionized dopants. The screening electrons do not form parallel conduction channel in low-temperature transport measurements due to their low mobility arising from their proximity to their parent silicon ions and their large effective mass in the X band of AlAs. All the layers except doping wells are grown at substrate temperature of 635 °C as measured by optical pyrometry. The substrate temperature is rapidly decreases to 450 °C for deposition of Si atoms to reduce the Si dopant migration [20], and a thin layer of GaAs is deposited following the silicon to reduce subsequent surface segregation. The growth proceeded at 1m/hr growth rate and the As flux ratio to Ga flux are set to 20 which corresponds to beam-equivalent pressure of $6.0 \times 10^{-6}$ Torr for arsenic. Reducing the As flux below $6.0 \times 10^{-6}$ Torr results in a hazy end-product in regions with low As beam exposure.

This active region is grown on top of the buffer layer separating it from the substrate. The buffer layer consists of two different superlattices (SL) namely 10nm GaAs SL and (10nm/3nm) $Al_{0.24}Ga_{0.76}As$/GaAs SL with 20 s pause between each SL layer. The role of GaAs SL layer is to smooth out the pristine GaAs substrate which becomes rougher during the initial oxide removal at substrate temperature $580 - 620°C$ under arsenic flux. The role of $Al_{0.24}Ga_{0.76}As$/GaAs SL is to block im-

purities from migrating to the active region due to the high chemical reactivity of the aluminum-containing layers and more smoothing of the surface.

It has been theoretically predicted that for AlGaAs spacer layer thicker than 70 nm, the mobility is limited by unintentional background impurities in the vicinity of the 2DEG [21, 22] and achieving electron mobility $> 30 \times 10^6 cm^2/Vs$ requires a uniform background impurity density below $2 \times 10^{13} cm^{-3}$. It has been shown that remote ionized impurity scattering is only responsible for 10% of the total scattering rate [1, 2]. This has been our motivation to purify the source materials either in-situ and/or ex-situ in order to grow high quality materials with minimal impurities.

In our first growth campaign starting from Jan 2011 to Dec 2013, we loaded commercially available Ga source with 7N purity (99.99999%) [23] and Al source with 6N5 purity (99.99995%) [24] and Arsenic source with 7N5 purity (99.999995%) [25] into MBE system. Impurity levels are measured by glow discharge mass spectrometry (GDMS). The early grown wafers showed very low quality transport results with electron mobility $\sim 1 \times 10^5 cm^2/Vs$ despite establishing very good UHV condition. This corresponds to p-type impurity concentration of $\sim 1 \times 10^{15} cm^{-3}$ as determined by electrical characterization of unintentionally doped bulk GaAs layers (5-10 $\mu$m). Hence the purest commercially available material is still dirty when it is considered to be loaded into the growth chamber and the source materials need to be additionally purified before using it for high mobility crystal growth.

A commonly used approach for cleaning up the source materials is via extended outgassing at high temperatures. Since most impurities like carbon and oxygen have higher vapour pressure than the source materials (Ga, Al and Si sources), the extended outgassing will clean up the materials by evaporating the impurities at higher temperatures. The As source is not subjected to outgassing treatment because it has high vapor pressure at temperature above 275 °C.

After loading the source materials into the growth chamber, the gallium sources were initially outgassed at 100 °C above their normal growth temperature for 7 h and finally outgassed at 200 C above growth temperature for 5 h. Outgassing at +200 C

corresponds to a GaAs growth rate of 20 $\mu$m/h. During the entire outgassing process, the substrate manipulator is kept in the transfer position such that the wafer puck points away from the sources and the beam flux gauge faces towards the sources. The main shutter that has been introduced previously is placed immediately in front of the ion gauge to protect it and other critical components on the manipulator from the elevated flux. During the outgass, the shutter in front of the Ga source effusion cells is opened. A small arsenic flux $\sim 2 \times 10^{-6}$ Torr is maintained during the cell outgassing to minimize deposition of liquid metal on critical components such as BF ion gauges electrical connections. The whole outgassing process is visually inspected to check the cleanness of crucible lips and the amount of droplet formation inside the crucible interior.

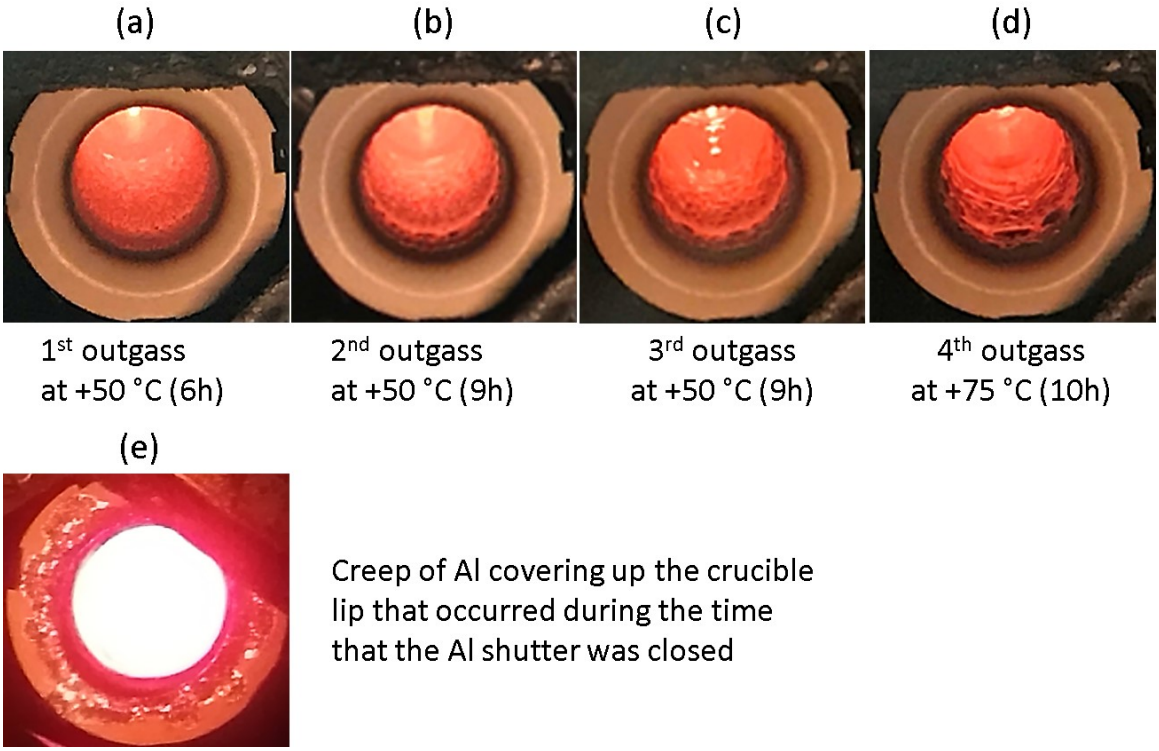


Fig. 1.6. a), b), c) and d) Creep of Al melt during the the successive outgassing of Al cell. e) Al has crept all the way up covering the crucible lip.

Special care should be taken during outgassing of Al source as it tends to climb up the crucible side walls and leads to possible flowing Al out of the crucible. Keeping the crucible lip colder than the melt increases the viscosity and slows down the Al creep. This is the reason the source shutter should be open during the entire outgassing. Figure 1.6 shows the gradual creeping of Al during the outgassing of Al source. It clearly shows that successive outgassing of Al cell results in building up Al puddles near the crucible lip. Figure 1.6e shows a catastrophic event when the Al shutter was closed during normal growth of GaAs/AlGaAs heterostrcutures but at growth rate. Ga cells do not suffer from metal creep up but it forms massive amount of Ga droplets that become bigger and bigger for an extended outgassing period. larger Ga droplets that form at the crucible orifice roll back into the hot melt and spit small particles of Ga on the wafer.

Figure 1.7 shows the improvement of 2DEG mobility for single interface heterojunction (SHJ) and doping well structures as a function of growth number in the first growth campaign. The first couple of single interface heterojunctions (SHJ) grown before Ga source outgassing showed insulating behaviour indicating a large amount of p-type impurities presents in the sample who eat up the charge carriers. However, after outgassing of Ga1 at +200 °C for 5h, the SHJ samples showed an electron mobility of $\sim 1 \times 10^6 cm^2/Vs$ and improved upon growing more wafers. Outgassing Al cell had minimal impact on the mobility improvement since the 2DEG electronic wave function exists primarily in the GaAs quantum well and not in the AlGaAs barrier. The rapid raise of mobility after outgassing Ga cell is believed to be due to the evaporation of high vapour pressure impurities in the Ga source. Further improvement in the mobility upon each growth is due to the self-clean up mechanism which happens at normal growth temperatures of Ga and Al source. After approximately 75 2DEG growths, the mobility reached $\sim 20 \times 10^6 cm^2/Vs$, where it saturated for the remainder of the first growth campaign. Low-temperature magneto-transport measurement of this high mobility 2DEG revealed development of fractional quantum states as is shown in Fig. 1.8.

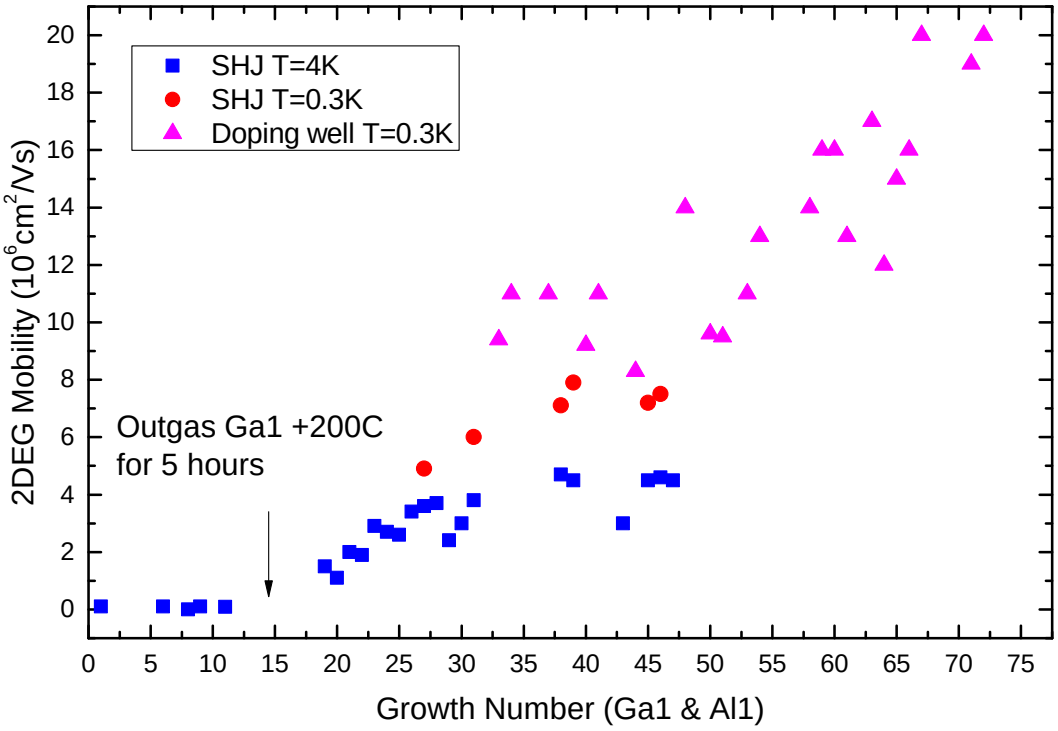


Fig. 1.7. Evolution of 2DEG mobility for single interface heterojunction (SHJ) and doping well structures as a function of growth number in the first campaign. Ga1 and Al1 refers to the particular cells used in the MBE for growing these heterostructures. Reprinted from J. Cryst. Growth, vol. 441, G. C. Gardner, S. Fallahi, J. D. Watson, and M. J. Manfra, 'Modified MBE hardware and techniques and role of gallium purity for attainment of two dimensional electron gas mobility $> 35 \times 10^6 cm^2/Vs$ in AlGaAs/GaAs quantum wells grown by MBE', 71-77, Copyright 2016, with permission from Elsevier.

The first growth campaign ended after As source is totally depleted. Total number of growths in the first campaign reached 420 growths with different heterostructures designs for several research projects including spin qubit and fractional quantum Hall effect [26–32].

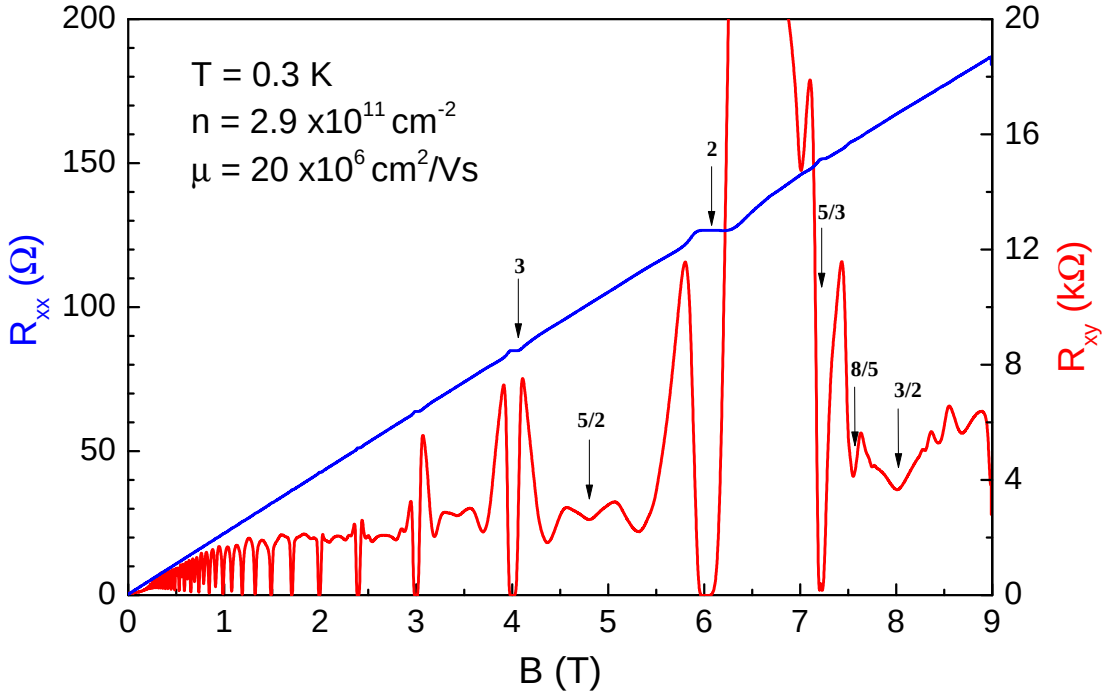


Fig. 1.8. Magnetotransport measurement results at 0.3K from a sample with mobility of $20 \times 10^6 cm^2/Vs$ and 2DEG density of $2.9 \times 10^{11} cm^{-2}$.

In the $2^{nd}$ growth campaign started from Aug 2013 until now, several modifications were made to MBE hardware as well as source materials to reduce the background impurities in gown wafers predominantly emanating from the source materials. We designed a substrate heater with a relatively dense resistive heater elements to reduce the thermal load in the growth chamber.

Apart from the effusion cells thermal load, the substrate heater also produces a substantial thermal load $\sim$ 150 W which varies for different Ta substrate holders and depends on the history of the holder. There is an experimental report by Umansky who has conducted a research on the effect of thermal load on the mobility of grown wafers and interestingly obtained an increase in mobility $\sim$ 40% after reducing the

heating power by $\sim 30\%$ [1]. This finding suggested to redesign our MBE substrate heater in order to reduce the overall thermal load in the growth chamber. In our new design of substrate heater which is shown in Fig. 1.9 , we increased the number of resistive heater elements from 4 to 6. Additionally, we doubled the number of heat shielding layers between the filament and the reminder of the substrate manipulator. Also, the opening to the filaments feet in the heat shield is reduced from 0.19" to 0.12" in diameter to prevent leakage of thermal radiation. As a result of these modifications, the required power to reach normal growth temperature of 635 °C decreased from 150 W to 120 W.

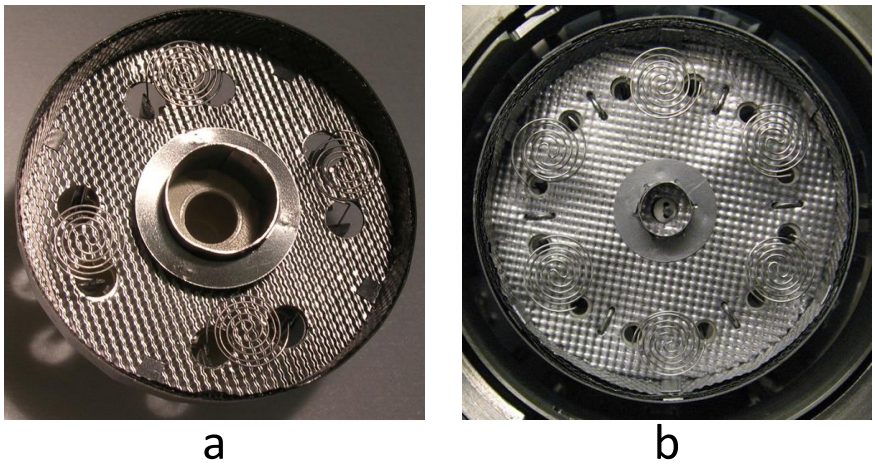


Fig. 1.9. (a) Four filaments substrate heater in the $1^{st}$ growth campaign. (b) Six filaments substrate heater in the $2^{nd}$ growth campaign. Reprinted from J. Cryst. Growth, vol. 441, G. C. Gardner, S. Fallahi, J. D. Watson, and M. J. Manfra, 'Modified MBE hardware and techniques and role of gallium purity for attainment of two dimensional electron gas mobility $> 35 \times 10^6 cm^2/Vs$ in AlGaAs/GaAs quantum wells grown by MBE', 71-77, Copyright 2016, with permission from Elsevier.

We built an ancillary chamber to outgass and clean the effusion cells and the crucibles to be loaded into the growth chamber. This ultra-clean UHV chamber is pumped by a CT-8 cryopump and can reach pressures below X-ray limit of a standard ion gauge (i.e. $2 \times 10^{-11}$Torr). This chamber is equipped with 200 AMU RGA and it

contains 4 source ports and it is designed to allow evaporated gallium to be captured in a vessel at the bottom of the chamber.

We constructed a custom glovebox to minimize introducing detrimental gas such as oxygen and water vapor pressure into the growth chamber. Commonly used technique for loading new source materials required using glovebag which is sometimes cumbersome and it suffers from poor visibility. This custom built glovebox that is shown in Fig. 1.10, provides significant advantages for major MBE maintenance operations including excellent visibility, robustness and the necessary manual dexterity for handling source materials and loading the crucible inside the effusion cell. This glovebox consists of a big opening in the back that seals on the source ports assembly and it is equipped with multiple ports for handling and assembling source flanges on growth chamber ports. We use a balloon made of polyethylene plastic to actively purge the entire volume of glovebox via inflating the ballon using pure Argon gas. The purity of Argon gas used for purging the glovebox is 99.9999% (6N) and it has been further purified after passing through a heated titanium gettering furncae, model 2G-100-SS by Centorr [33]. After couple of outgassing attempts  10, the amount of oxygen level inside the glovebox reaches below 30 pmm as measured by the trace oxygen analyzer [34].

By improving our MBE maintenance techniques and utilizing custom-made tools, we dramatically reduced the introduction of water vapor and oxygen gas into the growth chamber during charging the source materials and removed the necessity to bake the system at 200 °C after maintenance. This is particularly beneficial in an arsenic-filled MBE which readily absorbs water vapor and oxygen onto large surface areas covered with arsenic. By eliminating the baking process we keep the sources and the manipulator clean because the bake process can potentially redistributes the contaminants over the entire deposition chamber including the sources and substrate manipulator.

We quantified the the efficiency of the improved maintenance technique by comparing the RGA spectra before and after venting the growth chamber. After warming

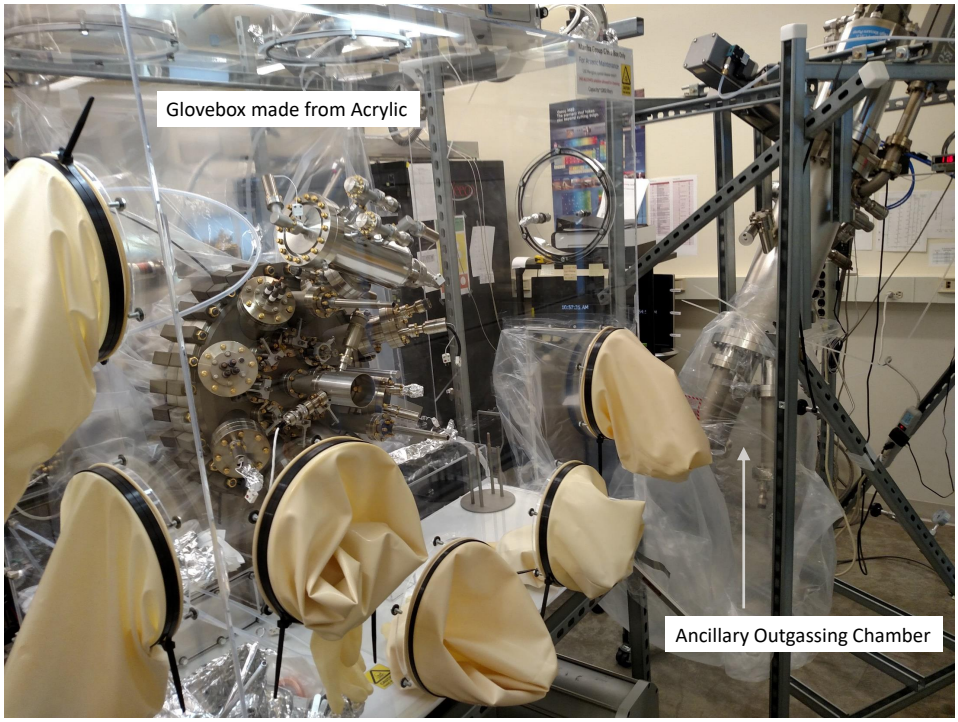


Fig. 1.10. The glove box enclosure which seals to the source flange of the MBE chamber and connects via a tunnel bag to UHV outgassing chamber. Reprinted from J. Cryst. Growth, vol. 441, G. C. Gardner, S. Fallahi, J. D. Watson, and M. J. Manfra, 'Modified MBE hardware and techniques and role of gallium purity for attainment of two dimensional electron gas mobility $> 35 \times 10^6 cm^2/Vs$ in AlGaAs/GaAs quantum wells grown by MBE', 71-77, Copyright 2016, with permission from Elsevier.

the MBE cryo shroud to room temperature and before venting the growth chamber, the pressure in the growth chamber was $\sim 1 \times 10^{-10}$ Torr. After venting and loading new sources, the growth chamber is pumped back down and the pressure in the growth chamber returned to below $2 \times 10^{-10}$ Torr within 24 h. The RGA spectra in Fig. 1.11 shows minimal change in the constituent partial pressures indicating the cleanness of the utilized MBE maintenance technique. The only species that have noticeable increase in partial pressure are water (18 AMU/e) and Argon (40 AMU/e). Note that Argon has been used as the vent gas. Water and Argon partial pressure

recovers after back-filling the cryo shroud with liquid nitrogen and after couple days pumping of the growth chamber.

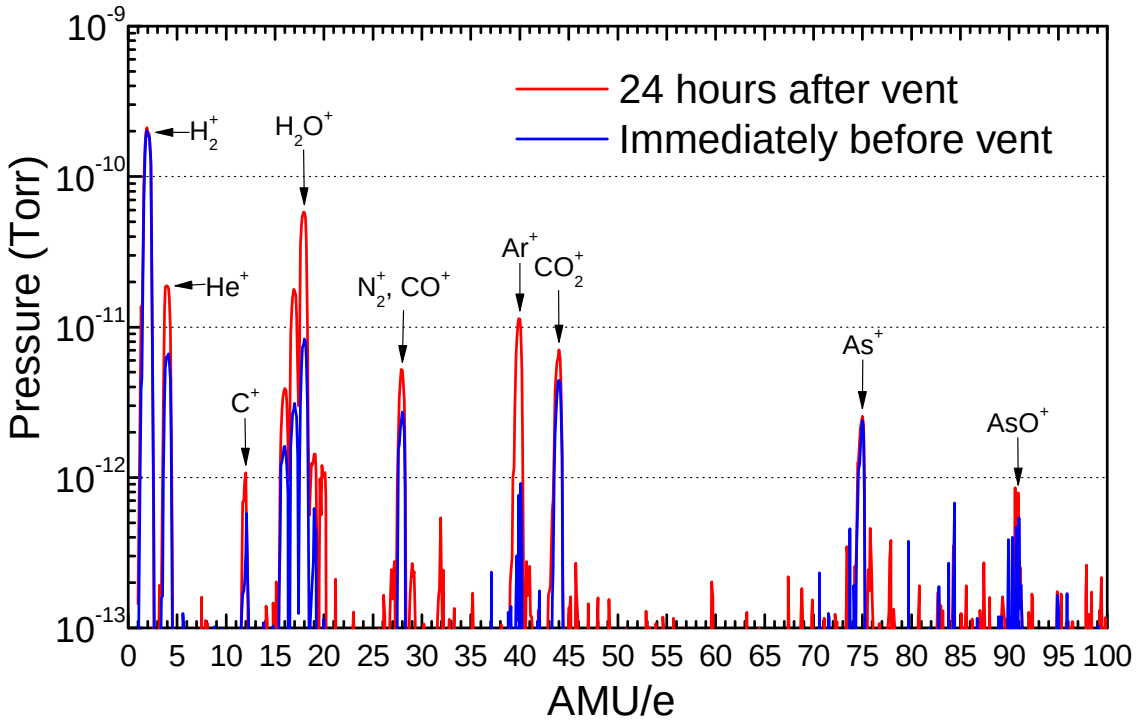


Fig. 1.11. Comparison of RGA spectra before vent and 24h after venting the growth chamber.

We studied the effect of Ga source material purity on the quality of our high mobility structure by loading two distinct gallium ingots with different nominal purity. One gallium effusion cell labeled as Ga1 is loaded with 7N gallium ingots supplied by Alcan [23] and it was the same lot that has been used in the first growth campaign. The second gallium effusion cell labeled as Ga2 is loaded with 8N gallium ingots supplied by Molycorp Rare Metals Inc. [35]. These ingots were packaged with tantalum sleeves of our own design between the ingot and the plastic packaging to reduce the risk of the plastic contaminating the gallium. Two aluminum effusion cells labeled as

Al1 and Al2 are loaded with ULVAC [24] material from the same lot used in the first growth campaign.

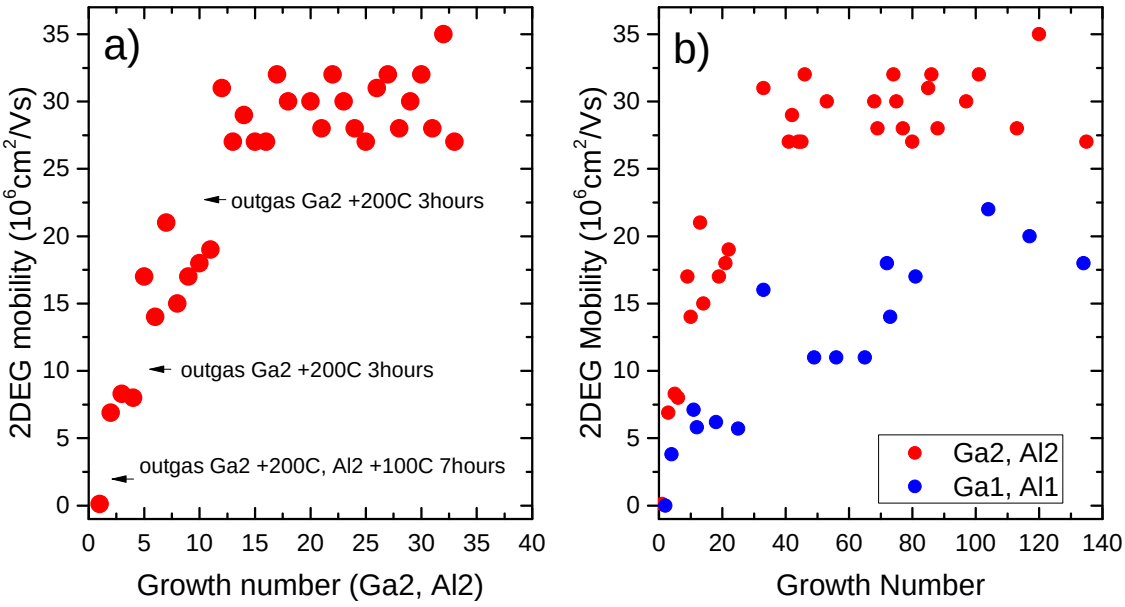


Fig. 1.12. (a) Discrete jumps in mobility are demonstrated using our high temperature outgassing procedure. (b) Plot of 2DEG mobility as a function of growth number demonstrates the difference in improvements between the two different gallium source materials despite receiving the same treatment. Reprinted from J. Cryst. Growth, vol. 441, G. C. Gardner, S. Fallahi, J. D. Watson, and M. J. Manfra, 'Modified MBE hardware and techniques and role of gallium purity for attainment of two dimensional electron gas mobility $> 35 \times 10^6 cm^2/Vs$ in AlGaAs/GaAs quantum wells grown by MBE', 71-77, Copyright 2016, with permission from Elsevier.

Figure 1.12 shows the evolution of electron mobility for high mobility heterostructure as a function of growth number and its variation after each high temperature outgassing exercise. Discrete jumps in mobility are seen in Fig. 1.12a with each outgassing of the Ga2 cell (Molycorp source material with 8N purity). It is obvious that each mobility jump is related to each outgassing experiment. High mobility het-

erostructures grown with Ga2 source reaches above $20 \times 10^6 cm^2/Vs$ after 10 growths and 2 high temperature outgassings (+200 °3hours) experiments. After the 3rd outgassing experiment, the mobility increased above $30 \times 10^6 cm^2/Vs$ for high mobility structures grown with Ga2. Similar discrete jumps were also observed for the Ga1 cell (Alcan source material with 7N purity), albeit with lower absolute value of mobility when compared to Ga2. Despite receiving the same number and intensity of high temperature outgassing, Ga2 was consistently able to produce samples of higher mobility than Ga1. The highest mobility achieved with Ga1 saturated at approximately $20 \times 10^6 cm^2/Vs$. We note that the aluminum cell outgassing (Al1 or Al2) did not influence this conclusion. The differences between Ga1 and Ga2 are most clearly seen in Fig. 1.12b, where the evolution of mobility for each Ga cell is shown over the course of the campaign. It seems that more outgassing of Ga cells can potentially lead to growth of even higher mobility but it comes at a cost of damaging moving parts on substrate manipulator due to material buildup. We continued the rest of campaign by growing heterostructures utilized to study fractional quantum Hall effect [36–40], spin-qubit [41–50], high electron mobility transistors [51] and other mesoscopic physics research [52–55].

Magnetotransport results for high mobility GaAs quantum well grown at the peak mobility of $2^{nd}$ growth campaign reveals well developed fractional quantum Hall states for both low and high electron density wafer. To obtain a low 2DEG density wafer $1.1 \times 10^{11} cm^{-2}$, the setback of doping layer in the high mobility heterostrcutre has been increased from 75 nm to 225 nm in order to reduce the charge transfer to the main quantum. Figure 1.13 shows the measurement results at 0.3K for high 2DEG density and low 2DEG density samples grown in $2^{nd}$ growth campaign. Electron mobility exceeding $35 \times 10^6 cm^2/Vs$ is achieved at $n = 3.0 \times 10^{11} cm^{-2}$ with well-developed fractional quantum Hall states. Based on the calculation in Ref. [22] our data suggests that the density of background charged impurity has been reduced to $\sim 1 \times 10^{13} cm^{-3}$. Particularly noteworthy is the development of the fractional quantum Hall series converging to $\nu = 1/2$ in the low density sample. The appearance of many

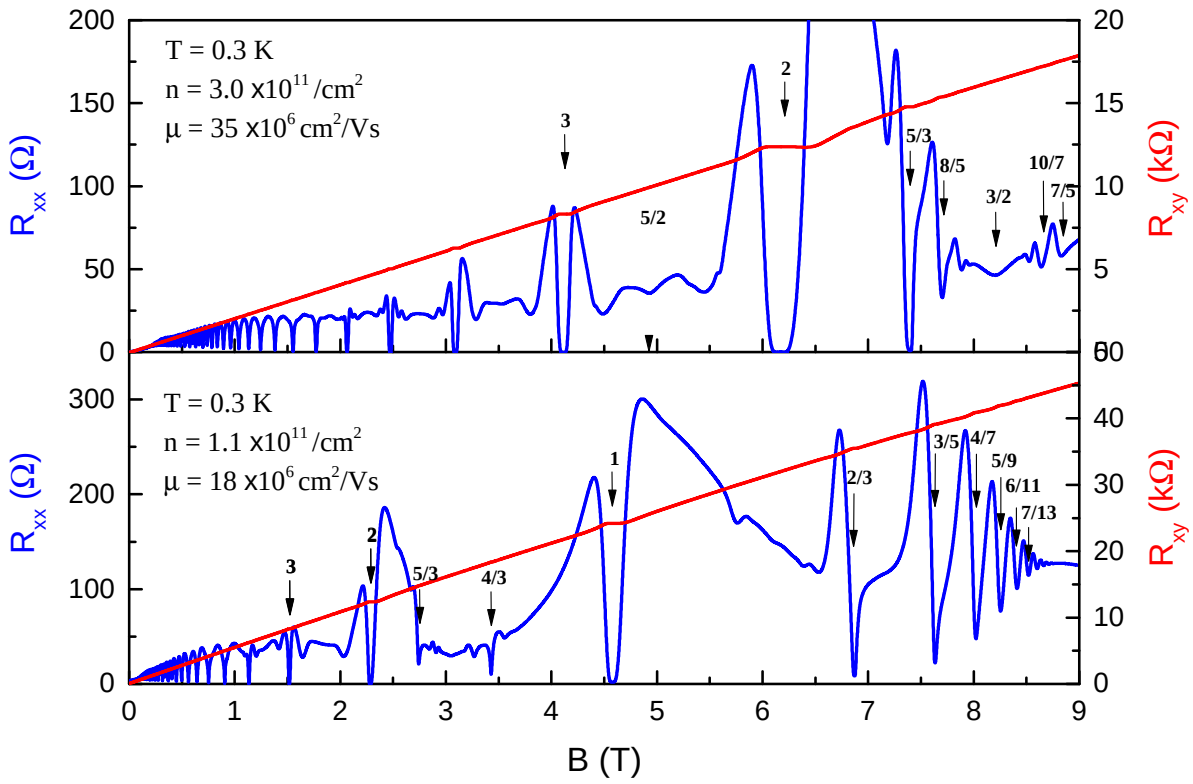


Fig. 1.13. The top panel shows transport data from a sample with mobility of $35 \times 10^6 cm^2/Vs$ and a density of $3.0 \times 10^{11} cm^{-2}$. The bottom panel shows transport data from a sample with lower density of $1.1 \times 10^{11} cm^{-2}$ and mobility of $18 \times 10^6 cm^2/Vs$ displaying strong fractional state development near $\nu = 1/2$. Reprinted from J. Cryst. Growth, vol. 441, G. C. Gardner, S. Fallahi, J. D. Watson, and M. J. Manfra, 'Modified MBE hardware and techniques and role of gallium purity for attainment of two dimensional electron gas mobility $> 35 \times 10^6 cm^2/Vs$ in AlGaAs/GaAs quantum wells grown by MBE', 71-77, Copyright 2016, with permission from Elsevier.

higher order fractions (e.g. up to $\nu = 11/21$ at T = 0.3 K) is an indication of not only high mobility but also of high 2DEG density uniformity and proper screening of residual potential fluctuations caused by the remote ionized donors.

# 2. LOW NOISE SI DOPED GAAS/ALGAAS HETEROSTRUCTURES FOR SPIN QUBIT

## 2.1 Introduction

Laterally gated semiconductor quantum dots are essential components for mesoscopic physics and are used to realize solid state qubit for quantum information processing. The term "qubit" represents the quantum analog of the classical bit (which refers to a basic unit of information with two states represented as 0 and 1, and is independent of the physical medium used to convey this binary information). For example, the spin state of an electron in a quantum dot is an ideal physical system for storing and processing quantum information [56,57]. Despite the conceptual similarities between qubits and classical bits, they differ in their practical use. As with classical bits, qubits convey information through binary states (typically these are the same states used by bits: 0 and 1). However, whereas the state of a bit may be either 0 or 1, a qubit may also occupy a superpositional state (simultaneously both 0 and 1) [58].

When a qubit is initialized in a superposition of two states and allowed to evolve, it precesses with a frequency proportional to the energy difference between the two states. Qubits are extremely sensitive to fluctuations in their local environment. When they interact with noisy environments, they experience decoherence. This leads to qubit oscillations decay, which limits the time scale in which qubits can be used for quantum information processing.

Two main sources of noise in semiconductors exist: charge noise and spin noise. Charge noise arises from occupation fluctuation of impurity trap centers (trapping and de-trapping of charge states) in the vicinity of qubits and results in the fluctuation of local electric fields. Due to spin-orbit interaction, charge noise can potentially cause

qubit spin dephasing. Spin noise can arise from fluctuations in the nuclear spins of the host material which is dominant in GaAs/AlGaAs heterostructures. Spin noise results in magnetic field fluctuation experienced by electron spin through hyperfine interaction. In general, charge noise results in large noise powers but only at low frequencies and the spin noise gives much weaker noise powers but over a much wider bandwidth [59].

This chapter investigates methods for minimizing charge fluctuation to produce reliably tunable and quiet platform for laterally gated nanodevices such as quantum point contacts (QPC) and quantum dots (QD). The chapter does not investigate phenomena related to spin noise. Because charge noises are dominant at low frequency regimes, the next section reviews low frequency noise studies for GaAs devices and describes various techniques which have been developed to reduce low frequency noise. The total number of silicon donors has been identified as an important parameter influencing low-frequency charge noise in modulation-doped $GaAsAl_xGa_{1x}As$ heterostructures. By reducing the total number of Si donors, quantum devices with minimal charge noise achieved that can serve as a robust, stable platform for spin qubit-based quantum computing.

## 2.2 Low frequency noise in GaAs nanodevices

Molecular beam epitaxy (MBE) growth is a technique for growing extremely pure GaAs/AlGaAs with minimal defects. However, the residual defects become more important as the dimensions of devices such as QPCs and QDs become smaller in nanometer scale. These residual defects may act as trap centers which randomly capture and emit charge carriers. This results in low frequency noise (such as burst and 1/f noise) and degradation of device performance at nanometer scale.

Li et al. provide the first experimental study on the noise characteristics of QPCs [60] at T=4.2K. The authors investigate low frequency noise in frequency span 100Hz<f<100kHz generated by electron transport through ballistic constriction. Ex-

perimental results shown in Fig. 2.1 demonstrate a linear increase in white noise with bias current, though lower than expected for full shot noise. Lesovik calculates

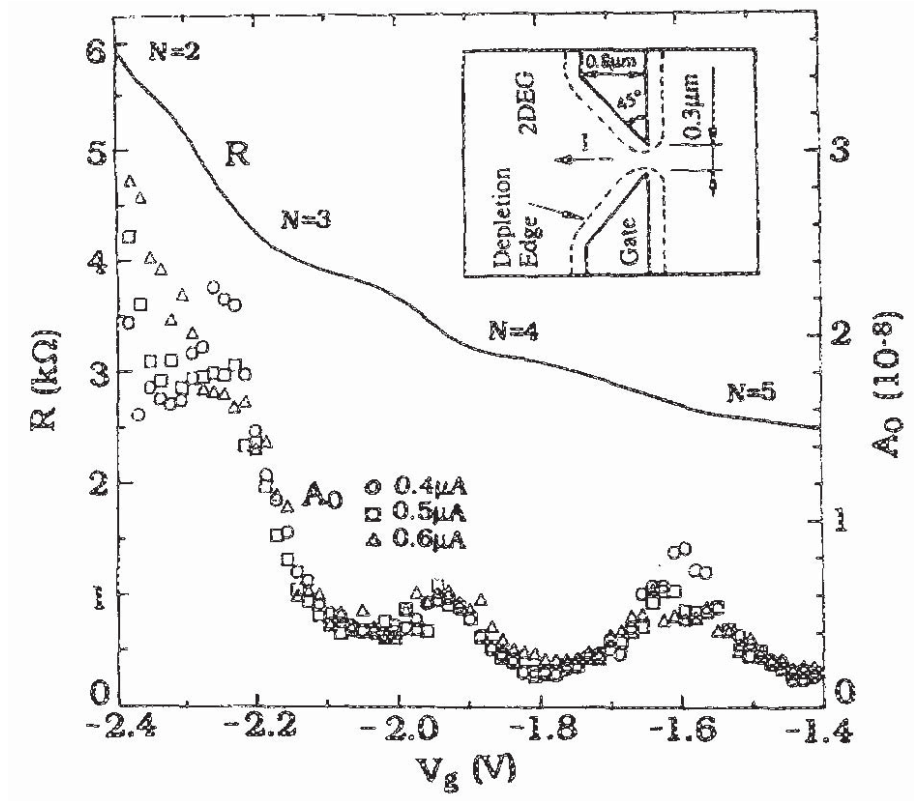


Fig. 2.1. R vs $V_g$ and $A_0$ vs $V_g$. $A_0$ is obtained by fitting $S_I$=$A_0I^2$/f + $S_0$ for I = 0.4, 0.5, and 0.6 $\mu$A. The approximate plateaus in R are assigned to the quantized resistances $h/2e^2$N, with N = 2,3,4, and 5. Inset shows the device geometry. Reprinted from Yuan P. Li et al.,'Low-frequency noise in transport through quantum point contacts', Appl. Phys. Lett. 57, 774 (1990), with the permission of AIP Publishing.

excess noise in quantum point contact theoretically [61]. The author predicts the suppression of shot noise in ballistic transport regimes in the center of conductance plateaus and demonstrates that the noise power measured in a 1D constriction with adiabatically tapered contacts is

$$S(\omega = 0) = (2e^2/h)V \sum_{j,k=1}^{N} t_{jk}(1 - t_{jk}) \tag{2.1}$$

where V denotes applied voltage. Therefore, shot noise vanishes on conductance plateau because $t_{jk} = \delta_{jk}$ (i.e., there is no scattering). If a defect in the constriction backscatters or reflects an electron from the constriction, the transmission probability $t_{jk}$ becomes less than unity. Thus, the conductance is reduced from the quantized value and noise can be observed.

In addition to shot noise, Li also reports on $1/f$ noise with an intensity that demonstrates minima whenever the conductance is set at a quantized conductance plateau. However, the origin of $1/f$ dependence of noise power and of minima in its intensity remained unclear. Subsequent work on QPC noise shows Lorentzian spectrum with $1/f^2$ frequency dependence [62–66]. The origin of Lorentzian noise spectral density is observed from measurements in the time domain in which the QPC resistance fluctuates randomly between two (or more) discrete values, spending on average time $\tau_d$ in low-resistive state and time $\tau_u$ in high-resistive state. In this two-state fluctuating case namely Random Telegraph Noise (RTN), the noise spectrum is given by [67]:

$$\frac{S_V(f)}{V^2} = \left(\frac{\Delta V}{V}\right)^2 \frac{4}{(\tau_u + \tau_d)} \frac{\tau_{eff}^2}{(1 + 4\pi^2 f^2 \tau_{eff}^2)} \tag{2.2}$$

with $1/\tau_{eff} = 1/\tau_u + 1/\tau_d$ and $\Delta V$ denotes the switching amplitude.

As with $1/f$ noise, intensity of RTN shows minima when conductance is set at a quantized conductance plateau. This aspect of the noise is universal. Reference [68] provides the explanation that the transmission of the 1D subband closest to its population threshold is more sensitive to changes in the local electrostatic potential. These potential changes are due to the fluctuation in occupancy of electron traps located at or near the point contact. The authors model the fluctuations at finite temperature via fluctuations in the effective number of transmitted channels (or equivalently in $\epsilon_F - \epsilon_0$). Lateral confining potential in the point contact is approximated by a parabola of strength $\hbar\omega_0$ and $\epsilon_n = \epsilon_0 + (n - \frac{1}{2})\hbar\omega_0$. Calculations below are based on assumptions of linear dependence of $\epsilon_0$ and $\hbar\omega_0$ with gate voltage $V_g$. Random changes in occupancy of trapping sites near QPC result in fluctuation of Coulomb

potential, the potential energy $\epsilon_0$ in the point contact with noise spectral density $S_{\epsilon_0}$. The relationship between $S_V/V^2$ and $S_{\epsilon_0}$ is given to first order by

$$\frac{S_V}{V^2} = \frac{S_G}{G^2} = \frac{1}{G^2}\left(\frac{\partial G}{\partial \epsilon_0}\right)^2 S_{\epsilon_0} \tag{2.3}$$

$$\frac{\partial G}{\partial \epsilon_0} = \frac{2e^2}{h}\frac{1}{k_B T}\sum_n f(\epsilon_n - \epsilon_F)[1 - f(\epsilon_n - \epsilon_F)] \tag{2.4}$$

with $f(\epsilon)$ the Fermi-Dirac distribution at temperature T. Both $G$ and $\partial G/\partial \epsilon_0$ are evaluated for the time-averaged value of $\epsilon_n$. The frequency dependence of $S_V/V^2$ is contained in $S_{\epsilon_0}$, while the G dependence of $S_V/V^2$ is contained in the $(\partial G/\partial \epsilon_F)^2/G^2$ term.

The universality of the quantum size effect is due to the term $(\partial G/\partial \epsilon_F)^2/G^2$ irrespective of the spectral dependence of $S_{\epsilon_0}$. In other words, temporal fluctuation in confining potential has the strongest effect on transport at the occupancy thresholds of the 1D subbands, where $\partial G/\partial \epsilon_0$ is largest. This is illustrated in Fig. 2.2 in which the electron energy $\epsilon = \epsilon_0 + (n - \frac{1}{2})\hbar\omega_0 + \hbar^2 k_x^2/2m$ is plotted vs. $k_x$ for the first several 1D subbands. $k_x$ is a component of the wavevector in the direction of electron propagation along QPC length. In the upper part of the figure when $\epsilon_F \approx \frac{1}{2}(\epsilon_1 + \epsilon_2)$ a small increment $\delta\epsilon_0$ of $\epsilon_0$ does not change the number of occupied subbands at $G \approx 2e^2/h$, while in the lower part of the figure where $\epsilon_F \approx \frac{1}{2}\epsilon_2$, a slight increase $\delta\epsilon_0$ of $\epsilon_0$ strongly affects the occupation of the 1D subband, resulting in a large change in G and a maximum in noise intensity.

This feature (increased sensitivity to small potential changes in the vicinity of QPCs) has been utilized to detect and read-out the occupation of the quantum dot states in solid state qubits in real time [32, 46, 50, 70, 71].

Other investigations reveal mechanisms of low frequency noise in modulation doped GaAs/AlGaAs heterostructures, including current leakage from surface gate through Schottky barrier [64, 72–74], electron hopping between 2DEG and trapping sites [68, 75], and electron hopping within the doping layer [62, 76, 77]. Experimental studies observe [77] that the noise level in laterally gated GaAs/AlGaAs heterostructures can be affected by gate voltage and low frequency charge noise increases as

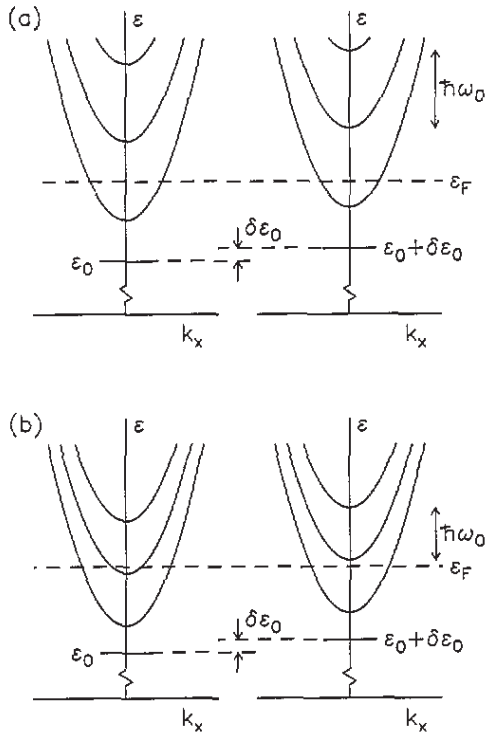


Fig. 2.2. Visualization of the quantum size effect in the noise intensity, with (a) $\epsilon$ versus $k_x$ for $G \approx 2e^2/h$, showing the small effect for $\delta\epsilon_0$ on G, and (b) $\epsilon$ versus $k_x$ for $G \approx 3e^2/h$, showing the strong effect for $\delta\epsilon_0$ on G. Reprinted from F. Liefrink et al. , Semicond. Sci. Technol., vol. 9, 2178-2189 (1994) [69]. IOP Publishing. Reproduced with permission. All rights reserved.

the gate voltage applied to the surface gate decreases and becomes more negative. A Schottky barrier reduces at more negative gate voltages and the observed gate voltage dependence of noise level is interpreted as evidence that the current leakage through a Schottky barrier is responsible for the charge noise.

For this reason, techniques for shifting the operation point to a less negative voltage to suppress charge noise in laterally gated devices fabricated on GaAs/AlGaAs heterostructures may be implemented. These include bias cooling [72] and the use of additional global top gates [73], both of which shift the operation point to a less negative voltage. An alternative approach to additional global top gates which may be more reliable is to introduce a thin insulating layer underneath the Schottky gates.

Subsequent sections of this report introduce each of these techniques in more detail and describe mechanisms of charge noise suppression for each technique.

### 2.2.1 Bias cooling technique

Laterally gated devices are normally cooled to cryogenic temperature with all gates grounded to the substrate. This is done in order to protect the device under test against electrostatic shocks. When using bias cooling techniques, a voltage $V_{gc}$ is applied between the gates and substrate while the device is cooled. This voltage is then removed at low temperature.

Literature demonstrates that, for structures with a uniform surface gate, bias cooling affects the degree of correlation established in the doping layer between the positively charged donors and the negatively charged DX centers, thereby influencing the 2DEG mobility [78,79]. This section focuses solely on the noise suppression effect driven by implementing bias cool technique and provides a model to illustrate why and how noise can be reduced by applying positive bias on the gates during sample cool down [73].

Figure 2.3 shows QPC gate voltage characteristic for different cool down bias voltages $V_{gc}$. For a positive (negative) bias, the gate voltage characteristic shifts towards less (more) negative voltages. In the inset, the shift of the depletion voltage is plotted vs the cooling bias. For small voltage biases, a built-in voltage forms during sample cooldown which is very close to $-V_{gc}$ and for higher voltage biases there is a very small deviation from $-V_{gc}$. A similar trend holds for the other threshold features such as the QPC pinch-off voltage.

Figure 2.3(b) shows that bias cooling has a dramatic effect on reducing random telegraph noise and causes the QPC to become quieter as $V_{gc}$ becomes more positive. In each curve, the QPC is set to its maximum sensitivity at the first conductance plateau riser i.e. $G \approx e^2/h$.

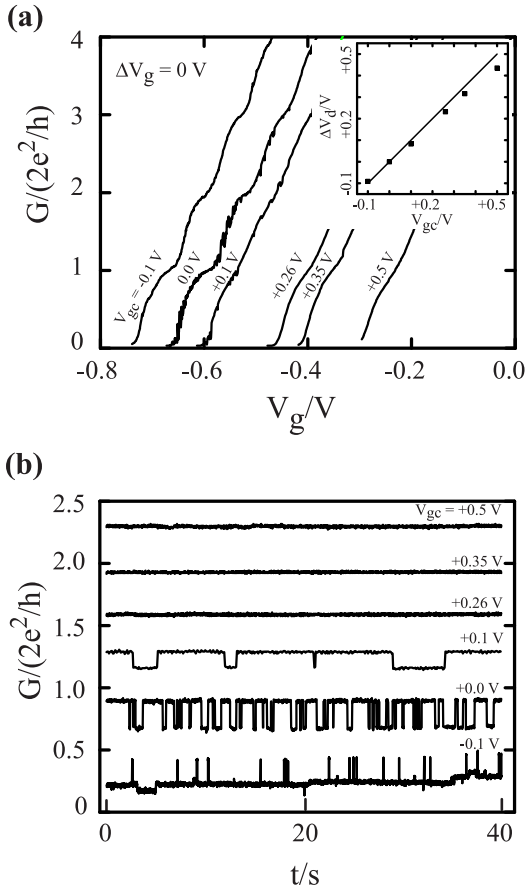


Fig. 2.3. Effect of bias cooling on random telegraph noise. (a) QPC gate voltage characteristics for bias voltages $V_{gc}$ applied during cool down. Inset: shift $\Delta V_d$ of the depletion threshold voltage measured for each cooling bias; line shows shift equal to the applied bias. (b) Time traces taken at maximum sensitivity of QPC conductance for each bias. Traces are shifted vertically for clarity. Reprinted figure with permission from M. Pioro-Ladrire et al., Phys. Rev. B 72, 115331 (2005) Copyright (2005) by the American Physical Society.

A proposed model explains the switching noise phenomenon and the effect of bias cooling on random telegraph noise. Figure 2.4 shows the conduction band in growth direction under a large gate on a sample that has been cooled with grounded gates (i.e. $V_{gc} = 0$). Three regions exist in the doped layer:

I. A thick ionized region closer to the cap which compensates surface states and generates the potential needed for the Schottky barrier on the surface. This

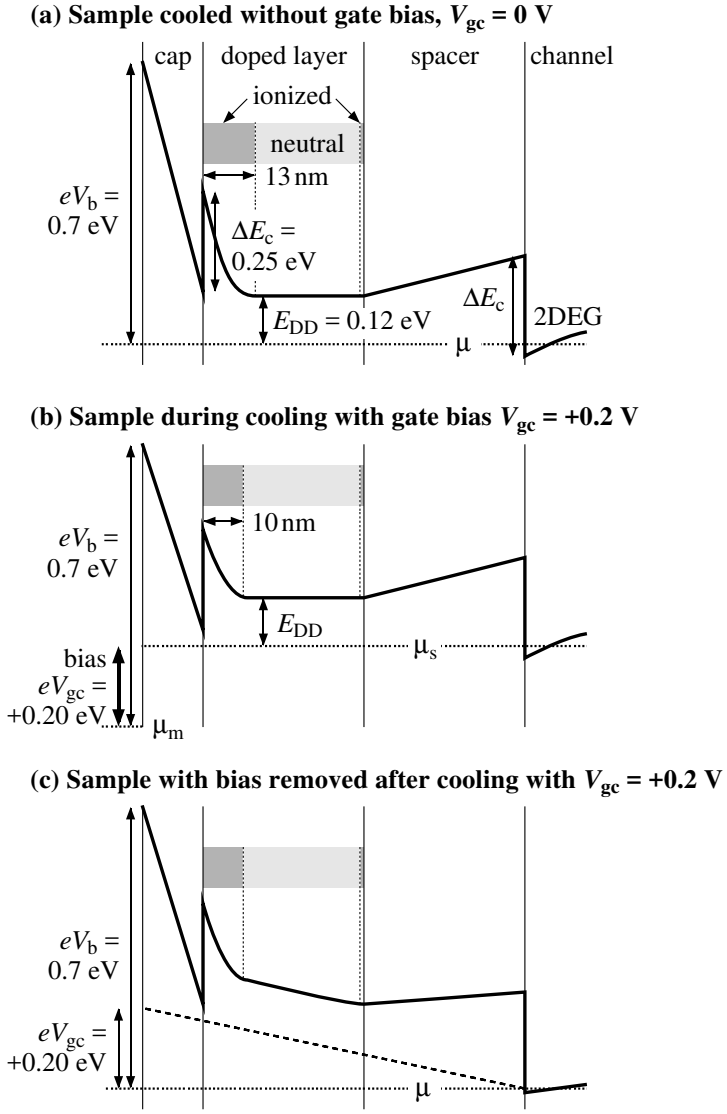


Fig. 2.4. Profiles of conduction bands under a large gate (a) for a sample without bias cooling, (b) during cooling with a positive gate bias of $V_{gc} = +0.2V$, and (c) after removing the applied bias in (b). The chemical potential of metal gate $\mu_m$ is pinned at an energy $eV_b$ below the GaAs conductance band by the large surface states while the semiconductor potential $\mu_s$ is pinned by DX centers at an energy $E_{DD}$ below the conduction band in the neutral (un-ionized) region of the doped layer. Reprinted figure with permission from M. Pioro-Ladrire et al., Phys. Rev. B 72, 115331 (2005) Copyright (2005) by the American Physical Society.

causes the conduction band to be lifted $eV_b$ above the Fermi level $\mu_m$ of the gate.

II. An unionized region in the middle of the doping layer. Here, electrons are trapped in DX levels, which pins the conduction band at an energy $eV_b$ above the Fermi level $\mu_s$ of the semiconductor . At no bias voltage $\mu_m = \mu_s = \mu$.

III. A thin ionized layer next to the spacer to transfer charges to the 2DEG. This layer is less than 1nm thick.

The unionized region is observed due to the wafer containing far more donors than are needed to compensate surface charges and 2DEG. This is a region which typically forms in doping layers. The model concentrates on uniformly doped GaAs/AlGaAs heterostructure, but also applicable to $\delta$-doped heterostructures.

During cooling with bias $V_{gc} = +0.2V$ on the gate, donors can easily change their occupation at room temperature when the bias is applied on the gates (see Fig. 2.4(b)). The mobile charge that are closer to the gate responds to the applied bias and attracts electrons into the doping layer. This reduces the thickness of the ionized region next to the cap from 13 nm to 10 nm. 2DEG is not affected.

When the sample is cooled below 100K, electrons in the doping layer become frozen in DX centers because the barriers to trapping and detrapping the electrons have become too high. Figure 2.4(c) shows the effect of removing the bias of $V_{gc} = +0.2V$ after sample has been fully cooled down; this is equivalent to applying a negative bias $Vg = -0.2$ to Fig. 2.4(b). Since the only mobile charges are electrons in the 2DEG, the density of the 2DEG reduces accordingly when the bias $V_{gc} = +0.2V$ is removed at low temperature. This confirms the hypothesis that a bias cooled at $V_{gc}$ becomes equivalent to a built-in gate bias of $V_g = V_{gc}$ at low temperature (plotted in the inset to Fig. 2.3(a)) where the data lie very close to a line of unit slope.

After removing the bias $V_{gc}$, the QPC is negatively biased to pinch it off. Suppose that the QPC width is designed such that it needs $Vg = 0.4V$ to pinch off when the sample is cooled without bias. Figure 2.5 (a) shows the conduction band along a line

that goes from a gate to the channel at the middle of the QPC. This line is not normal to the surface as in 2.4. The QPC is only just pinched off so that the conduction band in the midpoint of the channel touches Fermi level $\mu_s$. The negative bias on the gate raises its Fermi level $\mu_m$ by 0.4 eV, which permits electrons to tunnel into the 2DEG. This results in a current leakage and, consequently, to a telegraphic noise.

The leakage current can be classified into three regimes:

1. The current leakage is nearly insignificant for small negative bias because electrons must tunnel through the full thickness of the cap layer, doped layer, and spacer layers into the 2DEG.

2. The current starts to leak rapidly when the bias voltage rises to $eV_g > \Delta E_c \approx 0.25eV$ because electrons do not need tunnel through the spacer region.

3. As the bias voltage increases, the barrier for electrons at the Fermi level $\mu_m$ becomes narrower until electrons need to tunnel only through the cap layer and the shallow ionized layer of donors (less than 30 nm). Figure 2.5 (a) shows this limit.

Figure 2.5 (b) shows a case for the sample that has been cooled with positive bias $V_{gc} = +0.2V$. Due to the built-in potential of $-0.2V$, less negative voltage $V_g = -0.2V$ is required to reach the same operating point of Fig. 2.5 (a). Hence, a positive bias cool reduces current leakage because a smaller applied bias is needed for the same operating point of QPC.

Therefore, the origin of switching noise is determined to be caused by trapping and de-trapping of impurity sites driven by current leakage from surface gate. In pure telegraphic noise caused by current leakage, the electrons that tunnel from the surface gate reach the 2DEG region but may alternate between localized states before they reach 2DEG. If electrons tunnel to the 2DEG entirely through the conduction band, there is no switching noise. The position of these traps is predicted to be in the thin layer of ionized donors in the vicinity of the spacer layer. However, the origin of these trapping sites is not clear.

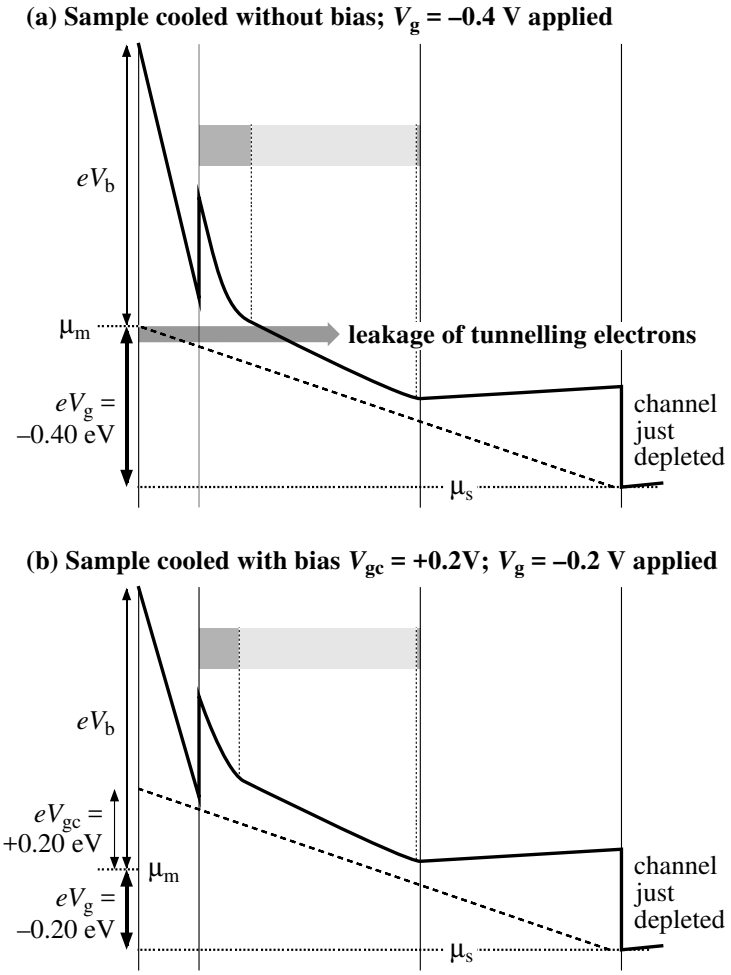


Fig. 2.5. (a) Conduction band profile for a gate voltage of $V_g = 0.4V$ applied to a sample without bias cooling. Electrons can are able to tunnel from the gate into the doped region. (b) Conduction band profile for the same operating point after a bias cool of $V_{gc} = +0.2V$. Because of the built-in gate voltage, only $V_g = 0.2V$ is needed to reach the same effective gate voltage of 0.4 V. Tunneling into the doped layer is no longer possible. Reprinted figure with permission from M. Pioro-Ladrire et al., Phys. Rev. B 72, 115331 (2005) Copyright (2005) by the American Physical Society.

### 2.2.2 Global top gate technique

This section reviews the effect of additional insulated top gates in reducing random telegraph noise in QPCs and the mechanism behind noise power reduction. The

work of Vandersypen's research group at Delft [73] demonstrates these effects. Figure 2.6 (a) shows QPC gate layout fabricated on GaAs/AlGaAs heterostructure with 90nm 2DEG depth. A uniform gate is positioned on top of these gates with dimension much larger than QPC gates separated by a 100nm thick calixarene insulating layer. Applying voltage $V_g$ on QPC depletes 2DEG underneath and creates a narrow constriction for electrons to pass through. The conductance through the QPC is plotted for two values of applied voltage on insulated top gate. Applying a negative bias on the top gate shifts the QPC pinch-off voltage to a less negative voltage.

Figure 2.6 (b) shows the effect of the top gate on suppression of random telegraph noise. Traces shown in Fig. 2.6 (b) are obtained by applying negative voltage on top gate in -0.2V increments. Accordingly, QPC gate voltage is made more positive to return the QPC to its operating point (i.e. $G_{QPC} \approx e^2/h$). The topmost trace in Fig 2.6 (c) shows a Lorentzian spectrum which is typical of two-level random telegraphic noise. The spectrum falls off at $1/f^2$ above corner frequency $f_c = \tau_{eff}^{-1} = \tau_u^{-1} + \tau_d^{-1}$. $\tau_u(\tau_d)$ represents the average time spent in low- and high-current states (as described in section 2.2). By eliminating RTN via top gate voltage, the frequency dependence of power spectral density goes from $1/f^2$ to $1/f$, indicative of an ensemble of weak fluctuators with homogeneous distribution of time scale $\tau_{eff}$.

From the dependence between RTN and gate voltages, it is clear that electron tunneling is main root cause of switching events. This tunneling occurs from metal gates through a Schottky barrier to trapping sites in the AlGaAs layer and subsequently to the 2DEG. Vandersypen's analysis is based on changes in trapping $\Gamma_{in} = \tau_d$ and release $\Gamma_{out} = \tau_d^{-1}$ rates for electrons tunneling from metal gate to trapping sites and release to the 2DEG. This is shown in Fig. 2.7 (b), assuming a deep trapping state in the band structure. By applying more negative voltage on the top gate, the Schottky barrier becomes higher. More negative voltage on top gate also raises trap energy relative to $\mu_m$ and reduces the number of available states for electrons to tunnel from the metal gate. By making top gate voltage to be more negative, the trap energy may be raised above $\mu_m$ and eventually leakage can be suppressed. Figure 2.7

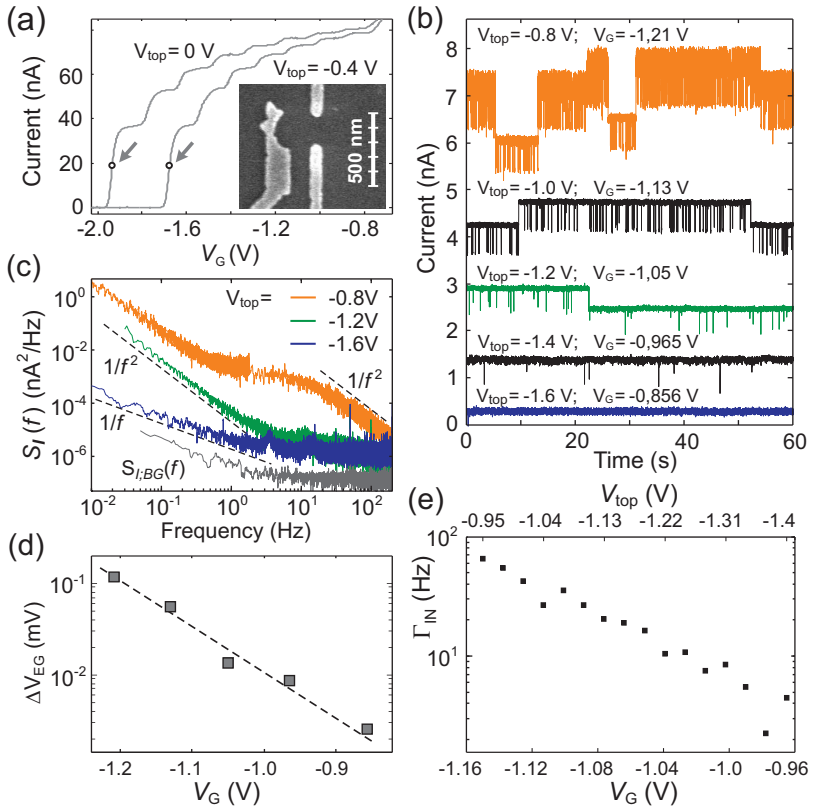


Fig. 2.6. (a) QPC pinch-off curves (two terminal, $V_{SD}$ = 0.8mV, T = 40 mK). The operating point is marked at the first riser of quantum conductance plateau. Inset: a Scanning Electron Micrograph of a typical device layout before deposition of the insulated top gate. (b) QPC time traces for indicated gate voltages, offset for clarity. (c) Power spectra density $S_I$(f) from FFT of time traces; setup noise background $S_{I;BG}$(f) recorded at zero $V_{SD}$. (d) Equivalent gate voltage noise $\Delta V_{EG}$. (e) Measured trapping rate in extracted from time traces as in (b), but for a different QPC. Reprinted figure with permission from C. Buizert et al., Phys. Rev. Lett. 101, 226603 (2008) Copyright (2008) by the American Physical Society.

(c) shows electric field lines for two configurations with and without top gate bias. Release rate for trapped electrons $\Gamma_{out}$ depends on the electric field at the location of trap center. By applying top voltage, the strength of the electric field reduces, thus reducing charge noise. Considering the nature of traps causing switching noise, the authors questioned the possible cause of DX center as a trapping site on charge noise

(as is claimed often) [73] by studying charge noise on different modulation doped GaAs/AlGaAs heterstructures with Al mole fractions ranging from x=0.1 to x=0.3. They found that the noise level is greatest in the x=0.1 sample, while the sample with x=0.3 demonstrates the least noise. For this reason, DX center is excluded from being a dominant trapping site that causes random telegraph noise.

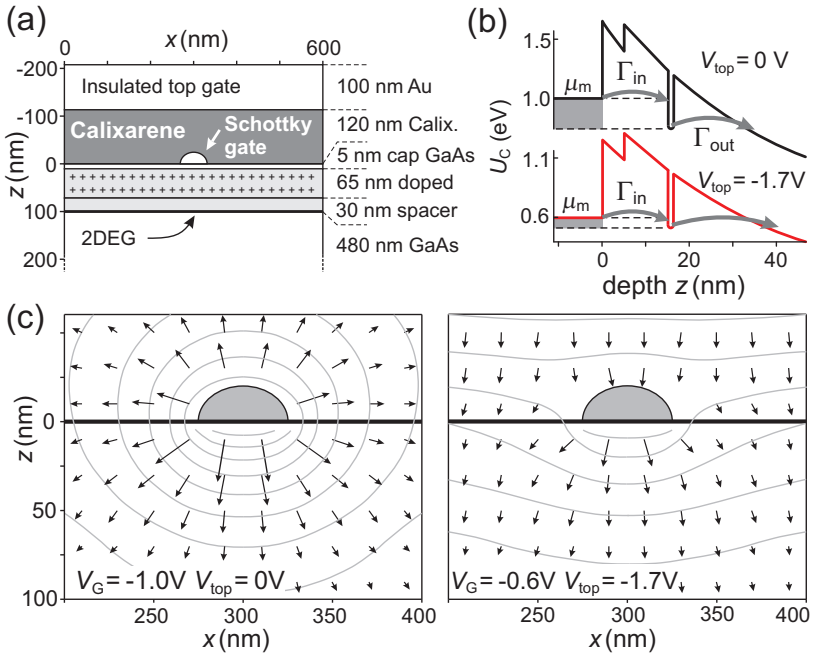


Fig. 2.7. (a) Simulated 2D device structure with $Al_{0.26}Ga_{0.74}As$ doped- and spacer layer. Si doping $n_{Si} = 0.3 \times 10^{18} cm^{-3}$; Calixarene simulated as $SiO_2$ with $\epsilon_r$=7.1. (b) Simulated conduction band profile under the Schottky gate at x=300 nm. Tunneling into a localized trap with fixed energy below $U_C$ occurs most easily from the quasi-Fermi level in the metal lead ($\mu_m$) where the barrier is lowest (this is generally an inelastic process). (c) Quiver plot of the simulated electric field and equipotential lines near the Schottky gate (gray shaded) for the indicated voltage configurations. Reprinted figure with permission from C. Buizert et al., Phys. Rev. Lett. 101, 226603 (2008) Copyright (2008) by the American Physical Society.

Laterally gated nanostructures such as QDs and QPCs are used to realize solid qubits and are essential building blocks for research in the field of mesoscopic physics. Such devices fabricated on modulation doped GaAs/AlGaAs heterostructure may

suffer from random telegraph noise and drift in operating gate voltage, resulting in device instability and decoherence. Charge noise is due to either (1) current leakage through the Schottky barrier and/or (2) electron hopping within the doping layer. Techniques exist which suppress charge noise via bias cooling and additional global top gate which shift the operation point to less negative voltage. However, these techniques do not remove the root cause of charge noise. This thesis addresses the root causes of low frequency charge noise and demonstrates the elimination of charge noise via hetrostructure engineering and reducing doping density. Its aim is to produce a quiet platform for mesoscopic physics and spin qubit research.

Via heterostructure engineering, the effective barrier for electron tunneling increases. Hence, results in charge noise reduction are caused by electron leakage from surface gates. By reducing doping density, the interatomic distance between donors increases, which causes the charge noise to decrease due to electron hopping within the doping layer.

## 2.3 Impact of silicon doping on low frequency charge noise and conductance drift in GaAs/AlGaAs nanostructures[1]

In order to study the effect of doping concentration on low frequency charge noise, modulation doped GaAs/$Al_{0.36}Ga_{0.64}As$ heterostructures with three different silicon doping densities $N_D$, $2.4 \times 10^{18}cm^{-3}$(Wafer A), $4.2 \times 10^{18}cm^{-3}$(Wafer B) and $6.0 \times 10^{18}cm^{-3}$(Wafer C) were investigated. These uniformly doped single interface heterostructures were grown by MBE with a 60nm AlGaAs spacer between the 2DEG and the doping region (14.5nm thick) and total 90nm 2DEG depth measured from the top surface. An overview of sample parameters is given in Table 2.1. We note that the heterostructure design of Wafer B is frequently implemented to fabricate spin qubits, and recent advances in two-qubit gate operation have been made with this design [50]. In Fig. 2.8 we show the conduction band profile for Wafer B simulated

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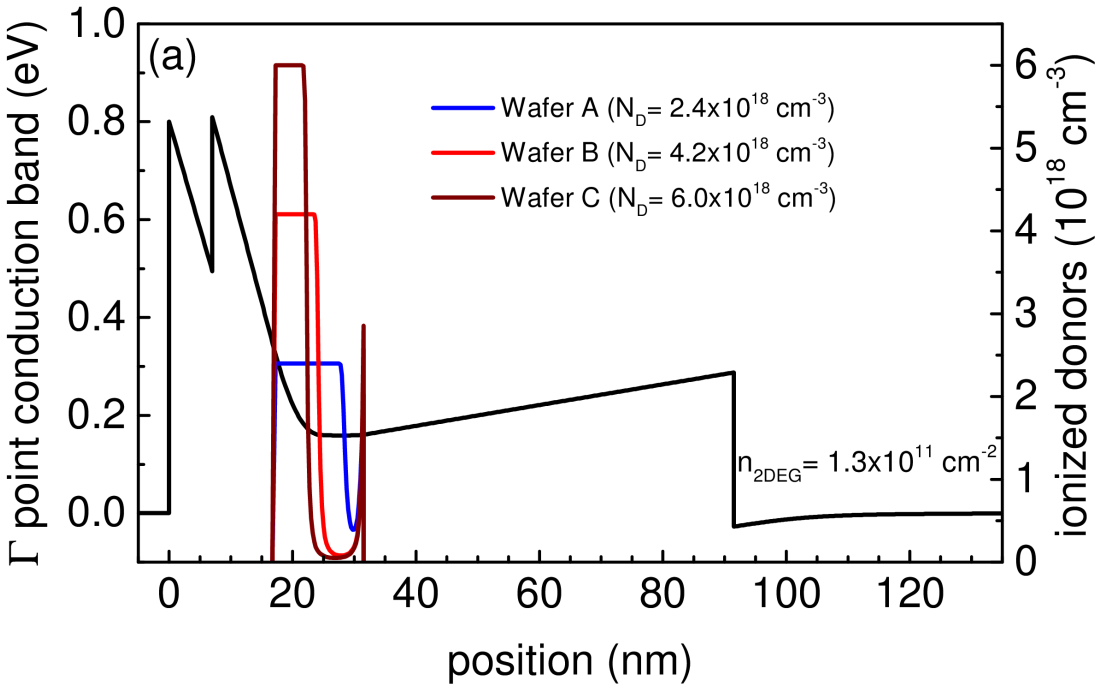


Fig. 2.8. Simulated heterostructure band diagram for uniformly doped single interface heterojuntion with varying doping density. Colored solid lines are the ionized donor profile for each doping concentration.

using the Nextnano software package [19]. We also show the ionized donor density for wafers A, B, and C.

Three distinct regions exist in the doping layer for each wafer: (1) a positively charged region closer to the cap layer that compensates surface states and produces a Schottky barrier $eV_b \sim 0.8eV$ at the surface; (2) a neutral region in the middle of the doping layer, where the Fermi level is located at an energy $E_D \sim 150meV$ [18,80] below the conduction band edge; and (3) a thin ($<$ 1nm) positively ionized layer from which electrons have been transferred to the 2DEG.

Microscopically, the neutral region is believed to be composed of positively and negatively charged Si donors with almost the same concentration. According to

Table 2.1
Characteristics of studied wafers including Si doping concentration $N_D$, doping width W, 2DEG density n, mobility $\mu$, operating gate voltage $V_g$, number of QPCs measured and Ohmic contact resistance for each wafer. The size of each Ohmic contact is 150$\mu$m×150$\mu$m.

| Wafer Name | $N_D$ ($cm^{-3}$) | W (nm) | n ($cm^{-2}$) | $\mu$ ($cm^2$/Vs) | $V_g$ (V) | # of QPCs measured | Ohmic contacts (Ω) |
|---|---|---|---|---|---|---|---|
| Wafer A | $2.4\times10^{18}$ | 14.5 | $1.1\times10^{11}$ | $2.7\times10^{6}$ | -0.5 | 6 | 140 |
| Wafer B | $4.2\times10^{18}$ | 14.5 | $1.3\times10^{11}$ | $5.1\times10^{6}$ | -0.6 | 3 | 60 |
| Wafer C | $6.0\times10^{18}$ | 14.5 | $1.4\times10^{11}$ | $4.7\times10^{6}$ | -0.6 | 6 | 50 |

negative-U model proposed independently by Chadi and Chang [18], and Khachaturyan, Weber, and Kaminska [81], the substitutional Si donor in $Al_xGa_{1-x}As$ (for Al mole fraction $x > 0.2$) occupying a Ga site has two possible electronic states: 1) a shallow donor level $E_d$ with no lattice relaxation and 2) a deep and localized donor level $E_{DX}$ with large lattice relaxation which binds two electrons. Based on the negative U-model, half of the donors in the neutral region are positively charged (ionized) shallow $d^+$ and the remaining half are negatively charged $DX^-$ states.

Importantly for our experiments, the doping width is kept constant at 14.5nm for the three wafers A, B and C; only the silicon doping density is varied. As charge transfer to the 2DEG is determined by the constant conduction band offset and setback, an increase in doping density does not significantly change the 2DEG density or the charge transferred to the surface. Rather, the width of the neutral region increases, as is seen by comparing the blue, red, and brown traces in Fig. 2.8. Wafer A is close to critical doping (meaning that nearly all dopants are positively ionized); if the doping were exactly critical there would be no neutral region. At the other extreme, Wafer C is significantly overdoped and has a large neutral region. Due to the presence of DX centers, the electrons in this neutral region can be frozen at low temperatures (below 100K) [82, 83]; no parallel conduction is observed in magnetotransport measurements (not shown). It has been experimentally found that doped GaAs/AlGaAs heterostructures in which DX centers form exhibit lower charge noise than structures without DX centers [73]. Additionally, we observe that after brief illumination with

a red LED at T = 4.2K, the 2DEG density of these structures increases significantly. This persistent photoconductivity is a signature of DX centers and confirms that our heterostructures are doped in the regime in which DX centers form; however, all of our charge noise measurements are performed without any illumination.

It is noteworthy that the mobility of Wafer A is nearly a factor of two lower than the mobilities of Wafers B and C. It has been shown that a correlation between the positively ionized $d^+$ states and negatively ionized $DX^-$ states results in a significant enhancement of mobility in overdoped structures [84, 85], however, nearly all the donors must be positively ionized in Wafer A; thus no correlation is possible for this wafer, resulting in lower mobility.

We utilized QPCs as charge sensors to detect charge noise. QPCs with a nominal width of 300nm were fabricated on all wafers using identical fabrication procedures to compare the level of charge noise for each wafer. An SEM image of a typical QPC is shown in the inset to Fig. 2.9. The processing steps are as follows: (1) photolithography of mesa pattern and mesa etch, (2) photolithography of ohmic contacts; evaporation of Ni/Au/Ge metal contacts and annealing (3) Electron beam lithography and evaporation of QPC gates with a 10nm Ti/25nm Au metal stack (4) photolithography and evaporation of bonding pads to wire bond devices to a chip carrier for measurement.

Each processing step runs the risk of damaging the wafer. Several measures were considered in order to minimize process induced damage (as well as it its potential effects on noise behavior). One of these measures is to minimize water usage on GaAs chips, as Deionized (DI) water can etch native oxide on the wafer and potentially change its surface chemistry. This is especially problematic for critically doped wafers on which any small perturbation of surface chemistry will compromise 2DEG density significantly. High energetic electrons used during E-beam lithography can expose areas of the wafer and cause 2DEG depletion in the exposed region. To minimize this effect, thicker PMMA (A4) with 200 nm thickness at 4000 rpm and 20keV electron energy has been used in this thesis. Previous attempts employed PMMA (A2) with

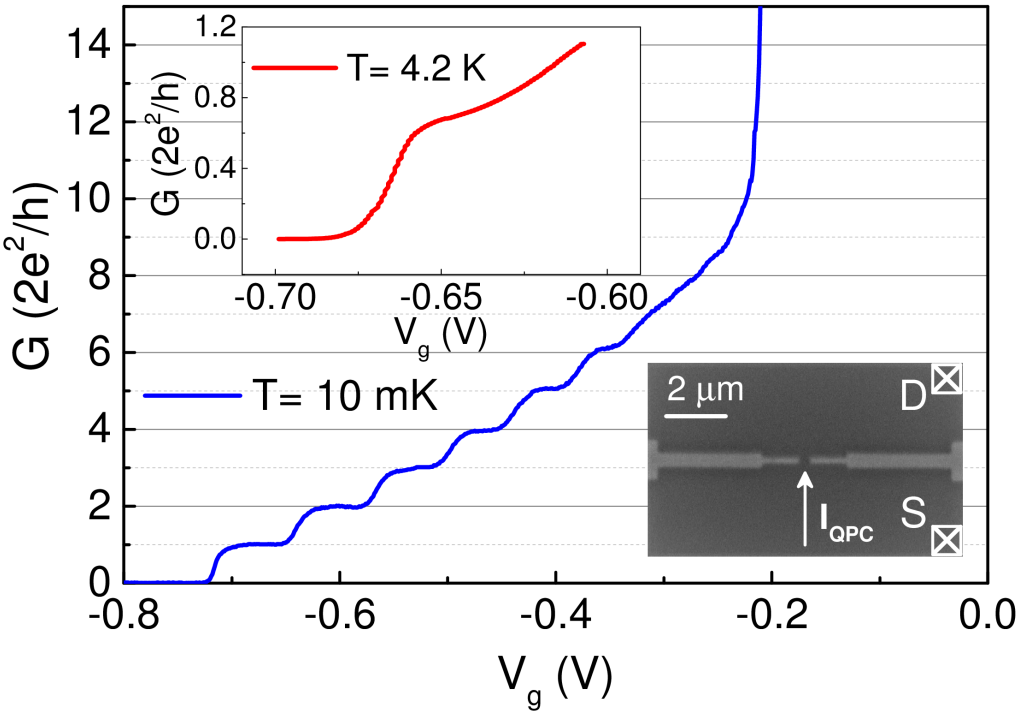


Fig. 2.9. Conductance G of a QPC as a function of gate voltage $V_g$ at T=10mK. Top inset: first riser of QPC conductance at T=4.2K. Bottom inset: SEM image of fabricated QPC on Wafer B.

60 nm thickness at 4000 rpm, which resulted in an increase of 3 orders of magnitude in 4-terminal resistance between ohmic contacts on the sides of QPC at zero gate voltage. This indicated that the area under the exposed region had already been depleted as a result of exposure to the E-beam. Lower E-beam energy can be used to reduce E-beam damage on the wafer at the expense of a reduction in pattern resolution.

Figure 2.9 shows a typical conductance plot of a QPC as a function of gate voltage $V_g$ taken in a dilution refrigerator with a mixing chamber plate temperature T=10mK; the conductance is quantized in units of $2e^2/h$ corresponding to discrete conductance modes of the device. Bias cooling is not employed in any of our experiments. The gate

voltage required to deplete the 2DEG beneath the gates is essentially identical for all the studied wafers and equal to -185 mV. The geometric capacitance between the gate and 2DEG is C=$\epsilon_0\epsilon_r$/d per unit area where d equals the 2DEG depth beneath the top surface. Assuming only coupling between the gate and 2DEG, we calculated the depletion gate voltage $V_{dep} = en/C = -180mV$ for $n = 1.3 \times 10^{11} cm^{-2}$. This nearly perfect agreement implies that charges in the neutral region do not respond to gate voltage and are frozen at low temperature.

The top inset shows the first riser in QPC conductance at T = 4.2K, where we operated the devices for noise measurements. At T = 4.2K, higher conductance plateaus are washed out but the QPC still has very high transconductance on the riser of the first quantized conductance plateau, making it very sensitive to the position of individual charges in the vicinity of the device.

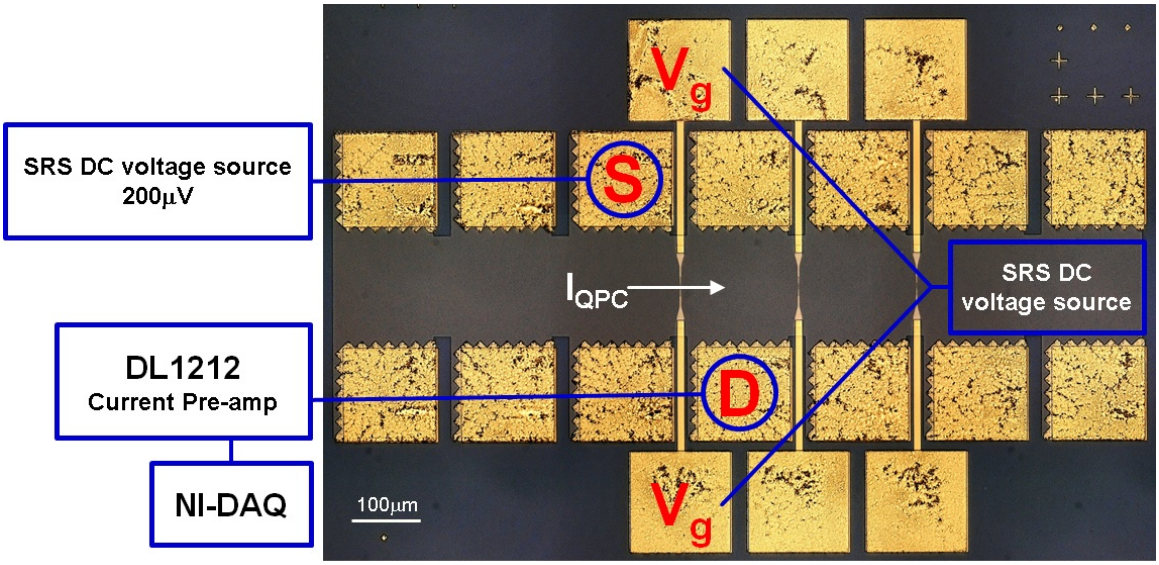


Fig. 2.10. Device layout and schematic picture of experimental setup for noise measurements. Three QPCs are being charachterized on single Hall bar device. Low noise DC source is used which is an essential component for ultra sensitive noise measurements.

Figure 2.10 shows device layout and QPC noise measurement setup. This measurement setup is a two-terminal measurement technique which a 200 $\mu V$ DC voltage is applied to the source and drain current is measured by a low noise current preamplifier (i.e. DL1212) fed to National Instruments NI-DAQ digitizer. Background noise due to the measurement setup is measured at $V_{SD} = 0$ and subtracted from total noise at finite $V_{SD}$ to obtain excess noise in the QPC.

**Short time scale conductance fluctuations**

The most striking observation of our study is the dramatic increase in low frequency noise associated with increased doping density as shown in Fig. 2.11. Conductance time traces for QPCs sitting at the first riser of conductance are shown in Fig. 2.11 (a) for QPCs from wafers A, B, and C. Note that the operating gate voltage is nearly indentical in all three cases. The conductance of the QPC on Wafer A is nearly constant, indicating that this QPC suffers minimal charge noise. The QPC from Wafer B shows increased noise and discrete switching events, while the QPC from Wafer C shows significant noise amplitude and severe RTN visible in the raw data. Clearly, the level of charge noise increases as the doping density is increased. The noise power spectral density, obtained from a Fast Fourier Transform (FFT) of the time traces, is shown in Fig. 2.11 (b). For comparison, the noise power spectrum of the measurement circuit with zero source-drain bias applied to the device is also shown. The increase of RTN as doping density is increased is reflected in the frequency dependence of power spectral density, which shifts from 1/f (for the lowest doping density) indicative of a broad ensemble of trapping sites with a homogeneous distribution of switching time scales to Lorentzian dependence $1/f^2$ (for the highest doping density) indicative of the strong influence of proximal two-level traps [86].

We quantify the noise level for each wafer in terms of equivalent gate voltage noise $\Delta V_g$, given in Eq. 2.5 (this represents the voltage noise level applied on the QPC gates that would produce the same conductance fluctuations as caused by the charge

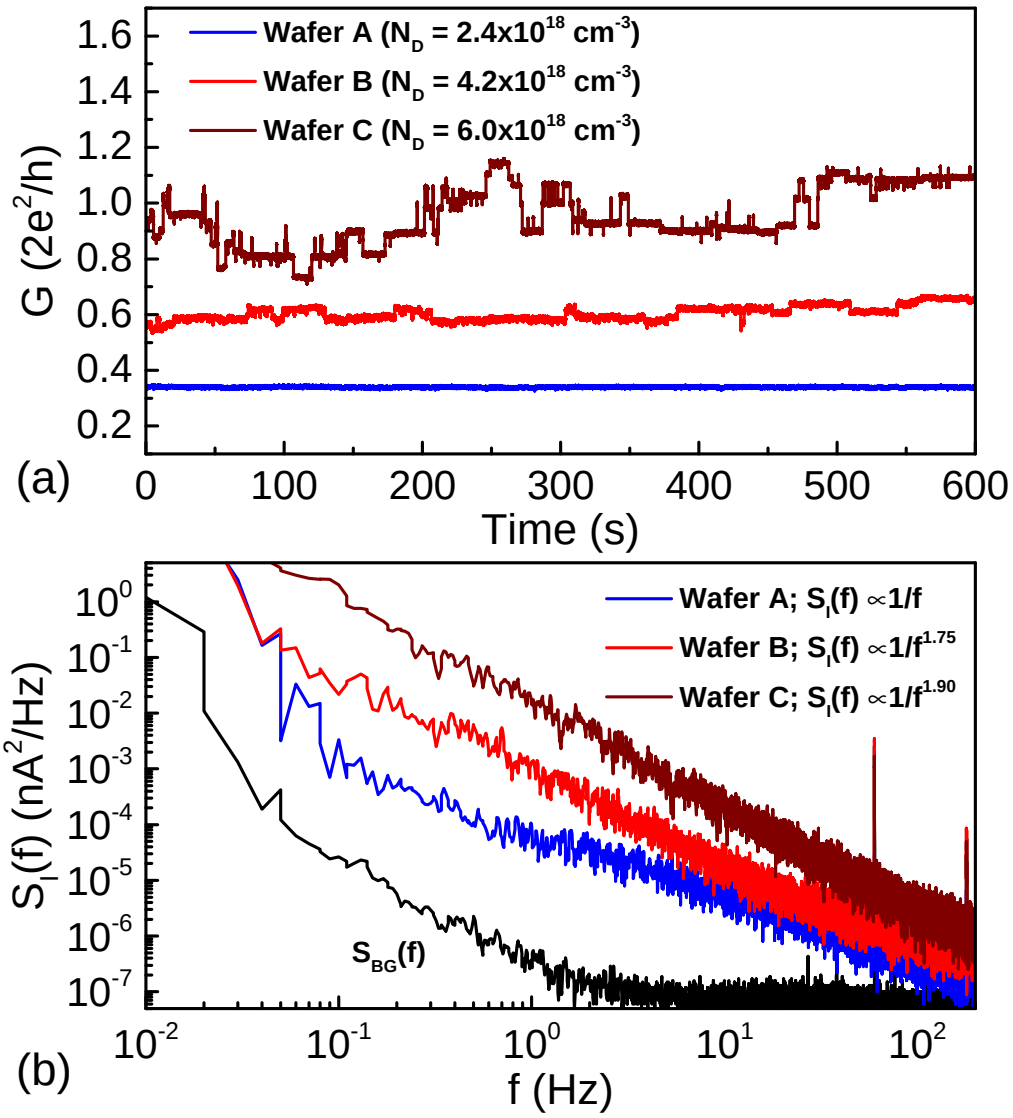


Fig. 2.11. (a) QPC time traces for structures with different doping densities, offset for clarity (Wafer B is offset by $0.2 \times (2e^2/h)$ and Wafer C is offset by $0.4 \times (2e^2/h)$) (b) Noise power spectral density $S_I(f)$ obtained from FFT of time traces, experimental background noise $S_{I;BG}(f)$ measured at zero source drain voltage (black trace).

noise) [87]. In Eq. 2.5, $S_I(f)$ is the power spectral density of current fluctuations through the QPC and $S_{I;BG}(f)$ is background noise due to noise in our instruments.

$$\Delta V_g = \sqrt{\int_{0.1Hz}^{100Hz} [S_I(f) - S_{I;BG}(f)]df} \Big/ \left(\frac{dI_{QPC}}{dV_g}\right) \tag{2.5}$$

Fig. 2.12 shows the equivalent gate voltage noise vs. doping density for each wafer. Each data point represents the average of different QPCs from each wafer; six QPCs were measured from Wafer A, three were measured from Wafer B, and six were measured from Wafer C. This plot shows a correlation between the noise level and doping density. In particular, the equivalent gate voltage noise is substantially larger for the highest doping density wafer, Wafer C, as is the device to device variation as indicated by the increase of the standard error.

According to the negative-U model, the neutral region of the doping layer is expected to contain ionized shallow donors ($d^+$) that may act as trapping sites and contribute to charge noise. Prevailing theory suggests that electrons tunneling from the Schottky gates are temporarily trapped on these sites and contribute to noise. As our heterostructures are essentially identical apart from the doping density, the operating voltages are nearly identical. This implies that the tunneling matrix element for electrons leaking from the surface gate are the same for all three wafers. Since the noise clearly increases as a function of doping density, we propose that the *number* of trapping sites (shallow ionized $d^+$ donors) within the neutral region has a primary impact. The noise level increases due to the increasing width of the neutral region and corresponding increase in available donor states. We are in essence increasing the final density of states for the tunneling process which leads to enhanced low frequency noise. While this analysis clearly suggests that heterostructures should be minimally doped to reduce low frequency noise, other considerations including formation of low resistance ohmic contact and production of high mobility 2DEGs make determination of optimal doping a subtle optimization problem.

**Long time scale conductance drift**

The second phenomenon we investigated is drift in conductance over long time scales at fixed gate voltage. A typical conductance time trace upon initial cool down for a QPC sitting on the first riser of conductance plateau is shown in Fig. 2.13 (a).

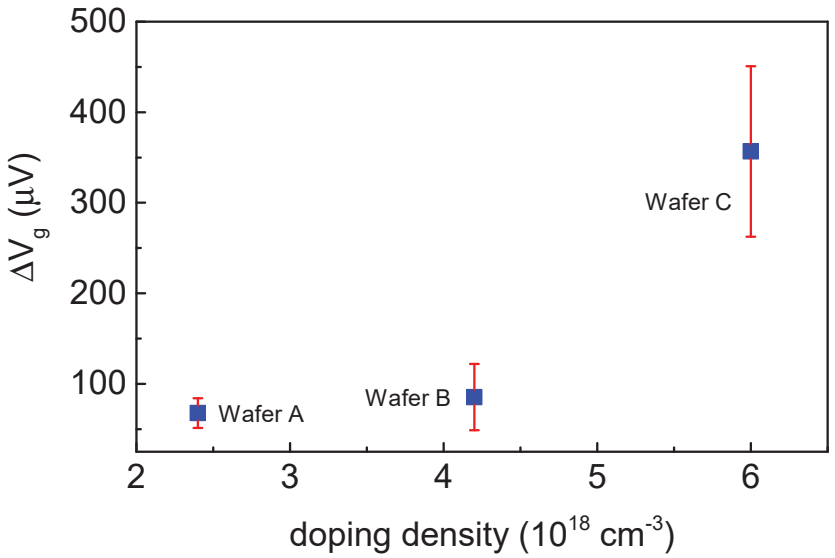


Fig. 2.12. Equivalent gate voltage noise $\Delta V_g$ vs. doping density for Wafers A, B and C. Each data point represents the average of different QPCs from each wafer. Six QPCs were measured from Wafers A and C, and three QPCs were measured from Wafer B. Error bars represent the standard error computed from the measurements of different QPCs from each wafer.

Although both negative and positive jumps in conductance occur, the overall trend is that conductance *decreases* over time at fixed gate bias; equivalently, the operating point of the QPC shifts to *less negative* voltage over time. We observed this trend for all QPCs cooled with the gates grounded and then energized at T=4.2K. Typically the largest amount of drift occurs within the first 24 hours after initially biasing the QPC at low temperature, after which the conductance starts to saturate.

We quantify the amount of drift exhibited by each sample as the shift in gate voltage required to operate the QPC on the first conductance riser after 24 hours. This quantity is plotted for each wafer in Fig. 2.13 (b); the data is from the same

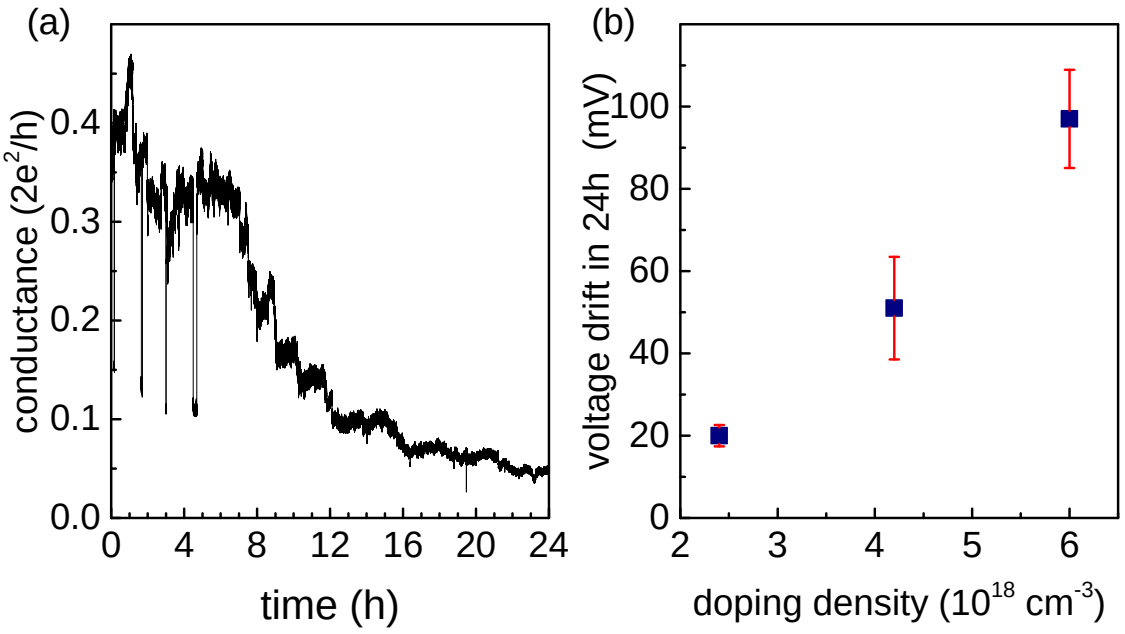


Fig. 2.13. (a) Long time scale conductance drift. (b) Total amount of gate voltage drift within 1st 24 hours of operation of QPCs for wafers A, B and C with different doping densities.

QPCs which were used to characterized noise. As with the RTN, it is clear that the level of QPC drift increases with increasing doping density.

Our data suggests that the drift phenomenon may be understood in the following way. Applying negative voltage to the surface gates raises the chemical potential at the gate, $\mu_{gate}$, relative to the chemical potential of the 2DEG, $\mu_{2DEG}$ that is connected to ground. Because the doping layer lies between the gate and the 2DEG, the chemical potential at the doping layer will tend to increase so that it is intermediate between $\mu_{gate}$ and $\mu_{2DEG}$, leading to an increase over time in the average occupation of donor states. Each time an electron tunnels to a donor site near the QPC, the repulsive potential causes a *negative* jump in the conductance of the QPC. However, because of the substantial tunneling barrier between the surface and the doping layer, the average occupation of donor sites increases slowly; the chemical potential at the doping layer

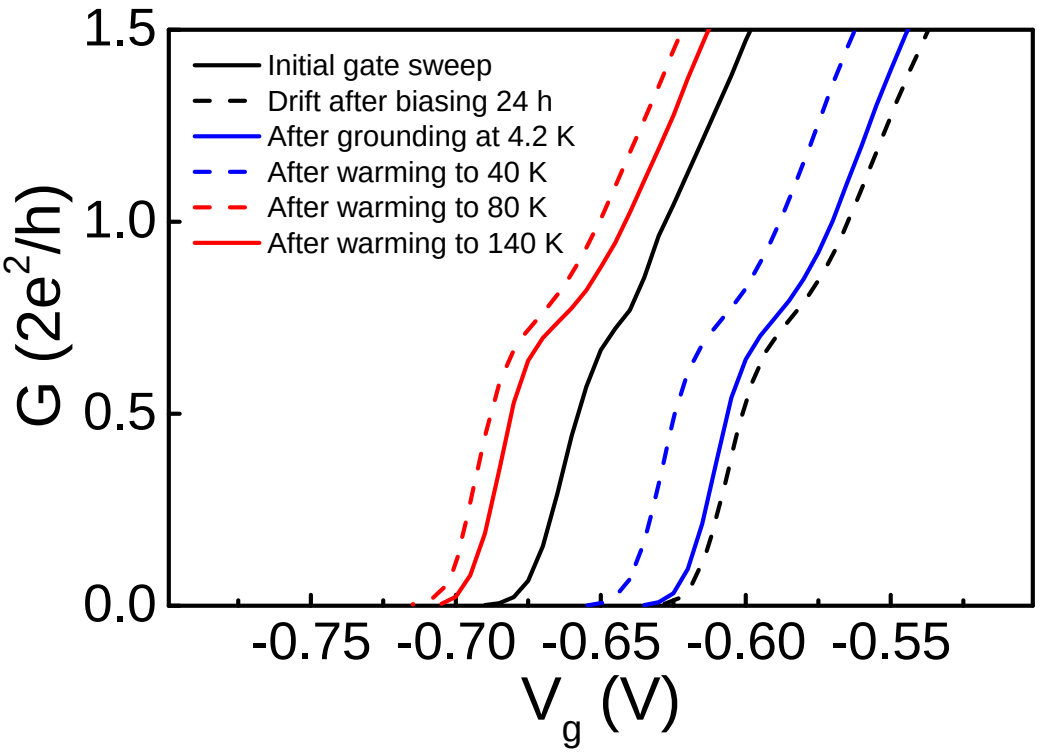


Fig. 2.14. QPC conductance plot vs gate voltage for Wafer B after warming up the QPC to T= 40K, 80K and 140K.

slowly rises as electrons tunnel to the available donor states before saturating at a steady-state value. The dynamics and saturation of this long time scale behavior may also be impacted by the complex electric field configuration in the immediate vicinity of the gate edges where the the electric field has both vertical and horizontal components. Additionally, the fact that the drift occurs over time scales much longer than the RTN suggests that drift may involve deep donor levels with a barrier to electron capture [18], whereas RTN may primarily involve shallow donor $d^+$ levels.

**Origin of conductance drift**

We performed an additional experiment to investigate the temperature stability of the charge accumulation associated with the conductance drift phenomenon. A QPC from Wafer B was biased on the riser of the first conductance plateau at T = 4.2K for 24 hours; significant conductance drift occurred during this period, consistent with the trend shown in Fig. 2.13. The shift in the conductance vs. gate voltage curve due to drift is shown in Fig. 2.14 (dashed black line compared to solid black line). The QPC was then swept to zero gate bias, and kept at zero gate bias at T = 4.2K for an additional 24 hour period. Next, the QPC gate bias was again swept to obtain the conductance vs. gate voltage curve (blue line in Fig. 2.14). After being kept at zero bias for 24 hours, the conductance vs. gate voltage curve did not return to the original state before the drift occurred, but remained shifted and closely matched the curve *after* the drift occurred. This indicates that at T = 4.2K, the accumulated charge that contributes to the conductance drift is frozen; it does not relax after the gate bias is removed. Next, we warmed the QPC to a series of increasingly higher temperatures: 40K, 80K, and 140K. The QPC was kept at zero gate bias and held at each temperature for approximately 20 hours; immediately after this period, the QPC was cooled to T = 4.2K and its conductance vs. gate voltage characteristics were measured. After warming to 40K, the conductance vs. gate voltage curve shifted to more negative bias (dashed blue line), but did not return all the way to its original state before the drift occurred, indicating that a significant fraction, but not all, of the charge accumulated due to drift remained frozen in place at T=40K. After warming to 80K, the conductance curve (dashed red line) shifted to even more negative bias beyond the initial pre-drift curve. We take this as an indication that the majority of donor states that have trapped electrons in the vicinity of the QPC are now thermally depopulated. Warming to 140K resulted in a slight shift in the conductance vs. gate voltage curve (solid red line). We attribute the small difference in the initial gate sweep at 4.2K and the sweep after warming the sample to T=140K

to random rearrangement of donors states as is typically seen in the majority of QPCs upon thermal cycling to room temperature.

The fact that the charge accumulated in the drift process remains frozen at T = 4.2K after the gate bias is removed indicates that the donor state involved in conductance drift has a barrier to emission. The $DX^-$ donor state traps an electron and is known to have a barrier to emission; however, charge in $DX^-$ states remain frozen at temperatures below 100K [82, 83]. The fact that we observe partial thermal depopulation at 40K and full depopulations at 80K suggests that the state responsible for conductance drift is shallower than the $DX^-$ state. Evidence for a trap state associated with the Si donors with a smaller barrier to emission than the $DX^-$ state was reported in Ref. [88]; it is plausible that these states could be responsible for the drift we observe.

## 2.4 Summary and outlook

In summary, we unambiguously identified the total number of silicon donors as an important parameter influencing low frequency charge noise and conductance drift in modulation doped GaAs/AlGaAs heterostructures. Our data suggests that electron tunneling to available donor states, especially those in the neutral region, contributes to charge noise and device drift. The comparatively short time scale of the charge noise implies that it primarily involves shallow donor states, while the much longer time scale and the apparent freezing of the charge involved in drift suggests that the drift involves deep donor states. Modulation doped GaAs/AlGaAs heterostructures should be grown close to critical doping (that is, with a minimal neutral region in the doping layer) to minimize the number of charge trap sites available. We emphasize that wafers used for mesoscopic devices are frequently grown with a significant degree of overdoping (similar to Wafer B), so there is ample room for reducing charge noise by reducing the doping density. Using this guideline, devices with minimal charge

noise may be achieved that can serve as a robust, stable platform for spin-qubit based quantum computing.

The conduction band profile sketched in Fig. 2.8 is based on the assumption of sharp doping profiles which is not exactly true and it should be calculated taking into account the broadening of the doping profile. In reality, the doping profile is broadened by the migration of Si atoms toward the growing surface [20] and the broadening width is comparable to 15 nm undoped region near the surface. The migration of Si atoms could result in reducing the Schottky barrier and contribute to the increase of charge noise. In order to reduce the Si migration, the undoped region near the surface can be grown at low-temperatures to keep the Schottky barrier as thick as possible.

All the studied heterostructures for charge noise have 2DEG depth $\sim$ 90 nm , however structures with shallower 2DEG equal or less than 50 nm below the surface are desired for devices with small features. Growth of shallow 2DEG is challenging as it requires very large doping densities in order to satisfy surface charge states which consequently results in more charge noise. On the other hand, shallower 2DEG will suffer from low mobility as it is dominated by remote ionized scattering and surface states. One possible approach to tackle these issues is to grow wafers with highly doped GaAs cap layer to satisfy surface charge states and moderately dope at the setback to provide charges to the 2DEG. Since the cap layer is highly doped, the Schottky barrier thickness will reduce resulting in top gate current leakage. However, using a thin high-K dielectric under the gate can effectively reduce the current leakage and a stable device can be implemented on these shallow structures.

# 3. INDUCED SUPERCONDUCTING GAP IN HYBRID SUPERCONDUCTOR-SEMICONDUCTOR HETEROSTRUCTURES

## 3.1 Introduction

Starting about twenty years ago, people began to realize that the weird laws of quantum mechanics can be used to do computations that are impossible or impossible to do quickly on a classical computer. The best known example is the problem of finding the prime factors of a large composite integer. A quantum computer is used to perform such computations using fundamental components called qubit and there are a lot of different ways in which a qubit can be realized physically. A qubit can be encoded in an elementary particle like a photon or a single electron in quantum dot or in trapped ions and also in more complex systems like superconducting circuit involving the collective motion of many electrons. These conventional qubits encoded in some two-level systems are prone to dephasing and decoherence due to local noise sources such as charge noise (random electric fields) and spin noise (random magnetic fields). A trick to store the information in a way that noisy environment doesn't affect it is to use the entanglement and to store the information in a highly entangled state of multiple qubits. In other words, the information can be encoded in the nonlocal correlations among multiple qubits what has been called quantum-error-correction. Thus, quantum-error-correction scheme requires that a single fault-tolerant logical qubit to be encoded in many physical qubits which is a major source of overhead and the number of physical qubits needed for practical application grows up rapidly.

An alternative approach for quantum computing is suggested by Alexei Kitaev [89] who pointed out that topology can be utilized to make a quantum computer work. Topology is a word that mathematicians use to describe the properties of objects

which remain unchanged if the object is smoothly deformed without tearing it. In the case of doing a protected quantum computation it is desirable to do quantum processing with physical interactions that have topological properties to be immune against the local sources of noises. An example of a topological interaction is manifested in the Aharonov-Bohm effect for which the state of an electron transported around a magnetic flux tube remains invariant if the electron's trajectory is deformed. A more complex topological interaction occurs for particles in 2D systems called anyons. A system consisting of many anyons have huge number of distinct quantum states which locally all look the same. Looking at anyons one at a time doesn't tell about the quantum state of the system. In other words, the quantum information is spread out very non-locally and it is stored in a collective properties of many anyons. This information which is encoded in a highly non-local way can be processed by sequence of exchanges of the anyons in a fault-tolerant way and it is hard to be damaged by local environmental noise. One idea about the physical system in which anyons can be realized involves a suggestion made by Kitaev [89] who predicted that the induced superconducting correlation combined with spin-orbit coupling and an applied magnetic field can drive the 1D system into the topological superconducting (p-wave) state which supports charge-neutral zero energy modes (called Majorana zero modes) at the ends of 1D system. Majorana zero modes are new major addition to the universe of exotic quasi-particles in condensed matter systems which obey non-Abelian exchange statistics and can be utilized to build fault-tolerant quantum computers.

Majorana zero modes do not naturally exist but can be engineered by hybridization of semiconductor with large spin orbit coupling and a conventional s-wave superconductor. The first experimental signatures of Majorana zero modes in superconductor-semiconductor hybrid devices (NbTiN-InSb nanowire) were observed by Kouwenhoven group in Delft [90]. The signature of Majorana zero modes involves the appearance of zero-bias conductance peak (ZBCP) when the bulk gap closes and reopens at the transition from topologically trivial superconducting state to a non-trivial topological superconducting state. Figure 3.1 shows the appearance of ZBCP at finite

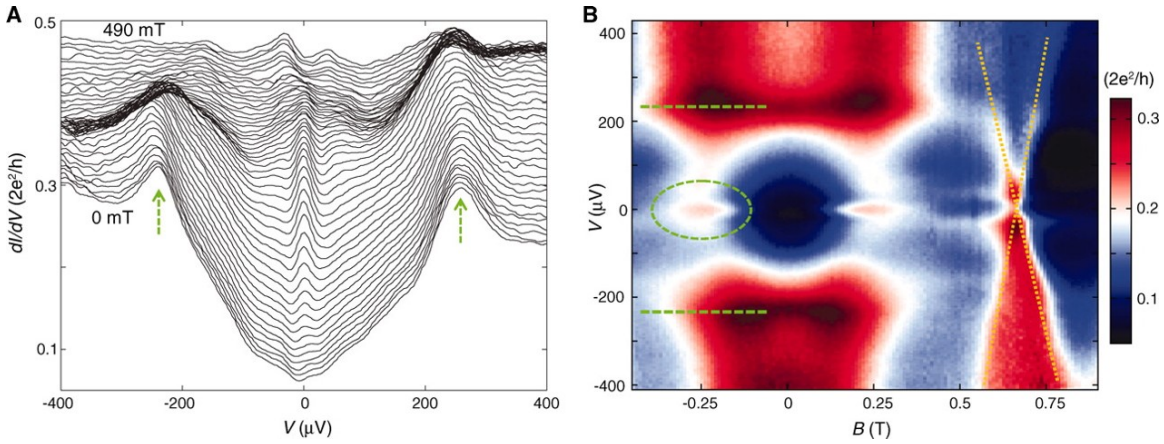


Fig. 3.1. (A) dI/dV versus V at 70 mK taken at different B fields. Arrows indicate the induced gap peaks. (B) Color-scale plot of dI/dV versus V and B. The ZBP is highlighted by a dashed oval; green dashed lines indicate the gap edges. From V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. A. M. Bakkers, and L. P. Kouwenhoven, Science 336, 10031007 (2012). Reprinted with permission from AAAS.

magnetic field (where the Zeeman splitting exceeds the gap) indicating that a normal electron tunnels directly into the end of superconducting wire at zero energy. At zero magnetic field, normal electron tunneling is prohibited indicating that there is no electron state available for tunneling. This was the first demonstration of Majorana fingerprint in hybrid semiconductor-superconductor devices and similar observation were made by Heiblum group at Weizmann Institute [91] in a different material system i.e. Al-InAs hybrid nanowire.

Since the observation of Majorana fingerprint, a great amount of attention was paid to improve the interface quality and inhomogeneity in the interface between the superconductor deposited on the semiconductor to induce superconducting pairing. Interface inhomogeneity is responsible for creating sub-gap states in the proximitized semiconductor [92] and can lead to poisoning of the Majorana zero modes and kill the topological protection by allowing excitations with arbitrarily small energy.

Growth of ultra-clean epitaxial Al-InAs hybrids with minimal interface defects and inhomogeneity was developed using state of the art MBE technique which has lead to promising reports of Majorana fingerprint in both 1D nanowire hybrids [93] and 2D superconductor-semiconductor hybrids with lithographically defined 1D superconducting wire [94]. Two-dimensional systems are of prime importance due to the possibility to easily scale up Majorana zero mode networks for practical realization of quantum computers. Lithographically defined SC wires on 2D platform studied so far [94, 95] require a relatively large magnetic field to trigger the topological phase transition. The strength of the Zeeman splitting necessary to trigger topological phase transition is characterized by the effective Lande factor $g^*$. If the effective g-factor is small, it will require a large magnetic field for the onset of topological phase transition. The effective g-factor of the SC wire studied in Ref. [94] is reported to be $\sim 4$ as determined via the linear dispersion of the Andreev bound state vs the magnetic field. The hybrid heterostructure utilized in this report consists of an InAs QW with an InGaAs barrier separating superconducting Al film from the 2DEG as shown in Fig. 3.2. The magnitude of InAs g-factor in the bulk is $\sim$15 and that of Al is $\sim$2. Comparing to the magnitude of bulk g-factor in InAs, the effective value of measured g-factor in hybrid heterostructure is substantially small. In this hybrid heterostructure the electronic wave-function of 2DEG in InAs has large weight in the superconductor, hence the effective g-factor reduces and becomes closer to that of Al. Low g-factor hybrid SC wire requires a larger magnetic field to produce Zeeman splitting larger than the SC gap which can potentially destroy the SC correlation before triggering topological transition. Hence, it is desirable to keep the magnetic field as low as possible because it also suppresses superconductivity and thus a large g-factor semiconductor is desired.

In order to increase the effective g-factor, an $Al_xIn_{1-x}As$ layer is utilized instead of $Ga_xIn_{1-x}As$ with larger conduction band offset with InAs to reduce the amount of hybridization between 2DEG(InAs) and SC(Al) wave-functions. Four wafers are grown with identical top barrier all with 15% Al content but different thicknesses

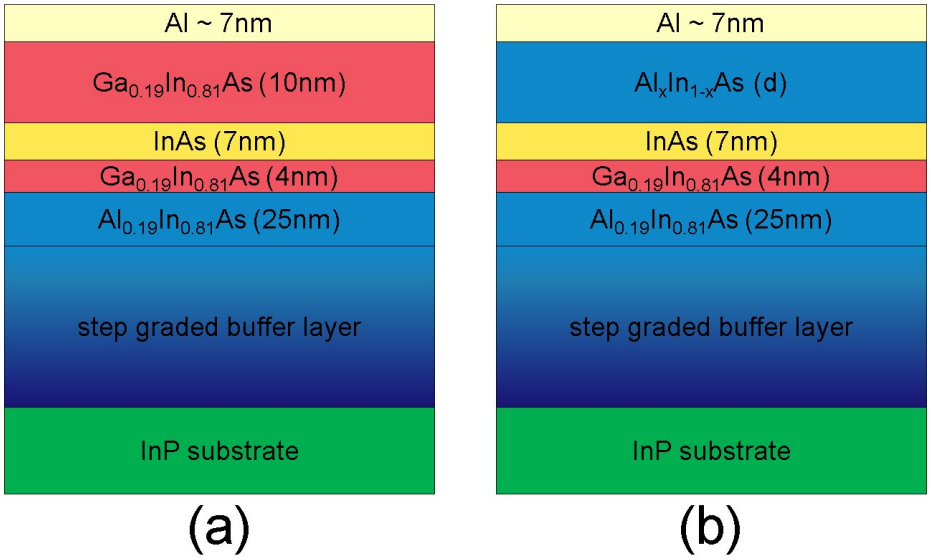


Fig. 3.2. a) 2D heterostructure used in Ref. [94] to create lithographically defined SC wire for observing Majorana zero modes. A 10nm $In_{0.81}Ga_{0.19}As$ barrier was used to separate 2DEG from the Al film. b) proposed heterostructure to control the amount of hybridization between electronic wave function in the semiconductor and the Al film using $Al_xIn_{1-x}As$ barrier with 15% Al content and thickness ranges from 3nm to 9nm

ranging from 3 nm to 9 nm. The induced SC gap are measured for grown wafers and its variation with the barrier thickness is compared with theoretical calculation from Santa Barbara Microsoft station Q team. This chapter is organized to demonstrate the growth of hybrid semiconductor-superconductor heterostructures, device fabrication and low temperature measurement of the induced gap and its variation vs the thickness of the barrier. Exhaustive information on physics of Majorana zero modes and their realization in hybrid superconductor-semiconductor materials can be found in well written thesis by Henri J. Suominen [96] and Morten Kjaergaard [97].

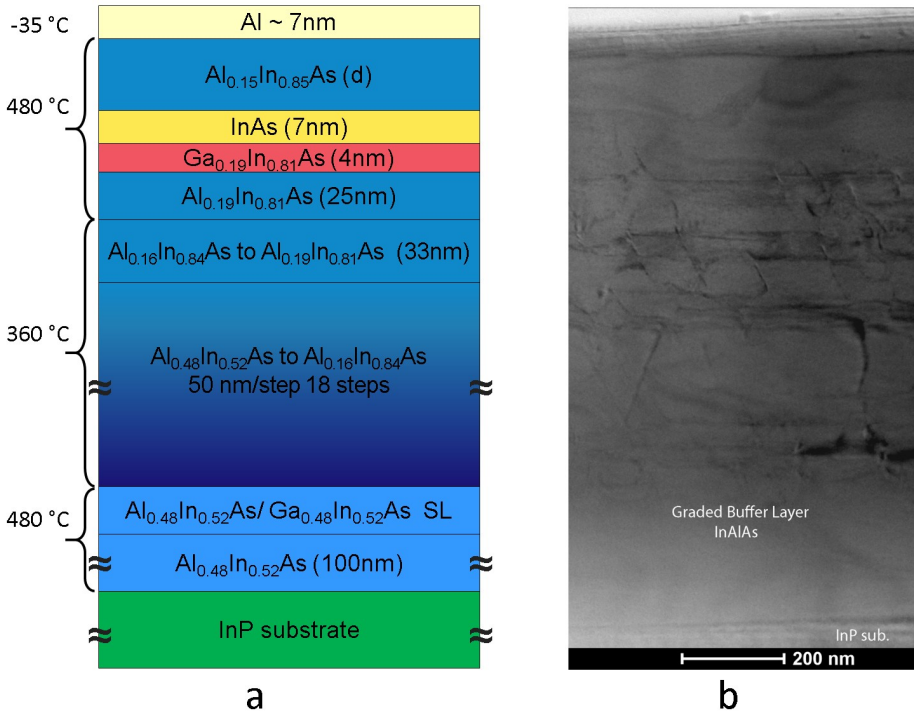


Fig. 3.3. a) Scheme of hybrid Al/$Al_{0.15}In_{0.85}As$/InAs layer sequence indicating the composition, thickness and growth temperature of each layer. b) Scanning transmission electron micrograph of a heterostructure with similar step-graded buffer region showing the misfit dislocations

## 3.2 MBE growth of hybrid Al/$Al_{0.15}In_{0.85}As$/InAs heterostructures

Hybrid Al/$Al_{0.15}In_{0.85}As$/InAs heterostructures are epitaxially grown on semi-insulating InP using Veeco Gen 930 MBE machine. Prior to epitaxial growth, the native oxides and carbons on InP substrate are thermally desorbed at 525 °C under moderate As pressure to prepare a clean and atomically ordered surface. This thermal desorption process at 525 °C continues until a $(4 \times 2)$ transition in RHEED pattern occurs. This is a transition in which the surface becomes metal (In) rich after desorbing the majority of native oxides.

A 100 nm thick $Al_{0.48}In_{0.52}As$ smoothing layer is grown at 480 °C which is lattice matched to InP substrate. Then, a short period superlattice of $Al_{0.48}In_{0.52}As$(2.5nm)

/ $Ga_{0.48}In_{0.52}As$(2.5nm) is grown to improve the smoothness of growth front and filter out the impurities originating from the substrate and block them from outdiffusion to the top most active region. Prior to the growth of InAs QW, a step-graded buffer layer is grown to compensate the lattice mismatch of 3.3% between InAs and the substrate. Growth of step-graded buffer layer of $Al_xIn_{1-x}As$ starts from x=0.48 to x=0.16 within 18 steps, 50nm for each, follows by linearly ramped steps from x=0.16 to x=0.19. Step graded buffer layer is grown at 360 °C and allow to control the misfit dislocations as they relieve the strain between the lattice mismatched layers. The active region is then grown at 480 °C which contains a 25 nm bottom barrier of $Al_{0.19}In_{0.81}As$, 4 nm $Ga_{0.19}In_{0.81}As$ layer, 7 nm strained InAs layer and top barrier $Al_{0.15}In_{0.85}As$ layer with thickness ranging from 3 nm to 9 nm separating the epitaxial Al film from InAs QW. 7 nm Al film was epitaxially grown at -35 °C. Figure 3.3 shows the layer stack for studied hybrid Al/$Al_{0.15}In_{0.85}As$/InAs heterostructures indicating the composition, thickness and growth temperature of each layer. Scanning transmission electron micrograph of the graded buffer region in similar heterostructure shows the misfit dislocations which drastically reduced at the end of graded buffer region.

### 3.3 Transport properties and gate response of 2DEG

In order to measure transport properties of the grown wafers, the Al film is striped first and a gated Hall bar is fabricated on the Al-striped wafers with a dielectric under the gates. The transport properties of grown wafers are measured at low temperature T = 10 mK using a standard lock-in technique. 2DEG density is extracted from low B-field (B $<$ 0.5T) dependence of Hall resistance, and it is repeated for different gate voltages. 2DEG depletion curves are plotted in Fig. 3.4a showing a linear dependence of 2DEG density vs gate bias voltage. The expected depletion point for the grown wafers is $\sim$ -0.5V (derived from simple geometric capacitance calculation) which is less negative than what has been observed experimentally and the depletion happens at more negative gate bias. A relatively linear and slow depletion of 2DEG

Table 3.1
Characteristics of studied wafers with different $Al_{0.15}In_{0.85}As$ barrier thickness ranging from 3 nm to 9 nm.

| Wafer Name | $Al_{0.15}In_{0.85}As$ thickness (nm) | $n_{peak}$ ($cm^{-2}$) | $\mu_{peak}$ ($cm^2/Vs$) | $V_{depletion}$ (V) |
|---|---|---|---|---|
| Wafer A | 3 | $1.2\times10^{12}$ | $27\times10^3$ | -1.0 |
| Wafer B | 5 | $1.5\times10^{12}$ | $31\times10^3$ | -0.7 |
| Wafer C | 7 | $1.0\times10^{12}$ | $67\times10^3$ | -0.8 |
| Wafer D | 9 | $1.0\times10^{12}$ | $125\times10^3$ | -1.1 |

density vs gate voltage indicates the existence of uniform density of interface states between dielectric and the semiconductor but it could be reduced by passivation of the semiconductor surface before dielectric deposition. Except wafer B, the zero gate bias 2DEG density decreases by increasing the thickness of $Al_{0.15}In_{0.85}As$ top barrier. This is expected behaviour since the charge transfer from surface to InAs QW decreases by increasing the thickness of the barrier. However, the reduction in zero bias 2DEG density does not follow the 1/d dependence for charge transfer and this could be due to the different fixed charges in the interface between the dielectric and semiconductor surface for each processed wafer.

The mobility vs 2DEG density is plotted in Fig. 3.4b showing a non-monotonic behaviour for all wafers. Starting at low density, the mobility increases first and after reaching its maximum mobility at $n \sim 1 \times 10^{12} cm^{-2}$(Wafer B is an exception) the mobility decreases. This 2DEG density at the peak mobility corresponds to the density at which the second sub-band of the quantum well has been populated. Table 3.1 shows transport characteristics of studied wafers with different $Al_{0.15}In_{0.85}As$ barrier thickness ranging from 3 nm to 9 nm. Wafers A and B with 3 nm and 5 nm barrier have more or less identical mobility, but the mobility increases for wafers with barrier thicker than 5nm barrier. This indicates the the mobility is strongly limited by the surface scattering for wafers with barriers below 5 nm.

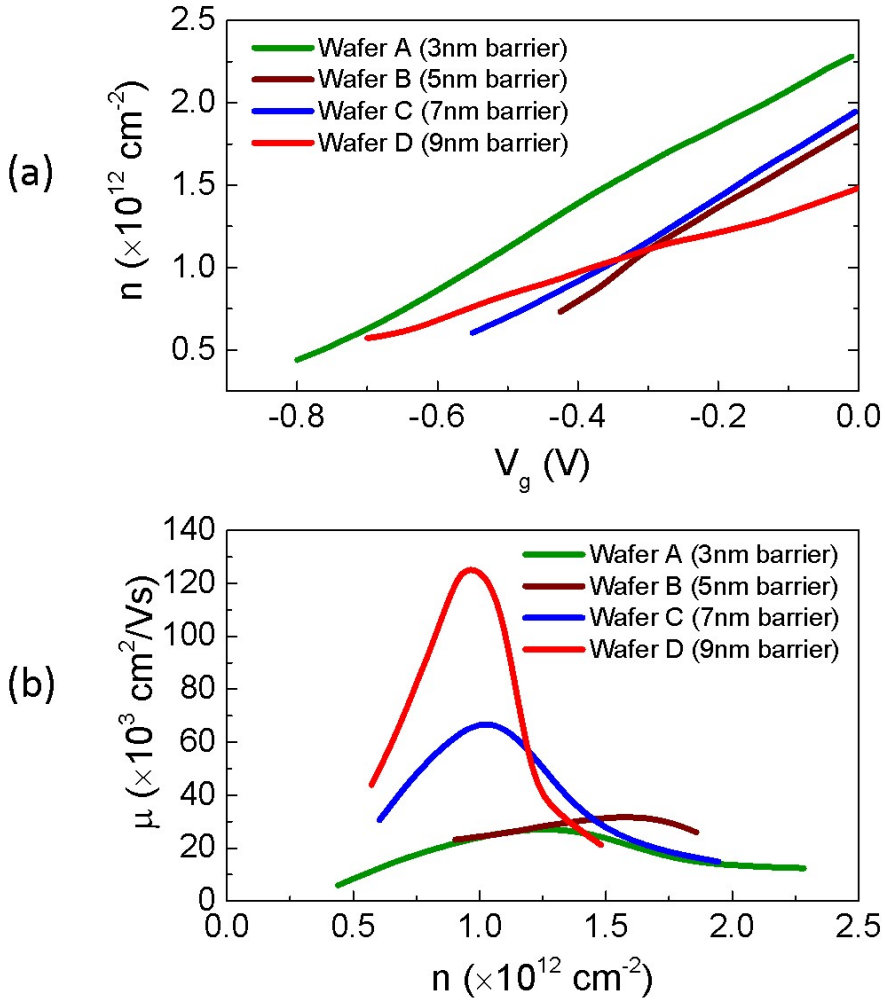


Fig. 3.4. a) Gate voltage dependence of 2DEG density in InAs QW for wafers with $Al_{0.15}In_{0.85}As$ barrier thickness ranging from 3 nm to 9 nm. b) mobility vs 2DEG density for fabricated Hall bars

### 3.4 Measurement of the induced superconducting gap

Two distinct devices namely Superconductor-Normal-Superconductor (SNS) junctions and S-QPC-N junctions are utilized to measure and extract the induced superconducting gap for grown hybrid superconductor-semiconductor heterostructures. From multiple Andreev reflections (MAR) in SNS junctions, the amount of induced gap is determined from the position of sub-harmonic gap structures in the the current-

voltage characteristics of the SNS junctions. Andreev reflection is a process in which an electron coming from normal region is reflected as a hole in an SN interface and a Cooper pair travels to the superconducting region. The physics of multiple Andreev reflections was introduced by Klapwijk, Blonder, and Tinkham [98] and then extended to include the effect of barrier in the SN interface [99,100] (OTBK theory). In an SNS junction transport at finite bias V, successive Andreev reflections occur at both superconducting electrodes and during every passage across the junction, the electrons and the reteroreflected holes acquire additional energy equal to eV. This process continues until the quasiparticle energy exceeds the superconducting energy gap and results in formation of sub-harmonic energy gap structures which is often observed as a series of differential conductance peaks at finite bias voltages. For highly transparent junctions the sub-harmonic gaps appear in conductance dips rather than conductance peaks [101]. Extraction of the induced superconducting gap from subharminc features is an indirect approach and sometimes it mixes with the conductance peaks from the pristine Al making it an inaccurate tool for estimation of SC induced gap in 2DEG. On the other hand, tunneling measurements in S-QPC-N device directly probe the density of states (DOS) in the proximitized 2DEG and it gives an accurate estimation of the induced superconducting gap. The measurement results for SNS and S-QPC-N junctions are given in the following sections. There are very useful thesis on this subject from Charlie Marcus group in Copenhagen University with a detailed information on the physics and operation of these junctions [96,97]

**SNS junctions**

Figure 3.5a shows the false-color scanning electron micrograph of a gated SNS junction where the density of charge carriers in the normal region can be tuned by the top gate bias. Normal region is 2DEG within InAs QW which is not covered with Al. Due to the proximity effect, the part of QW covered by Al become superconducting with gap $\Delta^*$ and Andreev reflections happen at interface between the covered

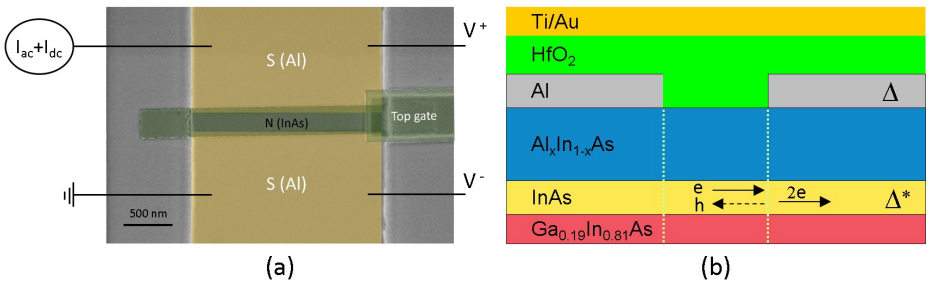


Fig. 3.5. a) False-color scanning electron micrograph of the S-N-S junction where the normal region is 2DEG in within InAs QW. b) Cross sectional schematic of the SNS device in . Due to the proximity effect, the part of QW covered by Al become superconducting with gap $\Delta^*$. Andreev reflections happen at interface between the covered and Al stripped regions.

and Al stripped regions as shown in Fig. 3.5b by dotted vertical lines. The electrons and the retroreflective holes gain additional energy equal to eV (i.e. V is the voltage drop across the junction). This process continues until the quasiparticle energy exceeds the superconducting energy gap and allows them to eventually escape into one of the reservoir. The multiple Andreev reflections create strongly non-equilibrium quasiparticle distribution in the contact area and give rise to discrete energy levels or resonances in the energy gap manifested as peaks in the differential conductance at discrete voltage bias across the junction. The conductance peaks are expected to follow the series $eV = 2\Delta^*/n$ (i.e. n = 1, 2, 3, ... is the number of Andreev reflections) from which the induced superconducting gap $\Delta^*$ can be extracted.

All measurements were performed in a dilution refrigerator with base temperature T ∼10 mK using current bias measurement setup as shown in Fig. 3.5. Standard lockin techniques with 5 nA AC current excitation at 83Hz are used to measure the differential resistance. DC voltage drop across the SNS junctions are measured using a DL voltage pre-amplifier with gain 1000. The differential resistance for SNS junction fabricated on Wafer B (with 5nm AlInAs top barrier) is shown Figure 3.6. Multiple Andreev reflections manifested as minima in differential resistance curve (blue color)

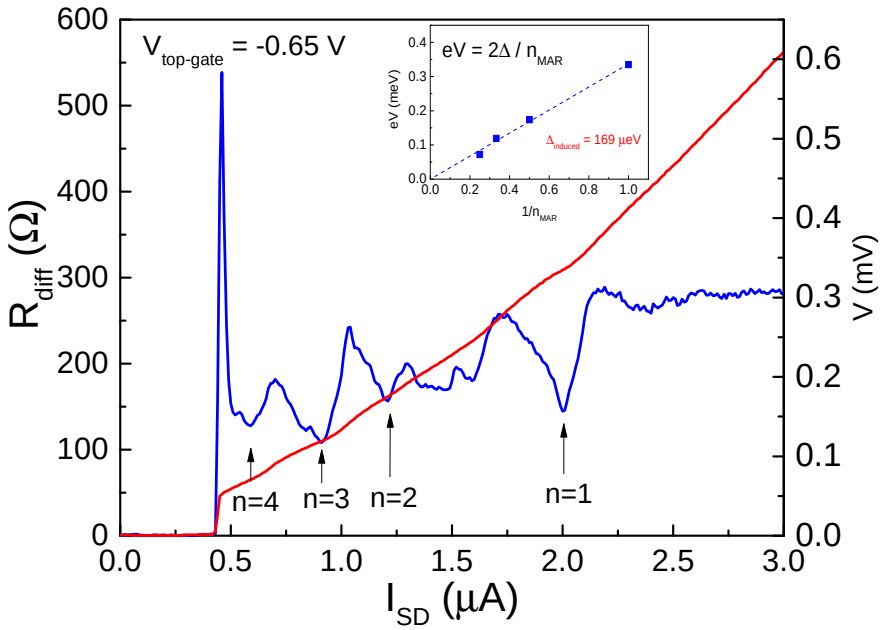


Fig. 3.6. The Differential resistance and DC component of the voltage drop across the SNS junction.Multiple Andreev reflections (MAR) corresponding to the induced gap $\Delta^*$ are shown. The inset shows a linear fit to the MAR resonances from which the induced gap $\Delta^*$ is extracted.

and indicated by arrows corresponding to the number of Andreev reflections. The inset in Fig. 3.6 shows a linear fit to the MAR resonances from which the induced gap $\Delta^*$ is extracted. There are also some unlabeled dips/peaks which are related to the pristine Al gap. In fact, the presence of two gaps in the density of states $\Delta$ and $\Delta^*$, results in addition of a new set of MAR resonances at $2\Delta/n$,$(\Delta - \Delta^*)/n$, $(\Delta + \Delta^*)/n$ [102, 103].

Similar measurement protocol for SNS junction is repeated for all the grown wafers with different barrier thickness and the extracted induced gap are listed in Table 3.2

### Tunneling spectroscopy of S-QPC-N devices

Properties of the induced superconductivity in InAs QW and its variation vs the barrier thickness are studied using S-QPC-N devices. Transport measurement across

Table 3.2
Induced gap vs barrier thickness extracted from SNS device measurement at 10 mK

| Wafer Name | $Al_{0.15}In_{0.85}As$ thickness | $\Delta^*$ |
|---|---|---|
| Wafer A | 3 nm | 200 $\mu eV$ |
| Wafer B | 5 nm | 155 $\mu eV$ |
| Wafer C | 7 nm | not measured |
| Wafer D | 9 nm | 25 $\mu eV$ |

a single SN interface in tunneling regime is performed to directly probe the BCS-like density of states in the proximitized 2DEG from which the induced gap can be extracted. A false-color scanning electron micrograph of the SN interface with a QPC in the middle (S-QPC-N) is shown in Fig. 3.7. By depleting the QPC to the tunneling regime $G_{QPC} << 2e^2/h$ (very weakly coupled regime) the differential conductance measurement across the QPC maps out the local density of states in the hybrid $Al/Al_{0.15}In_{0.85}As/InAs$ heterostructure. A voltage bias measurement scheme is used in the tunneling regime and the current through the QPC is directly measured using DL current pre-amplifier as shown in Fig. 3.7b. Inside the voltage adder, voltage division of $10^5$ and $10^{-3}$ was used for ac and dc respectively. Figure 3.7c shows the depletion curve and pinch-off voltage for Wafer A with 3 nm $Al_{0.15}In_{0.85}As$ top barrier. The inset shows the finite bias tunneling conductance vs source-drain dc voltage from which the induced gap is determined.

The same measurement technique is applied for all the grown wafers to obtain tunneling conductance vs the source-drain bias. Figure 3.8 shows the finite bias spectroscopy to obtain the induced gap for heterostructure with different barrier thickness 3 nm (Wafer A), 5 nm (Wafer B), 7 nm (Wafer C) and 7 nm (Wafer D). The BCS-like coherence peaks and hard gap are observed for all the wafers. The induced gap reduces by increasing the $Al_{0.15}In_{0.85}As$ top barrier, however the gap hardness does

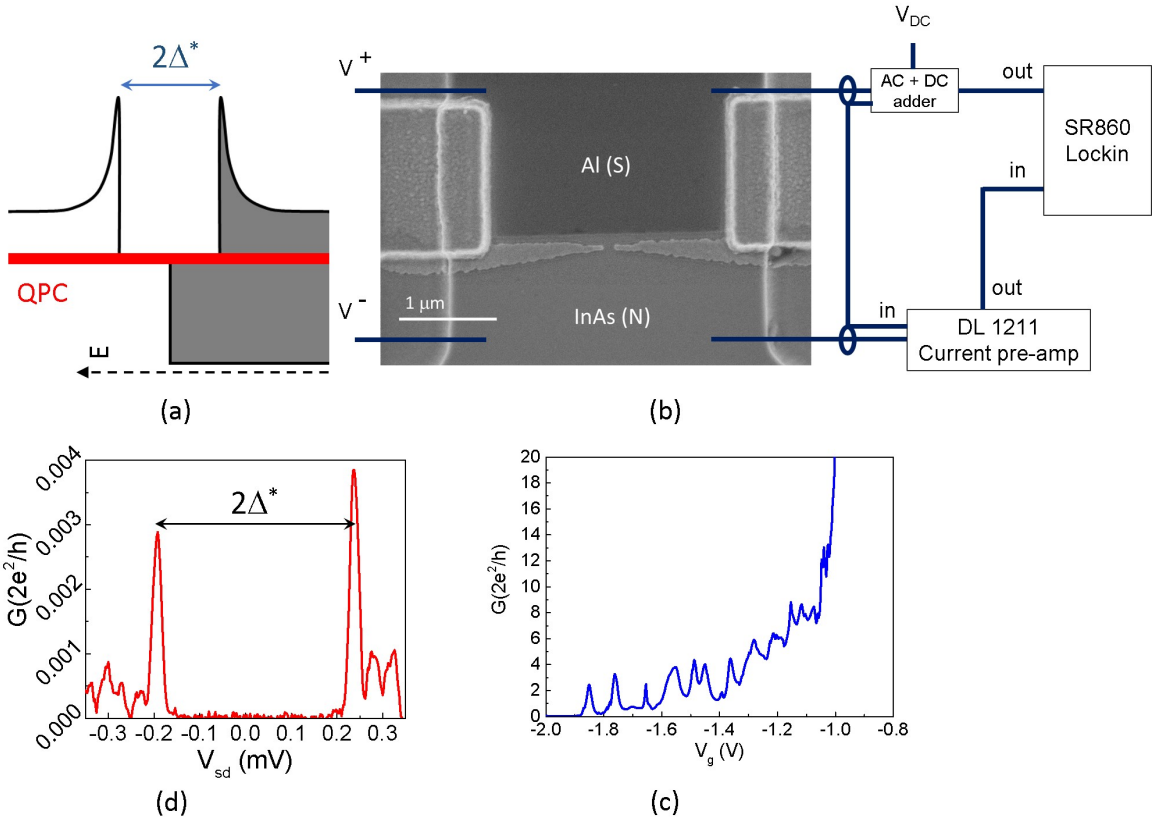


Fig. 3.7. a) Schematic of local density of states in the normal metal an superconductor. b) False-colored scanning electron micrograph of the S-QPC-N device, showing the measurement configuration. The normal metal is 2DEG located in the InAs QW and superconducting part is the proximitized 2DEG by Al thin film which is superconducting with induced gap $\Delta^*$. QPC is used to tune the NS interface into the tunneling regime with $G_{QPC} << 2e^2/h$. c) 2DEG depletion curve and QPC pinch off. d) Differential conductance in the tunneling regime.

not change significantly in spite of reduction in the degree of hybridization between Al and 2DEG.

Figure 3.10 shows the comparison of experimental data for the induced gap with the simulated induced gap (unpublished result by G. W. Winkler and his colleagues in Microsoft Quantum - Santa Barbara Station Q [104]). The simulation for induced gap has a decent agreement with the experiment The important parameter in the

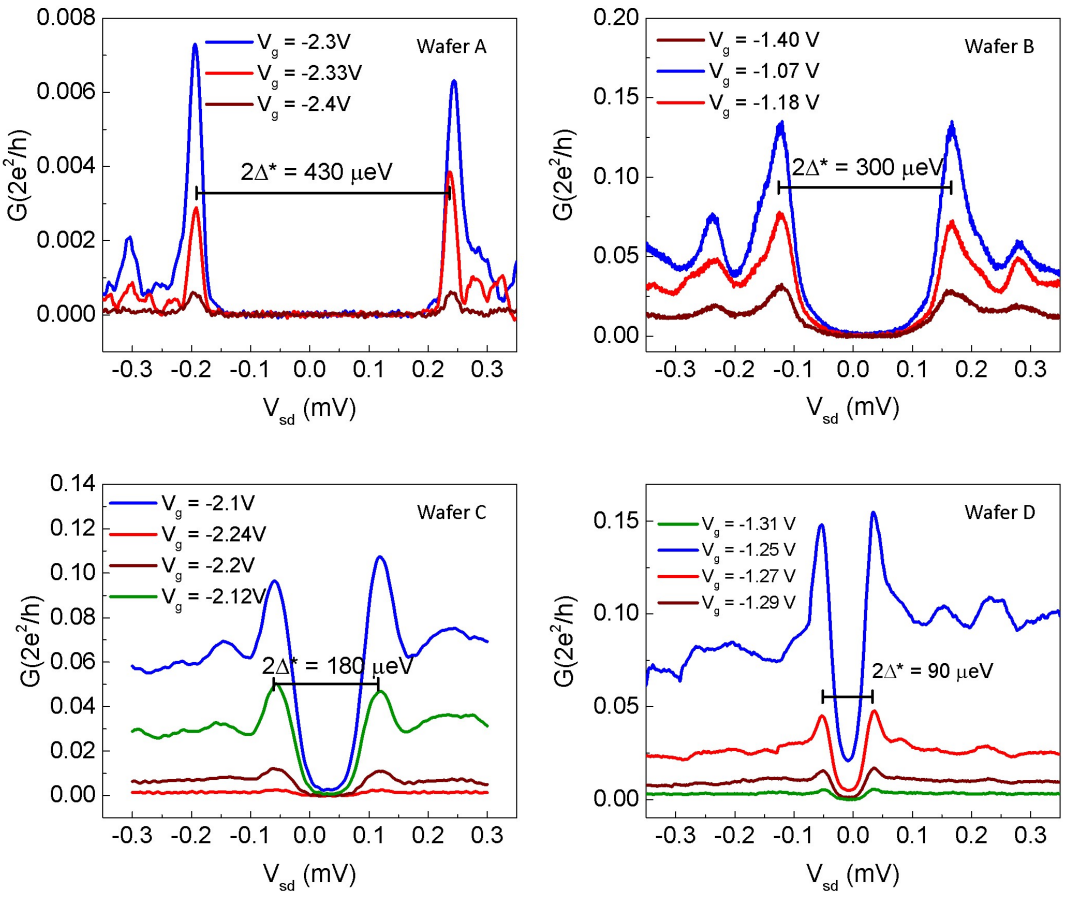


Fig. 3.8. Finite bias spectroscopy showing BCS-like coherence peaks for heterostructure with different barrier thickness 3 nm (Wafer A), 5 nm (Wafer B), 7 nm (Wafer C) and 7 nm (Wafer D).

simulation is the conduction band offset at the surface of $Al_{0.15}In_{0.85}As$ barrier which determines the leakage of Al SC wave function into the semiconductor region. There is a little bit discussion on the error bars in the experimental data. The uncertainty in measuring the induced gap could come from the statistics of various device measurements as the measured gap varies for devices fabricated on different portions of the wafer. There is not enough data-points for different devices to obtain the uncertainty in the measured gap. Another and the most important source of uncertainty in the

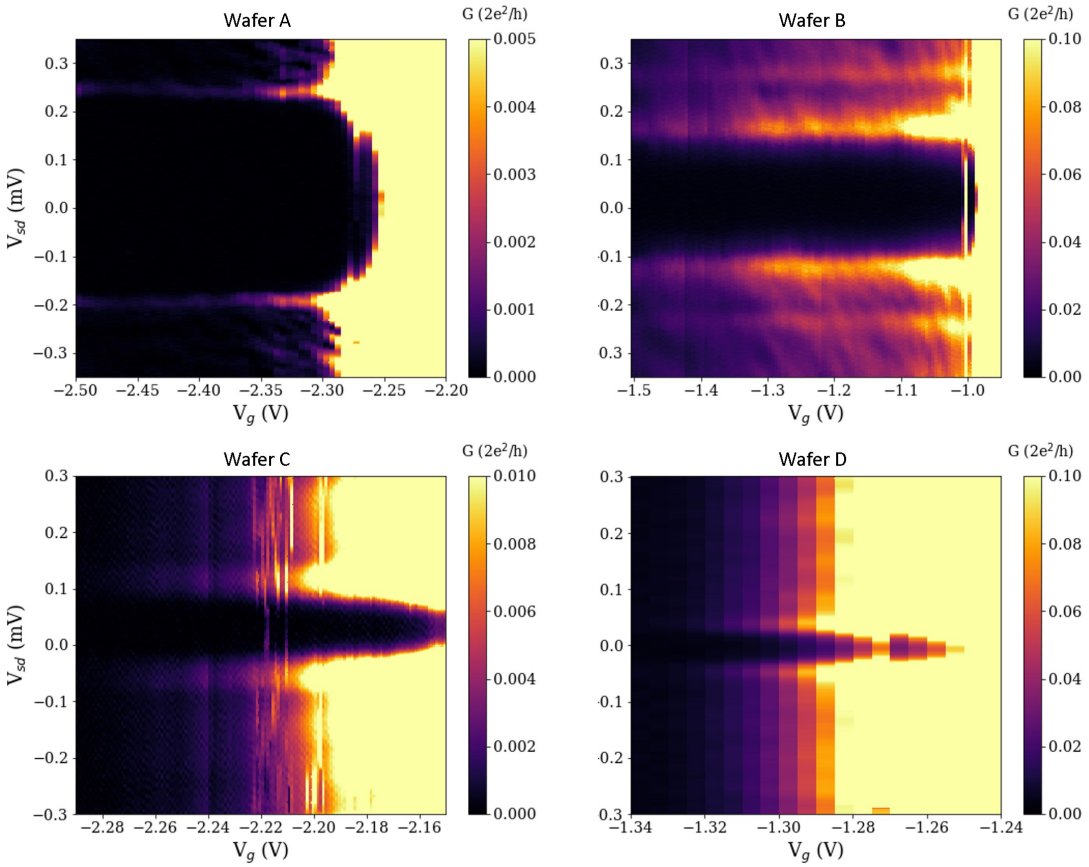


Fig. 3.9. 2D tunneling conductance as a function of QPC gate voltage and source-rain bias. The BCS-like coherence peaks survived at more negative QPC gate bias.

the measured gap comes from the variation in the barrier thickness which could be 1ML (0.3 nm) corresponds to 8 $\mu eV$ which set the upper limit for the error bars in the measured induced gaps.

The next step is to find the effective g-factor for the studied wafers. The aim is to find a wafer with highest possible effective g-factor which shows a hard induced gap at the same time. These two factors are antagonistic since wafer with very large g-factor in the InAs haterostructures requires a minimal overlap with the superconducting wave-function of the Al film leading to normal state in the 2DEG. We are searching

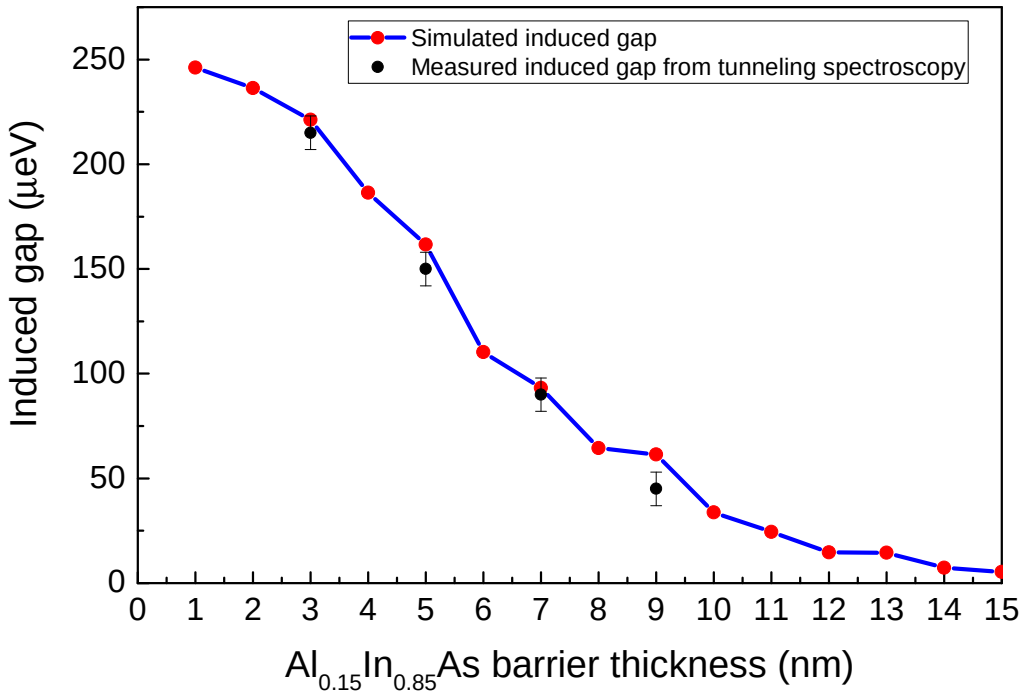


Fig. 3.10. Measured and simulated induced gap dependence vs $Al_{0.15}In_{0.85}As$ top barrier thickness.

for an optimum overlap using $Al_{0.15}In_{0.85}As$ top barrier to control the amount of this overlap to realize a SC proximitized 2DEG possessing a high g-factor.

The effective g-factor defines as the rate of linear decrease of Andreev bound states energy as a function of applied magnetic field. The effective g-factor for hybrid InAs nano wires has been previously measured and its variation vs the back-gate (to tune the level of hybridization between electrons in InAs and the superconducting Al) is reported in Ref. [105]. Similar method can be utilized in 2D hybrid heterostructures but in a lithographically defined SC wire as shown in Fig. 3.11 . The Zeeman splitting of the Andreev bound states can be derived by measuring the differential conductance of the normal electrons to the SC wire as a function of source-drain

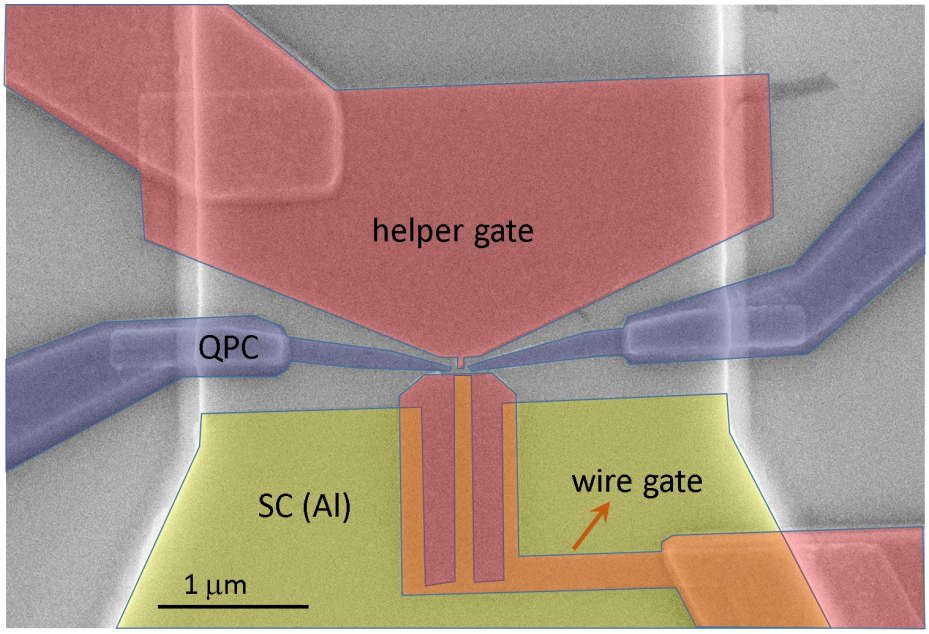


Fig. 3.11. Lithographically defined SC wire to measure the effective g-factor. QPC are used to tune the conductance into the tunneling regime and helper gate is utilized to fine tune the potential landscape around the QPC. Wire gate is used to deplete the 2DEG in the normal region such that the SC wire becomes isolated.

bias and the applied magnetic field along the wire. This is an ongoing project to be accomplished by other graduated student.

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