TRANSITION METAL DICHALCOGENIDE BASED MEMORY DEVICES AND TRANSISTORS

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To my beloved parents

Xiaogong Zhang **and** ***Ruixiang Zhang***

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ABSTRACT

Zhang, Feng Ph.D., Purdue University, August 2019. Transition Metal Dichalcogenide Based Memory Devices and Transistors. Major Professor: Joerg A. Professor.

Silicon based semiconductor technology is facing more and more challenges to continue the Moore's law due to its fundamental scaling limitations. To continue the pace of progress of device performance for both logic and memory devices, researchers are exploring new low-dimensional materials, e.g. nanowire, nanotube, graphene and hexagonal boron nitride. Transition metal dichalcogenides (TMDs) are attracted considerable attention due their atomically thin nature and proper bandgap at the initial study. Recently, more and more interesting properties are found in these materials, which will bring out more potential usefulness for electronic applications. Competing with the silicon device performance is not the only goal in the potential path finding of beyond silicon. Low-dimensional materials may have other outstanding performances as an alternative materials in many application realms.

This thesis explores the potential of TMD based devices in memory and logic applications. For the memory application, TMD based vertical devices are fully studied. Two-terminal vertical transition metal dichalcogenide (TMD) based memory selectors were firstly built and characterized, exhibiting better overall performance compared with some traditional selectors. Polymorphism is one of unique properties in TMD materials. 2D phase engineering in TMDs attracted great attention. While electric switching between semiconductor phase to metallic phase is the most desirable. In this thesis, electric field induced structural transition in $MoTe_2$ and $Mo_{1-x}W_xTe_2$ is firstly presented. Reproducible bipolar resistive random access (RRAM) behavior is observed in $MoTe_2$ and $Mo_{1-x}W_xTe_2$ based vertical devices. Direct confirmation of a phase transition from a 2H semiconductor to a distorted $2H_d$ metallic phase was

obtained after applying an electric field. Set voltage is changed with flake thickness, and switching speed is less than 5 ns. Different from conventional RRAM devices based on ionic migration, the $MoTe_2$-based RRAMs offer intrinsically better reliability and control. In comparison to phase change memory (PCM)-based devices that operate based on a change between an amorphous and a crystalline structure, our $MoTe_2$-based RRAM devices allow faster switching due to a transition between two crystalline states. Moreover, utilization of atomically thin 2D materials allows for aggressive scaling and high-performance flexible electronics applications. Both of the studies shine lights on the new application in the memory field with two-dimensional materials.

For the logic application, the ultra thin body nature of TMDs allows for more aggressive scaling compared with bulk material - silicon. Two aspects of scaling properties in TMD based devices are discussed, channel length scaling and channel width scaling. A tunability of short channel effects in MoS_2 field effect transistor (FET) is reported. The electrical performance of MoS_2 flakes is governed by an unexpected dependence on the effective body thickness of the device which in turn depends on the amount of intercalated water molecules that exist in the layered structure. In particular, we observe that the doping stage of a MoS_2 FET strongly depends on the environment (air/vacuum). For the channel width scaling, the impact of edge states in three types of TMDs, metallic T_d-phase WTe_2 as well as semiconducting 2H-phase $MoTe_2$ and MoS_2 were explored, by patterning thin flakes into ribbons with varying channel widths. No obvious charge depletion at the edges is observed for any of these three materials, which is different from what has been observed in graphene nanoribbon devices.

1. INTRODUCTION

Transition metal dichalcogenides (TMDs) have attracted great attention as potential building blocks for various electronic applications, e.g. logic devices [1,2], flexible electronics [3–5] and optoelectronics [6], due to their atomically thin nature and physical properties [7]. What application realm will be the most suitable for these novel classes of materials? There is no single answer. Low-dimensional materials offer the unique properties to open a door for the discovery of novel electronic applications. Two-dimensional (2D) materials have in-plane and out-of-plane direction. The significant different lattice arrangements in these two directions further impact the physical properties. Therefore, the vertical transport study in TMDs is equally important compared to the lateral transport. We have studied the vertical charge transport through TMDs and built a model to theoretically analyze the current [8]. Moreover, TMDs exist in various crystalline phases which exhibit semiconducting, semimetallic and metallic properties. Since for some TMD compounds the energetic difference between the various phases is rather moderate [9, 10], if we can electrically control the different semiconducting and metallic phases, TMDs can be a good switching material for memory application. In this thesis, TMD based vertical devices show great potential in the memory application as selectors and RRAM devices.

1.1 TMD based memory devices

Innovation in modern storage applications is intimately connected with the development of the entire field of modern information technology. Denser, faster and less power consuming memories are highly sought after by the industry. Flash shows in this context excellent performance specs for nonvolatile memory applications, benefiting from Moore's Law improvements in cost per bit [11, 12]. Moreover, three-

dimensional (3D) vertical NAND flash promises even further density improvements compared to current planar NAND technologies [13]. However, flash also faces its own set of issues related to the reliability of operation, due to the small amount of charges involved in the storage process, where the loss of just a few electrons can result in vastly different device performance specs. Consequently, the bit error rate (BER) has been increasing with shrinking device dimensions from one to the next technology node, posing a severe challenge for future applications [14–16].

On the other hand, resistive random access memory (RRAM) occurs promising as an emerging technology due to its potential scalability, high operation speed, high endurance and ease of process flow [17, 18]. Moreover, the possibility of creating 3D stacked RRAM structures makes this technology even more appealing [19, 20]. Here we will discuss a novel RRAM cell that utilizes for the first time ultra-thin transition metal dichalcogenide (TMD) layers as the active layer in a one resistor (1R) configuration. RRAM devices are typically two-terminal structures whose operation are based on changing the resistive state of the element to store information in a nonvolatile fashion by applying a sufficiently high voltage or by driving a large enough current through it. Many different metal oxides such as NiO [21], TiO_x [22], HfO_x [23] have been studied as switching materials. RRAM occurs promising as an emerging technology due to its potential scalability, high operation speed, high endurance and ease of process flow.

Typically two types of switching mechanisms are distinguished in RRAM devices. In the valence change memory (VCM), the electromigration of induced anions modifies the valence states of the cations. For example, the memresistive switching behavior in NiO is due to the drift of oxygen vacancies forming a conductive path under an external electric field [24]. TiO_2 based RRAM switching on the other hand occurs through the formation and disruption of a conductive Magnli phase Ti_nO_{2n-1} [25]. On the other hand, RRAM devices operating based on the electrochemical metallization rely on the anodic dissolution (oxidation) of an active metal electrode (e.g. Ag [26] or,

Cu [27]) and electrodeposition (reduction) of the metal ions inside the active switching material.

All the observed RRAM behavior involves the uncontrollable movement of individual atoms. The reliability is a big challenge in the future applications. Therefore, there is a need in the art for a new switching mechanism for fabricating RRAM devices.

Recently, a number of research groups have started to explore 2D materials for RRAM applications. The advantage of these materials lies potentially in their atomically thin nature that may enable a tunable range of small operation voltages and allows for 3D integration if combined with quasi-metallic graphene layers as electrodes [28]. In this work, electric field induced structure transition from the semiconducting 2H phase to a more conductive state $2H_d$ (a distorted 2H state) is observed in vertical $MoTe_2$ devices. It shows stable and reproducible RRAM behavior. The set and reset voltages are tuned by the flake thickness. The switching speed can be less than 5 ns. The adjustment ability of operation voltage and its atomic thin nature make it appealing in the real application. Moreover, the switching mechanism may provide a potential solution to resolve the reliability issue in the conventional RRAM devices.

Besides the $MoTe_2$ based RRAM devices are characterized, TMD based RRAM selectors have also been studied. In the real RRAM crossbar array, a selector is usually in series with RRAM device in each cell. A selector has three important factors: i) small resistance at V_{DD}, which will not reduce the on-state performance of RRAM, ii) large resistance at 1/2 V_{DD} or 1/3 V_{DD}, suppressing the leakage current, and iii) bidirectional operation. The atomic thin nature of the TMDs allows for the achievement of high current, while the Schottky barriers formed between contact metals and TMD materials benefit the non-linearity at the half voltage. The novel two-terminal memory devices based on TMD materials are shown in Chapters 2, 3 & 4. I experimentally demonstrated for the first time a novel two-terminal vertical transition metal dichalcogenide (TMD) based memory selectors and $MoTe_2$ based

RRAM. The initial studies on the TMD based memory devices open a door to explore the novel application with 2D materials.

1.2 TMD based transistors

Device scaling from one to the next technology node is becoming more and more challenging. To continue the Moore's law, 2D materials attract great attention due to their ultra-thin body nature compared to bulk material silicon. Transition metal dichalcogenides gain intense interests due to their physical properties. To explore the possibilities of TMDs as an option material to continue the Moore's law, channel length scaling and channel width scaling were studied in this work. In Chapter 5, the tunability of short-channel-effects in MoS_2 field effect transistors were explored, and provided the first time experimental evidence of a change in the two-dimensional electrostatics in MoS_2 FETs as a function of the device environment. In Chapter 6, the impact of channel width scaling on the transport in three TMD materials, semimetallic T_d-phase WTe_2 and semiconducting 2H-phase $MoTe_2$ and MoS_2 were studied. No obvious depletion region was identified for channel widths down to 25 nm, which is different from graphene nanoribbon devices.

2. TRANSITION METAL DICHALCOGENIDE BASED MEMORY SELECTORS

Novel two-terminal vertical transition metal dichalcogenide (TMD) based memory selectors were experimentally demonstrated for the first time. They exhibit better overall performance compared with some traditional selectors, and the ultra atomic thin nature makes them even appealing in the real application.

2.1 Introduction

In the real application, resistive random access memory (RRAM) is built as cross-point array. For the $V/2$ write scheme, to select a device, the word line (WL) is set to V, and the bit line (BL) is set to $V/2$. The other word lines and bit lines are set to $V/2$. As it is shown in Fig. 2.1. Besides the selected cell, there will be sneak current passing through the other unselected cells, resulting in large power consumption. Therefore, selector devices play an important role to ensure that an individual memory element can be properly addressed through reading and writing while at the same time the information stored in the other cells of the same array does not get perturbed and power does not get wasted by undesirable leakage through unselected cells. Fig. 2.2 implies the current differences of the RRAM device with and without the selector. From Fig. 2.2(b), the current at $V/2$ gets highly suppressed, while the current at V does not affect too much.

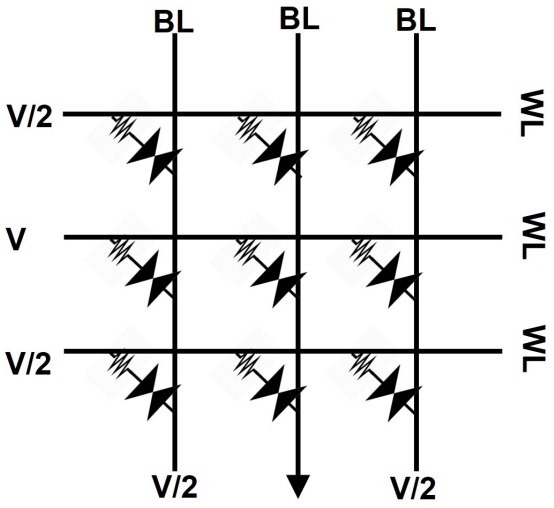


Fig. 2.1. Cross-point array $V/2$ write operation implies the sneak current paths.

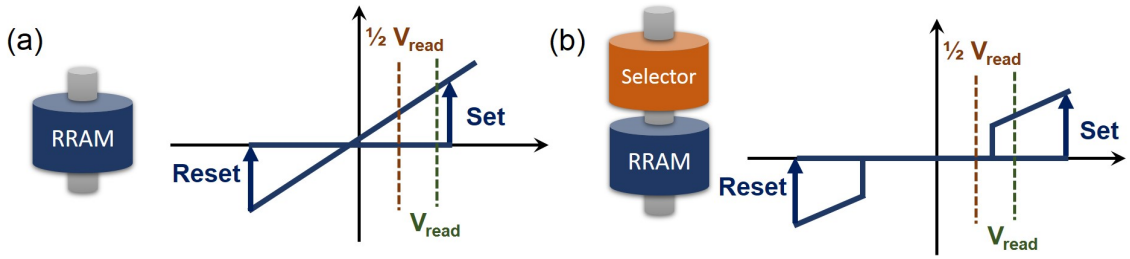


Fig. 2.2. RRAM current curves with (a) and without (b) selector.

An ideal selector device has to fulfill many criteria simultaneously such as: i) it has to support high on-state current density (10^7 A/cm^2), ii) it has to exhibit a large nonlinearity at half bias $NL_{1/2}$, iii) it should be capable of bidirectional operation, and iv) it should be back-end-of-the-line (BEOL) compatible [30]. Moreover, its operation voltage needs to be compatible with the memory element. In the context of the above two-terminal devices are desirable for ease of integration, and silicon based diodes, oxide pn-junction diodes and threshold voltage switches, such as metal-insulator-transition (MIT), are candidates that have been explore. However, all of

these three types of selector devices suffer from serious drawbacks. For example, two-terminal NPN silicon diodes do not conform to high-density, nonvolatile memories with 3D stack structures due to their high processing temperature between 700°C and 1000°C and the difficulty of growing high-quality epitaxial silicon over metals. Although amorphous silicon can eliminate the need for a single-crystal silicon seed and allows for low processing temperatures of around 800°C, it does not provide the required semiconducting performance. Oxide-based access devices on the other hand can be processed at low temperatures but do not reach the desired on-current levels, while MIT-based selectors cannot provide the desired $NL_{1/2}$. This makes developing novel types of selectors and ultimately a cell highly desirable.

2.2 Transition metal dichalcogenide based selectors

Based on previous study on the vertical transport in TMD devcies, there are mainly three current components, thermal difussion current, Fowler-Nordheim tunneling current and direct tunneling current [8]. The tunneling current in the vertical structure will produce the non-linearity, and the ultra-thin property in TMD will allow to achieve high on-state current. We experimentally demonstrate for the first time a novel two-terminal vertical transition metal dichalcogenide (TMD) based memory selector. It exhibits better overall performance compared with above mentioned two terminal selector candidates and shows the highest vertical current density in TMDs reported so far.A typical device design and an optical and SEM images are shown in Fig. 2.3. First a layer of Ti/Au (10 nm/25 nm) which acts as a bottom electrode was deposited onto a 90nm silicon dioxide (SiO_2) layer located on top of a highly doped silicon wafer. Next, TMD flakes from either (i) WSe_2 (HQ Graphene), (ii) MoS_2 (SPI Supplies), or (iii) $MoTe_2$ (2D Semiconductors) were exfoliated onto this electrode using standard scotch tape techniques, followed by a thermal evaporation of 55 nm SiO_2 acting as an insulating layer. The device fabrication was finished by

the definition of a Ni (85 nm) top electrode. As noted above a selector should fulfill all of the criteria i) through iv).

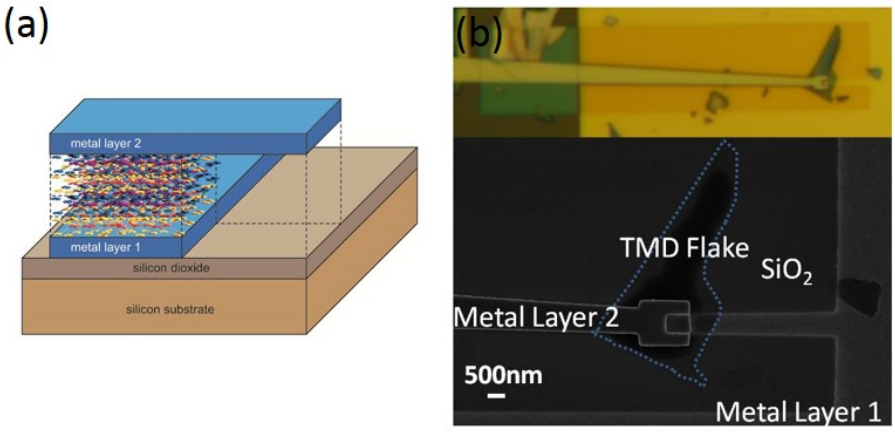


Fig. 2.3. (a) 3D cartoon of a vertical TMD device and (b) optical and SEM images showing the top (Ni) and bottom (Ti/Au) electrodes, and the SiO_2 isolation layer as well as the actual flake. Device design ensures that only vertical transport exists. Copyright © (2017) IEEE.

From the results presented in Fig. 2.4, all the IV curves are symmetric and bidirectional, and it is apparent that MoS_2 devices naturally exhibit high current densities (10^6 A/cm^2 at 3 V for 13 nm), while WSe_2 stacks allow achieving large $NL_{1/2}$ values (1000 for 9 nm) with a trend towards better performance for thinner layer thickness. The tunneling barriers between the material and electrodes play a crucial role for the device performance especially at low bias. The trend of higher current levels for MoS_2 if compared to $MoTe_2$ and WSe_2 is in qualitative agreement with our findings on the change of Schottky barriers (SBs) in lateral devices from the same materials.

Fig. 2.5 illustrates normalize area current density changing with flake thicknesses. As expected, thinner flake device exhibits higher current density. Different metal electrodes do not have obvious effects on the current levels as Fig. 2.5(a) shows. By comparing the performance of these three types of TMD materials, WSe_2 is the best choice in terms of $NL_{1/2}$ and current level.

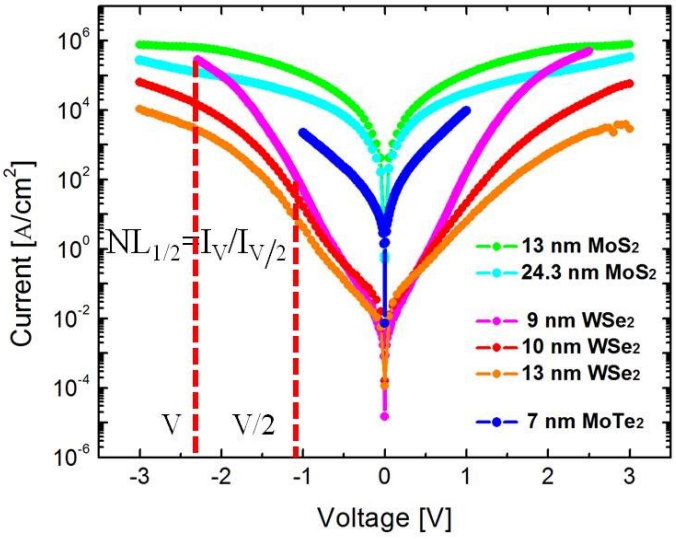


Fig. 2.4. Area normalized I-V curves of vertical MoS_2, WSe_2, and $MoTe_2$ devices for different flake thicknesses. Copyright © (2017) IEEE.

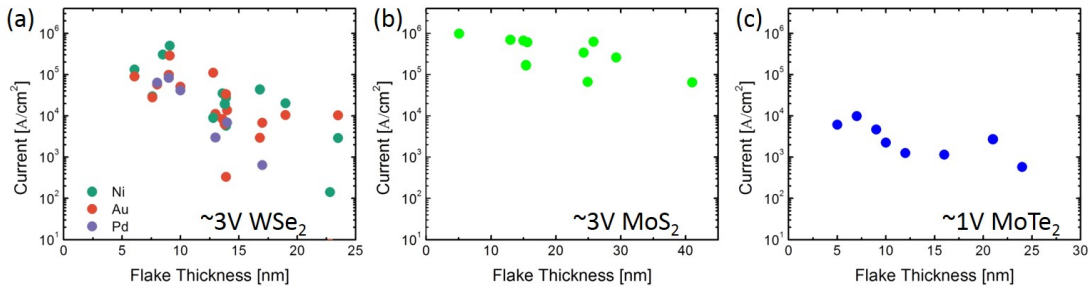


Fig. 2.5. Area normalized current density vs. flake thickness of vertical (a) WSe_2, (b) MoS_2, and (c) $MoTe_2$ devices. (a) shows the current levels of vertical WSe_2 devices with different metal contacts, Ni, Au, and Pd. Copyright © (2017) IEEE.

Fig. 2.6 is a summary benchmarking chart of experimental results of vertical TMD based devices with different flake thicknesses as well as the performance of oxide, MIT, and silicon selectors. Vertical WSe_2 devices exhibit good performance close to silicon based selector and indicate a trend that thinner flake device has

better on-current and $NL_{1/2}$ toward to the target selector performance. Unlike the noncompatibility of BEOL due to the high temperature growth condition in silicon, low temperature TMD growth has been reported to be possible at temperature as low as 350°C [31] indicating an opportunity for integration of novel 3D layered structures of two-terminal TMD selector/RRAM memory (1S1M) unit in the long run.

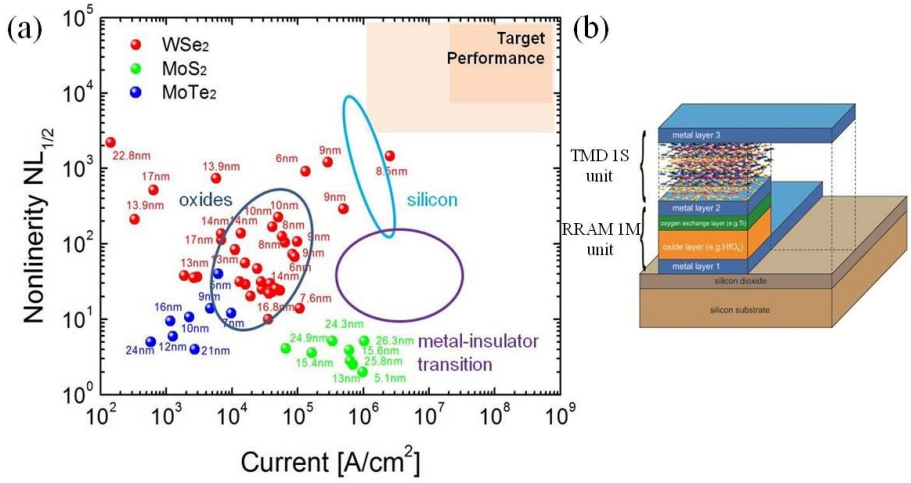


Fig. 2.6. (a) Summary benchmarking chart of WSe_2, $MoTe_2$ and MoS_2 selectors performance with different flake thickness, also including the information on oxide, MIT and silicon selectors provided in reference [32]. The operation voltages of WSe_2 and MoS_2 are around 3V, and the value of $MoTe_2$ is extracted at voltage of 1 V. (b) Layout of the proposed two-terminal TMD-selector / RRAM-memory (1S1M) unit as a vertical implementation of a non-volatile memory. Copyright © (2017) IEEE.

2.3 Conclusion

Two-terminal vertical transition metal dichalcogenide (TMD) based memory selectors were firstly built and characterized. They shows promising performance for the future use. This research shines some light on the new application in the memory field with 2D materials.

3. $MoTe_2$ AND $Mo_{1-X}W_XTE_2$ BASED RESISTIVE RANDOM ACCESS MEMORY (RRAM) DEVICES

Over the past years, transition metal dichalcogenides (TMDs) have attracted attention as potential building blocks for various electronic applications due to their atomically thin nature. An exciting development is the recent success in engineering crystal phases of TMD compounds during the growth due to their polymorphic character. Here, we report an electric field induced reversible engineered phase transition in vertical 2H-$MoTe_2$ devices, a crucial experimental finding that enables electrical phase switching for these ultra-thin layered materials. Scanning tunneling microscopy (STM), scanning tunneling spectroscopy (STS) and scanning transmission electron microscopy (STEM) were utilized to analyze the TMD crystalline structure. Direct confirmation of a phase transition from a 2H semiconductor to a distorted $2H_d$ metallic phase was obtained after applying an electric field. $MoTe_2$ and $Mo_{1-x}W_xTe_2$ alloy based vertical resistive random access memory (RRAM) cells were fabricated to demonstrate clear reproducible and controlled switching with programming voltages that are tunable by the layer thickness and that show a distinctly different trend for the binary compound if compared to the ternary materials.

3.1 Introduction

Many applications such as memristors [34], micro-motors [35], electronic oscillators [36], and sensors [37] greatly benefit from recent trends in the area of phase engineering. The most prominent materials that are explored in this context are VO_2 and NbO_2 which can both undergo a Mott metal-to-insulator transition [38] and amorphous-to-crystalline phase change materials as $Ge_2Sb_2Te_5$ [39]. Recently, transition metal dichalcogenides (TMDs) attracted considerable attention in the field of 2D phase engineering due to their polymorphic character. TMDs exist in various crystalline phases which exhibit semiconducting, semimetallic and metallic properties. In particular, experimental phase diagram data and density functional theory (DFT) calculations indicate that the most thermodynamically stable phase at room-temperature for molybdenum and tungsten containing dichalcogenides is the semiconducting hexagonal (2H) phase, with the exception of WTe_2, for which the metallic octahedral (T_d) crystal structure is stable at standard conditions. However, since for some TMD compounds the energetic difference between the various phases is rather moderate [9] [10], several groups are working on phase engineering of TMDs. For example, Py et al. [40] demonstrated a 2H to 1T phase transition in MoS_2 through the intercalation of lithium and Liu et al. [41] introduced an in-situ phase transition in MoS_2 by means of electron beam irradiation. However, MoS_2 might not be the ideal candidate for TMD phase engineering. Due to a very low energy difference between the metallic (1T′) and the semiconducting (2H) phase of $MoTe_2$, it is considered the most promising TMD material for phase engineered applications [9] [10]. Experimental results on $MoTe_2$ include strain-induced semiconductor-to-metal transitions in $MoTe_2$ at room temperature [42] and growth controlled transformations between the 1T′ and 2H phase by means of tellurization rate [43] and temperature control [44–46]. However, device compatible methods to switch between the different phases in $MoTe_2$ have yet to be reported. Ultimately, for device applications, controlling the phase of a TMD by means of an electric field and introducing a semiconductor-to-metal phase

transition in this way is most desirable. Here we demonstrate experimentally an electric field induced reversible semiconductor-to-metal phase transition in vertical 2H-$MoTe_2$ and 2H-$Mo_{1-x}W_xTe_2$ devices. Scanning tunneling microscopy (STM) was carried out to evaluate the structural impact of the electric field and scanning tunneling spectroscopy (STS) was utilized to unambiguously demonstrate the localized semiconductor-to-metal phase transition. Scanning transmission electron microscopy (STEM) showed that a distorted metallic $2H_d$ phase formed in 2H-$MoTe_2$ and 2H-$Mo_{1-x}W_xTe_2$ based RRAM devices that consist of a sandwich structure of TMD layers between metal electrodes after electric field application. In fact, some preliminary studies on lateral transport through grain boundaries in MoS_2 [47], vertical large area transport through a thick MoO_x/MoS_2 or WO_x/WS_2 stack [48], and vertical large area transport through a 1T MoS_2 nanosheet [49] indicate that TMDs can exhibit memristive features in a two-terminal measurement configuration. However, none of the above articles provides a viable route towards the development of scaled high performance RRAM cells, mainly since in all of the above cases memristive switching depends on, or is mediated by uncontrollable defects in the device structures.Furthermore, the voltage ranges for switching to occur are either intrinsically too large [47] or too small [48] for RRAM applications [18]. In contrast, here we present for the first time vertical RRAM cells with areas in the 0.1 μm^2 range from exfoliated single crystal $MoTe_2$ and $Mo_{1-x}W_xTe_2$ where the switching in these novel cells is mediated by a semiconductor-to-metal phase transition, while maintaining its crystalline structure, and set voltages are approximately linearly proportional to the flake thickness.

3.2 2H-$MoTe_2$ and 2H-$Mo_{1-x}W_xTe_2$ based RRAM

Fig. 3.1(a) shows a schematic as well as optical and SEM images of a typical vertical TMD RRAM device under investigation. Top contact areas are approximately 0.1 μm^2. Our device design ensures that only vertical transport occurs from one to

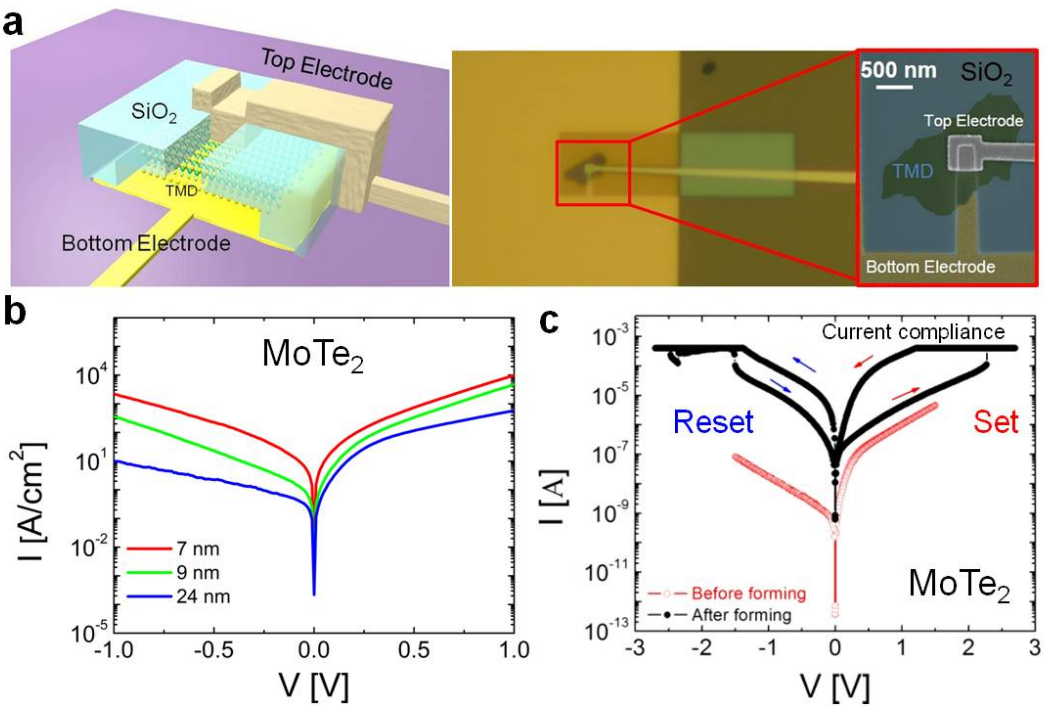


Fig. 3.1. Vertical TMD based device characterization. (a) Schematic diagram of a vertical TMD device and optical and SEM images showing the top (Ti/Ni) and bottom (Ti/Au) electrodes, and the SiO_2 isolation layer as well as the actual flake. (b) Area normalized I-V curves of vertical $MoTe_2$ devices before electroforming for different flake thicknesses. (c) I-V curves of a vertical $MoTe_2$ device from a flake with a thickness of 24 nm and a contact area of 520 nm x 330 nm. Red circles show I-V curves before memristive switching occurred. The solid black dots show the current versus voltage dependence after forming. Arrows indicate the sweep direction of the applied DC voltage. The current compliance is set to 400 μA. Copyright © (2019) Springer Nature.

the other electrode without any lateral transport contributions. Because of the large aspect ratio between the top contact area and the flake thickness, spreading resistance contributions can be ignored and the active device area is identical to the top contact area. Area normalized I-V curves of exemplary vertical $MoTe_2$ devices are shown in Fig. 3.1(b). For all measurements the bottom electrode was grounded. Experimental

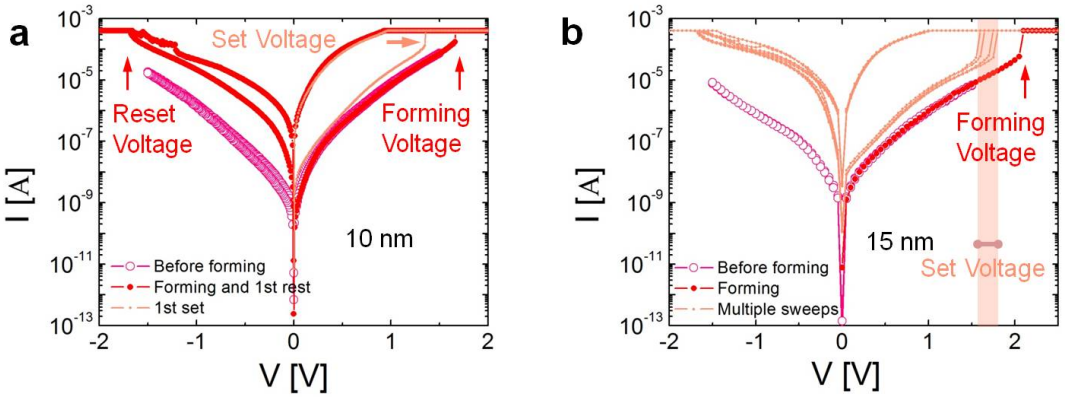


Fig. 3.2. Typical I-V curves of a vertical $MoTe_2$ RRAM showing the forming process. (a) RRAM forming for a 10 nm thick flake including first set and reset. (b) Multiple sweeps after forming had occurred for a 15 nm flake. Note the rather narrow band of set voltages. Current compliance is set to 400 μA for both cases.

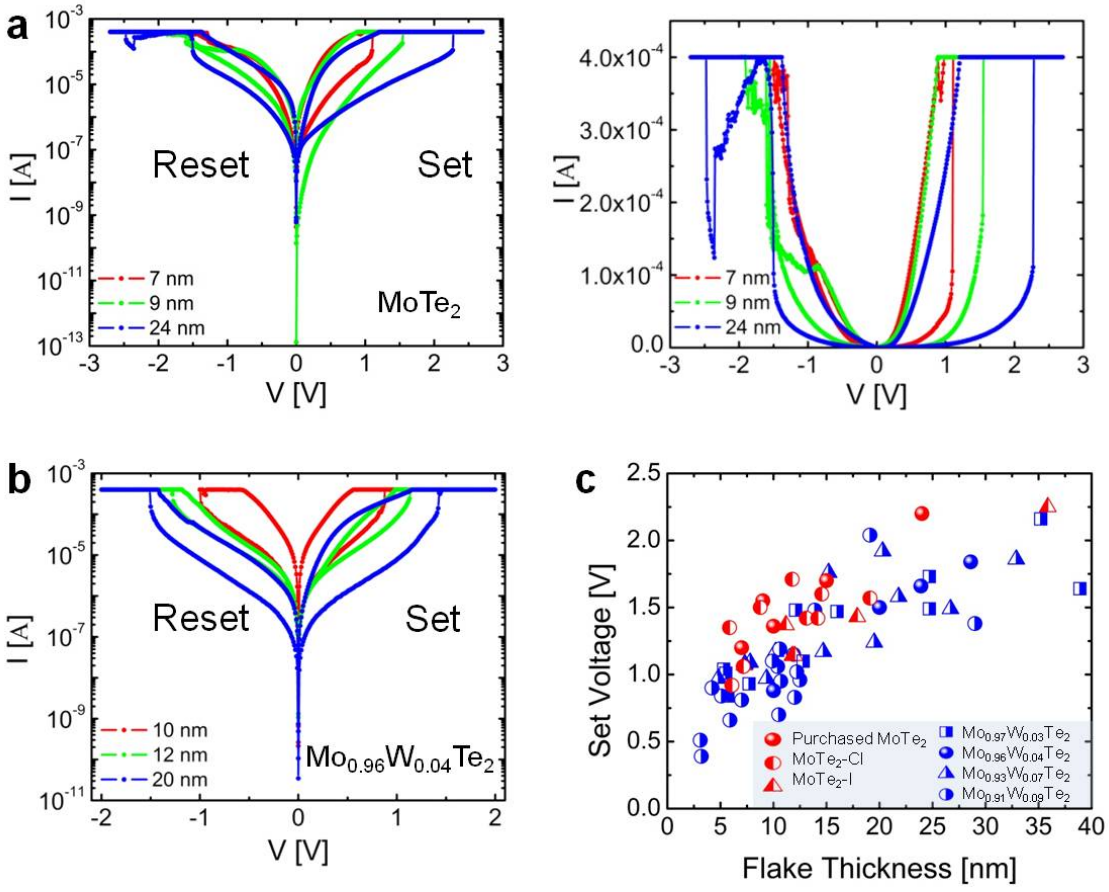


Fig. 3.3. 2H-$MoTe_2$and 2H-$Mo_{1-x}W_xTe_2$ based RRAM behavior and their set voltages as a function of flake thickness. (a) Log and (b) linear scale I-V curves of vertical $MoTe_2$ RRAM devices after electroforming. The active device area of the 7 nm, 9 nm, and 24 nm $MoTe_2$ flake devices are 542 nm x 360 nm, 542 nm x 360 nm and 518 nm x 332 nm respectively. (c) Log scale I-V curves of vertical $Mo_{0.96}W_{0.04}Te_2$ RRAM devices after electroforming with a current compliance of 400 μA. The active device area of the 10 nm, 12 nm, and 20 nm $Mo_{0.96}W_{0.04}Te_2$ flake devices are 500 nm x 380 nm, 522 nm x 400 nm and 510 nm x 384 nm respectively. (d) Set voltage values scale with the flake thickness of $MoTe_2$, $Mo_{0.97}W_{0.03}Te_2$, $Mo_{0.96}W_{0.04}Te_2$, $Mo_{0.93}W_{0.07}Te_2$ and $Mo_{0.91}W_{0.09}Te_2$. The error bars of the set voltages and the flake thicknesses are in the range of the dots sizes. $MoTe_2$-Cl and $MoTe_2$-I denote crystals grown with $TeCl_4$ and I_2 transport agents, respectively.

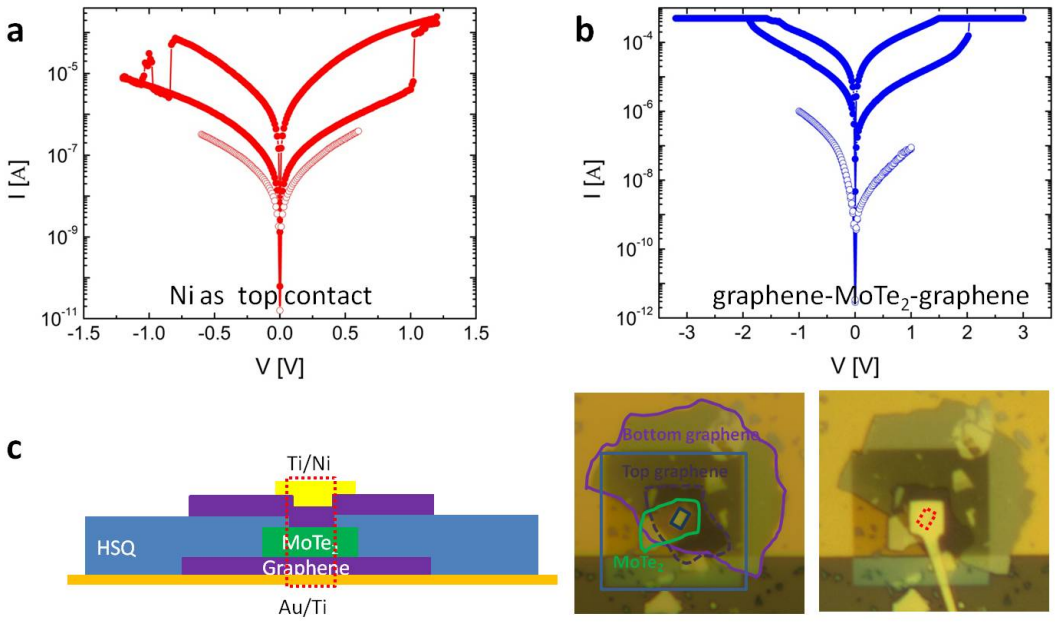


Fig. 3.4. Impact of the choice of metal electrodes on the RRAM behavior. (a) The intrinsic and RRAM curves of a vertical $MoTe_2$ device with Ni as top contact. The Au bottom pad is the source in these measurements. (b) The intrinsic and RRAM curves of a vertical graphene-$MoTe_2$-graphene device. The top graphene layer acts as the source in these measurements. (c) A schematic and optical images of a graphene-$MoTe_2$-graphene device. Note that the bottom graphene is located on a Au pad and that the top graphene layer is capped by a Ti/Ni electrode to ensure true vertical transport.

current densities follow the expected trend with thickness. Device characteristics are reproducible and do not change substantially after multiple scans between -1 V and +1 V. The situation however changes when the voltage range is extended. $MoTe_2$ devices can transition into a LRS as illustrated in Fig. 3.1(c) at a set voltage (here V_{SET} = 2.3 V). The details on the forming process are provided in Fig. 3.2. After the forming event, device characteristics can be cycled to exhibit typical bipolar RRAM behavior in terms of: a) remaining in their LRS when no voltage is applied, b) preserving the low resistive state over an appreciable voltage range until a sufficient reset voltage (here V_{RESET} = -1.5 V) of polarity opposite to the set voltage is reached, and c) remaining in their respective high resistive state (HRS) until the set voltage is reached. Note that after the forming has occurred the HRS always remains more conductive than the original state of the device indicating that a permanent electronic change has occurred. For the case displayed in Fig. 3.1(c), the current ratio between the HRS and the LRS is about 50 at V_{READ}=1 V when the compliance is set to 400 μA.

In order to further explore the switching mechanism in TMDs, RRAM cells with exfoliated $MoTe_2$ layer thicknesses between 6 nm and 36 nm were fabricated. All cells were nonvolatile and stable for read disturb measurements. Before the forming process, the current per unit area through the vertical structures scales approximately inversely proportional with the flake thickness for not too small voltages (Fig. 3.1(b)). However, once the system transitions into its LRS, current levels (below the compliance) occur to be rather similar and do not show any coherent scaling trend with the flake thickness or active device area. This observation is consistent with the notion that the formation of conductive filaments that enable the LRS is not uniform but gives rise to local current paths. For flake thicknesses from 6 nm to 36 nm, the set voltages can be tuned from 0.9 V to 2.3 V (see Fig. 3.3(d)). Noteworthy, the RRAM behavior is independent of the contact metal used, which indicates that the switching mechanism does not involve tunneling through the interfacial Schottky barriers or

metal ions diffusion. For example, employing Ni or graphene instead of Ti/Ni as top electrode resulted in the same RRAM performance as shown in Fig. 3.4.

Next, we explore the impact of the material preparation and composition on RRAM characteristics by extending experiments to 2H-$MoTe_2$ obtained using different approaches and further to 2H-$Mo_{1-x}W_xTe_2$ alloys. Similar switching characteristics of $MoTe_2$ devices fabricated using either commercial material or crystals synthesized in this work using different temperatures and transport agents (see Methods) indicate that the observed RRAM effect is not related to the processing conditions (Fig. 3.3(c)). $Mo_{1-x}W_xTe_2$ devices exhibit very similar switching behavior and their characteristics also depend monotonically on the flake thickness (see Figs. 3.3(b) and (c)). However, while we are currently unable to resolve a quantitative trend of the set voltages as a function of W-content, the set voltages for the $Mo_{1-x}W_xTe_2$ alloys show a tendency of being smaller than for the $MoTe_2$ devices (see Fig. 3.3(c)), implying that the critical electric field needed to trigger the RRAM behavior may have been reduced in alloys. DFT calculations [10, 50, 51] and recent experimental results [52] suggest that substitution of Mo by W in $MoTe_2$ and creation of a $Mo_{1-x}W_xTe_2$ alloys reduces the energy difference between 2H and 1T′ phases, which in turn should reduce the set voltages of $Mo_{1-x}W_xTe_2$ RRAM devices as compared with their $MoTe_2$ counterparts. We believe that Fig. 3.3(c) shows a first experimental evidence of this trend.

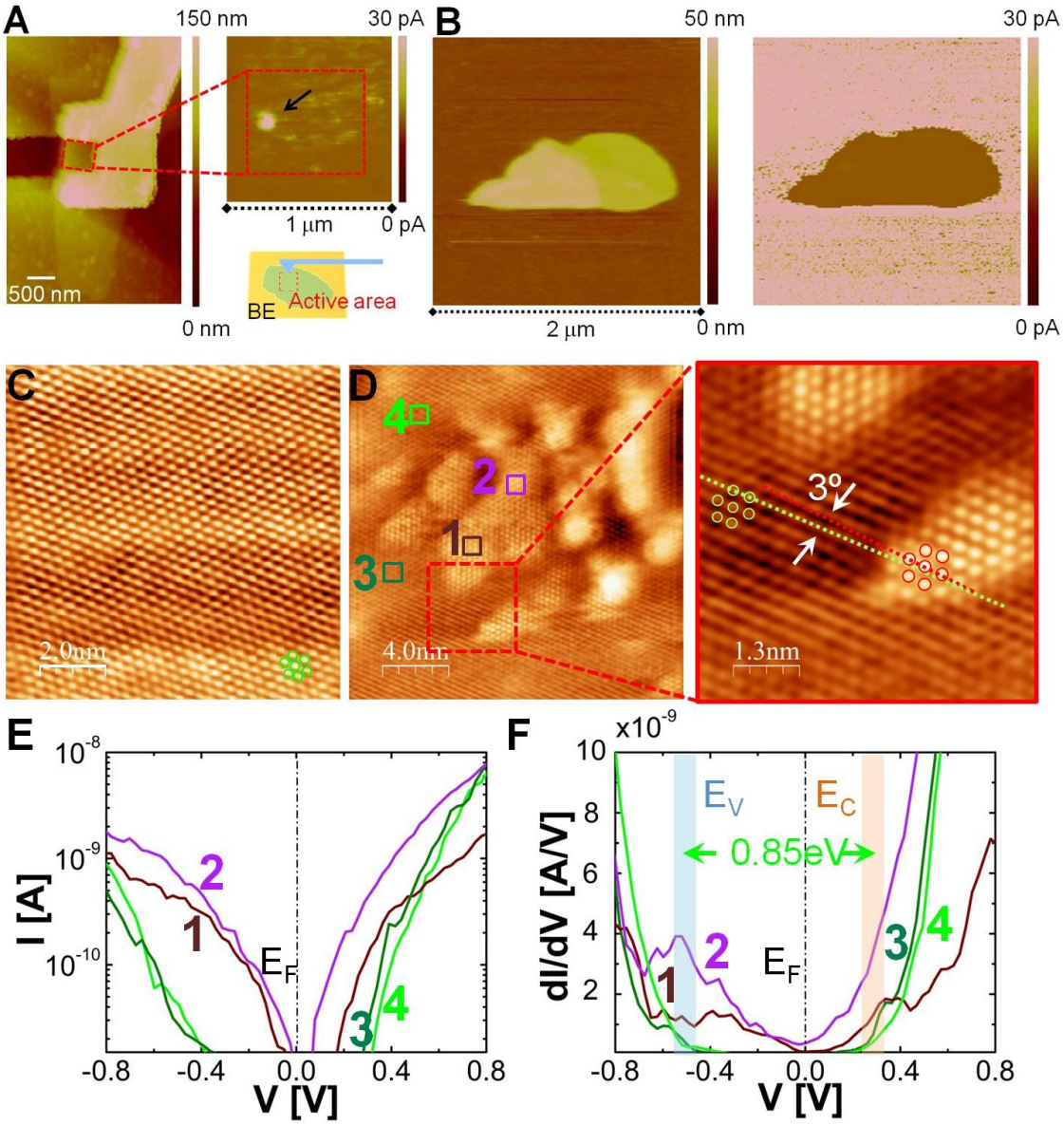
3.3 Electric field induced semiconductor-to-metal transition

In general, the electroforming process in RRAM devices aims at creating a conductive filament by applying a sufficiently high electrical bias, which in turn results in an electric field and Joule heating inside the sample. Both, the field and the heating can result in the formation of conductive filaments that define the LRS while the HRS is characterized by the absence of these filaments [18]. In order to confirm the formation of conductive filaments in the case of $MoTe_2$ RRAM cells, conductive AFM

(C-AFM) measurements were carried out. First, a fully functional $MoTe_2$ device was biased to form the LRS, and then wet chemical etching was used to remove the top electrode. This approach allows access to the TMD surface after the presumed filament formation to perform a local analysis of the surface resistivity after the forming process had occurred. As shown in inset of Fig. 3.5(a) by the arrow, a bright spot of 80 nm in diameter, which was formerly covered by the top electrode (red marked rectangle), is indicative of a current path through the TMD. For comparison, those $MoTe_2$flakes that did not undergo a forming process show a uniform, highly resistive surface (see Fig. 3.5(b)).

In order to explore the filament formation mechanism in case of $MoTe_2$, STM was used to perform a detailed surface analysis at room temperature. Fig. 3.5(c) shows a representative STM image of the pristine exfoliated $MoTe_2$ flake. The atomic surface structure of the 2H-phase of the $MoTe_2$ single crystal demonstrates the expected C_3 symmetry with an interatomic distance of 0.34 nm. Imaging was performed with a bias voltage of -0.9 V. To mimic the situation in $MoTe_2$ RRAM cells under forming conditions, a bias of -3 V was applied to a contact underneath the TMD relative to the STM tip while scanning. Next, an STM image was taken again at a bias of -0.9 V. As apparent from Fig. 3.5(d) the surface image appears drastically different after voltage application, and non-uniform bright regions are clearly visible in the figure. A corrugation profile measured along the bright region. Protrusions with a height of 0.3 nm to 0.6 nm on the sample surface are clearly observed, which are interpreted as possible topographic changes in conjunction with changes in the local density of states (LDOS) (see discussion below). Next, scanning tunneling spectroscopy (STS) measurements were performed at four distinct locations as marked by the colored squares 1 through 4 in Fig. 3.5(d). Locations 1 and 2 fall into the region of alteration while 3 and 4 are located in the unperturbed region of the sample that we will label as pristine in the following discussion. Fig. 3.5(e) shows the obtained I-V characteristics at the four locations. Higher current levels in particular for small applied voltages are observed for locations 1 and 2 (the modified areas) if compared

Fig. 3.5. C-AFM, STM and STS measurements. (a) Current mapping of a $MoTe_2$ flake after the set process and the formation of the LRS has occurred using a conductive AFM (C-AFM). The red dashed square denotes the active device area before removal of the top electrode. Note the bright spot marked with an arrow that we interpret as a filament. (b) C-AFM images of a pristine $MoTe_2$ flake (left: topography and right: current map) showing no indication of the aforementioned highly conductive area. (c) STM image (filtered) of the pristine $MoTe_2$ surface. (d) STM image (filtered) of a portion of the surface region in (c) after a voltage of -3 V was applied to a contact underneath the TMD relative to the STM tip. The zoom-in image indicates that the position of Te atoms has changed after voltage application. The Te rows in the voltage modified region are rotated 3° relative to the atomic rows in the pristine part. However, the C_3 symmetry of the atomic lattice is still clearly visible (green circles for pristine part and red circles for modified area). All images were recorded at tunneling currents of 2 nA and a bias voltage of -0.9 V. (e) shows I-V characteristics obtained by STS measurements corresponding to locations 1 through 4 in (d). (f) shows the corresponding dI/dV spectra with the blue band indicating the position of the valance band edge and the orange band indicating the position of the conduction band edge for the pristine $MoTe_2$ in agreement with the I-V characteristics of locations 3 and 4. Note that 1 and 2 clearly show the absence of a bandgap after voltage application.


A
150 nm
30 pA
1 μm
0 pA
500 nm
BE
Active area
0 nm
B
50 nm
30 pA
2 μm
0 nm
0 pA
C
2.0nm
D
4
2
1
3
4.0nm
3º
1.3nm
E
10^-8
10^-9
10^-10
I [A]
2
1
E_F
3
4
-0.8
-0.4
0.0
0.4
0.8
V [V]
F
x10^-9
10
8
6
4
2
dI/dV [A/V]
E_V
E_C
← 0.85eV →
1
2
E_F
3
4
-0.8
-0.4
0.0
0.4
0.8
V [V]

with 3 and 4 (pristine areas). The corresponding dI/dV curves shown in Fig. 3.5(f) are a measure of the local density of states (LDOS). While characteristics obtained for the pristine areas (locations 3 and 4) indicate the presence of a bandgap in the range of 0.85 eV, consistent with the extracted bandgap of 2H-$MoTe_2$ from electrical measurements [53], the LDOS of locations 1 and 2 shows a finite density of states even at zero bias, implying that these regions had become metallic after a forming voltage had been applied. At a first glance, the positions of atoms in the modified (red circle) and the pristine (green circles) regions occur identical (C_3 symmetry) as shown in the zoom-in Fig. 3.5(d). However, by comparing the positions of atomic sites along the red and green dashed lines, a clear distortion between tellurium atoms in the pristine and voltage disturbed areas is apparent. The atomic rows of Te in the pristine and voltage modified areas are rotated relative to each other by 3° to 6° as shown in Fig. 3.5(d). The same phenomenon is observed when $Mo_{0.96}W_{0.04}Te_2$ devices are analyzed by STM (see Fig. 3.6 for details). Last, it is important to note that like in the RRAM cell metallic features that were created by applying a voltage of -3 V can be turned semiconducting again by applying a voltage of opposite polarity. Since the change of surface topography is highly non-uniform however, it is at this stage not possible to unambiguously follow one particular STM feature exclusively through the setting and resetting procedure. The sum of these observations lead us to believe that $MoTe_2$ undergoes a reversible phase transition from a semiconducting to a metallic state under application of an electric field, which is responsible for the RRAM behavior observed by us and reported here.

Next, it is worth asking the question whether any stable metallic phase is expected to exist in $MoTe_2$ that can be created by means of an electric field. Indeed, STM tip induced phase transitions were observed previously in $TaSe_2$ [54] and TaS_2 [55] Moreover, DFT calculations [9] predict that the semiconducting 2H phase in $MoTe_2$ is energetically different by only 31 meV per formula unit from the semi-metallic monoclinic 1T′ phase, a value much smaller than for other TMDs. While these facts speak potentially for an electrically induced 2H-to-1T′ phase transition, one

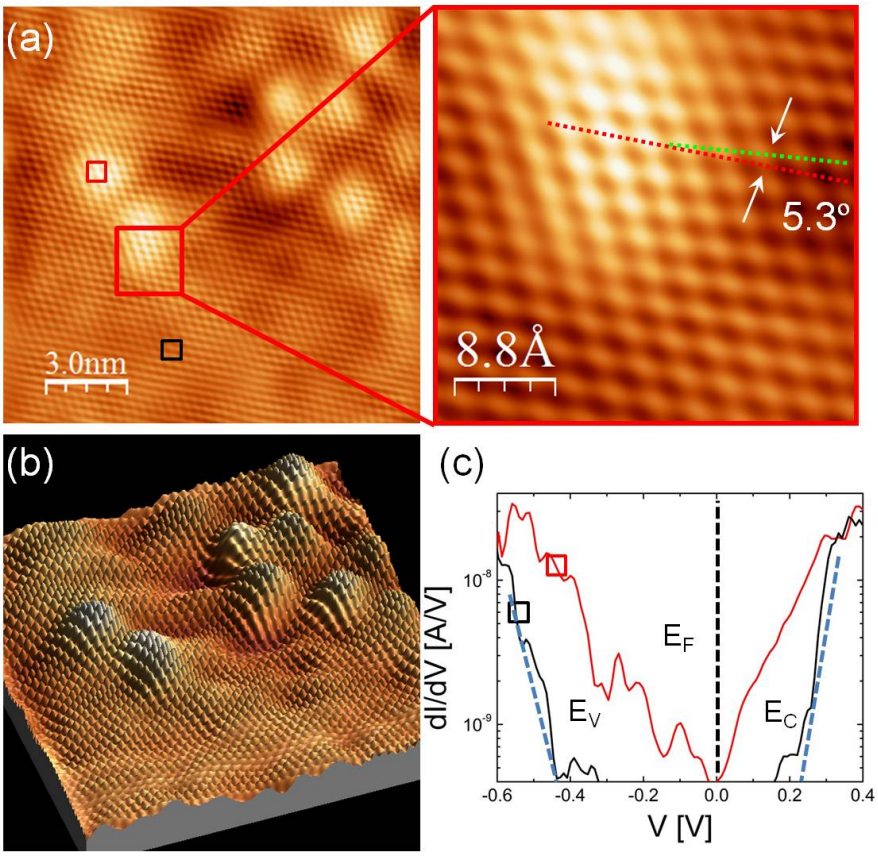


Fig. 3.6. (a) STM image (FFT filtered) of $Mo_{0.96}W_{0.04}Te_2$ after a voltage of -3 V was applied to a contact underneath the TMD relative to the STM tip. Bright spots are created, similar to the case of $MoTe_2$ after electric field modification. The zoom-in image indicates that the positions of Te atoms have changed after voltage application. Both images were recorded at tunneling currents of 2 nA and at a bias voltage of -0.9 V. (b) is the 3D image of (a), if treating the bright areas as protrusions. (c) dI/dV spectra corresponding to the marked positions in (a). The bright area shows metallic behavior after voltage modification.

would expect to observe a rectangular surface unit-cell in the areas of the protrusions which is characteristic for the 1T′ phase, while our STM image supports more a rotation of the hexagonal 2H-$MoTe_2$ surface cell between the pristine and the voltage modified areas. On the other hand, the 1T′ phase is a modified 2H phase with distinct atomic shifts, and the projected structures, e.g. of Te, on (001) for both 2H and 1T′ have rather similar lattice constants, with a=3.52 Å for the 2H hexagonal phase and a=3.47 Å, b=6.33 Å for the 1T′ pseudo-hexagonal phase. It is thus possible that the topographical changes hinted at above mask the clear distinction between those two phases. An alternative explanation, involves an electrical field induced local rotation of the topmost 2H-$MoTe_2$ planes, resulting in the observed angle between Te-rows in the pristine and modified areas as described above (see Fig. 3.5(d)). Indeed, similarly rotated structures have been reported after electron irradiation of 2H-$MoTe_2$ [56]. Since the atomic arrangement in the modified and the pristine regions occur similar as shown in the zoom-in Fig. 3.5(d), we conclude at this stage that a metallic hexagonal 1T phase or a metallic distorted $2H_d$ phase has been created by applying an electric field.

To identify the exact nature of the observed field induced phase change further, scanning transmission electron microscopy (STEM) of cross-sectional samples was utilized for both $MoTe_2$ and $Mo_{1-x}W_xTe_2$ devices. Before performing the STEM analysis, RRAM devices underwent the same forming process as described above to create filaments in the flakes. Fig. 3.7(a) shows a cross-sectional atomic-resolution high-angle annular dark field (HAADF)-STEM image of a $Mo_{0.96}W_{0.04}Te_2$ device. The RRAM multilayer structure is clearly visible from the HAADF contrast. Note that the STEM image displays the TMD flake both in the active $Ni/Ti/Mo_{0.96}W_{0.04}Te_2/Au/Ti/SiO_2$ (right) and non-active region (left) where an SiO_2 isolation layer on top of the TMD prevented RRAM operation. For all scans performed, we observe that the non-active area only exhibited the original 2H phase of $Mo_{0.96}W_{0.04}Te_2$. On the other hand, in the active region, two structurally distinct domains are observed; the domains are marked as 2H and $2H_d$ in Fig. 3.7(b), which is a zoom-in HAADF image of the

red-marked box in (a). The $2H_d$ region, delineated by the white dash-dotted lines, is about 80 nm wide (consistent with the diameter of the filament measured by C-AFM) and extends vertically through the whole $Mo_{0.96}W_{0.04}Te_2$ flake. Fig. 3.7(c) of the 2H region shows an atomic HAADF image in $[110]_{2H}$ zone axis with well-resolved atomic columns of Mo/W and Te. Fig. 3.7(d) shows a structural HAADF image from the $2H_d$ domain. Instead of the well-aligned atomic columns as observed for the 2H structure, the atomic columns of the $2H_d$ structure are not resolved in this orientation due to apparent shift and splitting along the c-direction.

In an attempt to achieve better structural resolution of the $2H_d$ structure, the TEM sample was tilted 30° around the c-axis of the 2H to $[120]_{2H}$ zone axis. For the 2H structure, Fig. 3.7(e) shows again well-resolved atomic columns of the 2H phase. As for the $2H_d$ structure, Fig. 3.7(f) shows a distinct splitting for both Te and Mo/W atomic columns, which suggests that the atoms in each atomic column experienced a substantial relative displacement, primarily along the c-direction, upon electric field application. Nano-beam diffraction (NBD) was further performed in an attempt to understand the details of the $2H_d$ structure. Figs. 3.7(g) and (h) are NBD patterns taken from the $2H_d$ structure with the neighboring 2H structure in $[110]_{2H}$ and $[120]_{2H}$ zone axes respectively. There are no additional reflections beyond the 2H superlattice reflections observed, neither along the rows indicated by yellow arrows nor between the reflections as illustrated by the blue arrows in Fig. 3.7(h). The absence of such extra-reflections precludes the presence of the well-known 1T, 1T′ and T_d phases in the region of the $2H_d$ structure. Although the atomic images of the $2H_d$ structure in Fig. 3.7(d) and (f) show substantial differences from the 2H structure, no apparent differences could be recognized in the NBD patterns taken from the $2H_d$ structure and neighboring 2H structure. These observations suggest that the $2H_d$ phase is a distorted metallic modification of the 2H structure, perhaps some transient state with atoms displaced toward one of the lower symmetry structures, but still within the crystal symmetry of the 2H structure.

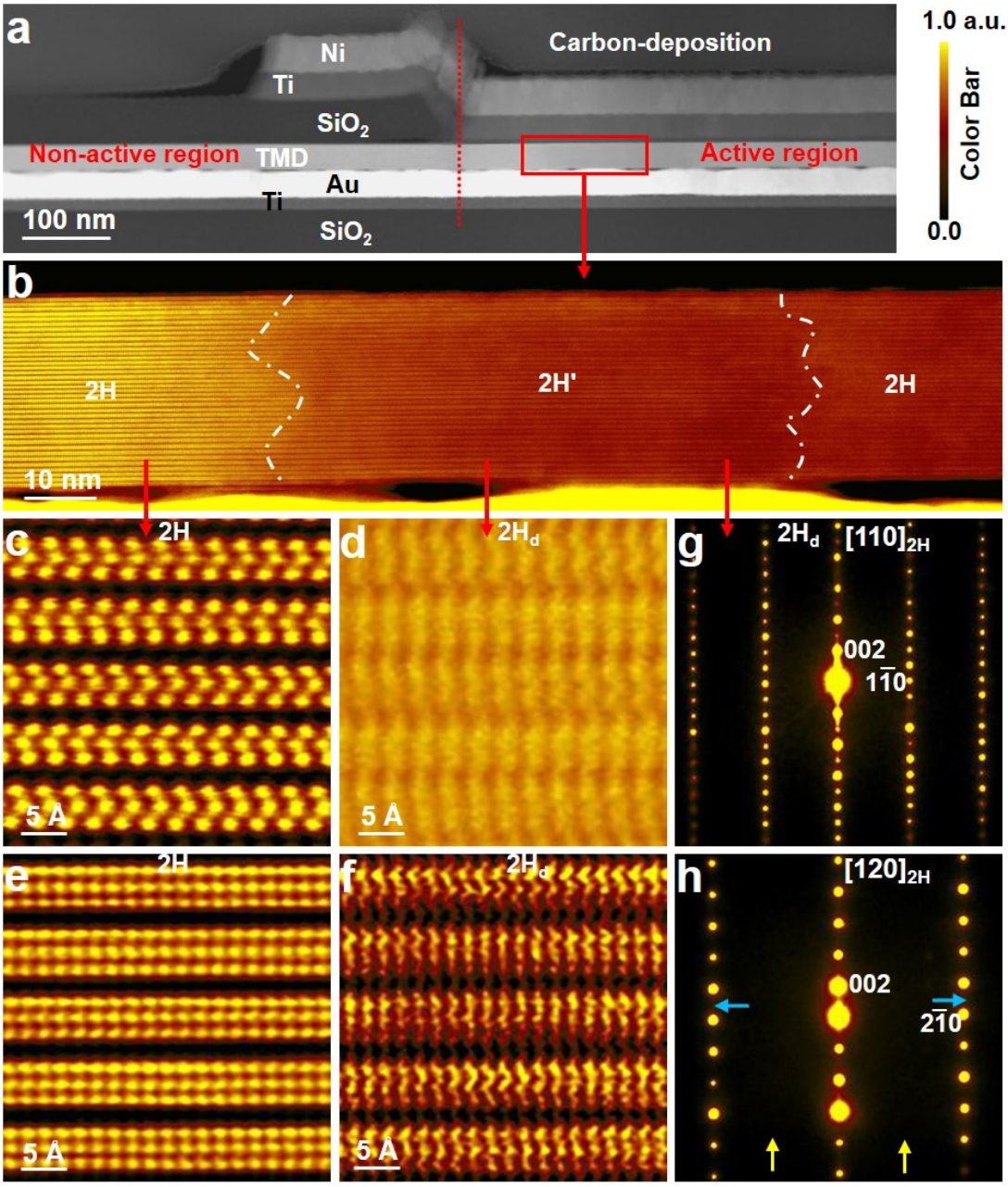


Fig. 3.7. STEM measurement and analysis. (a) HAADF-STEM image showing cross-section of the $Mo_{0.96}W_{0.04}Te_2$ device. (b) Higher magnification HAADF image from the region defined by a red box in (a) and showing co-existence of a distorted structure ($2H_d$) with 2H. (c, d, e, f) Atomic-resolution HAADF images taken along the $[110]_{2H}$ zone-axis (c, d) and $[120]_{2H}$ zone-axis (e, f), showing the intact 2H and distorted $2H_d$ structures respectively. (g, h) Corresponding nano-beam diffraction pattern taken from the distorted $2H_d$ area, which is still indexed as the 2H structure. False colors are added to aid the eye.

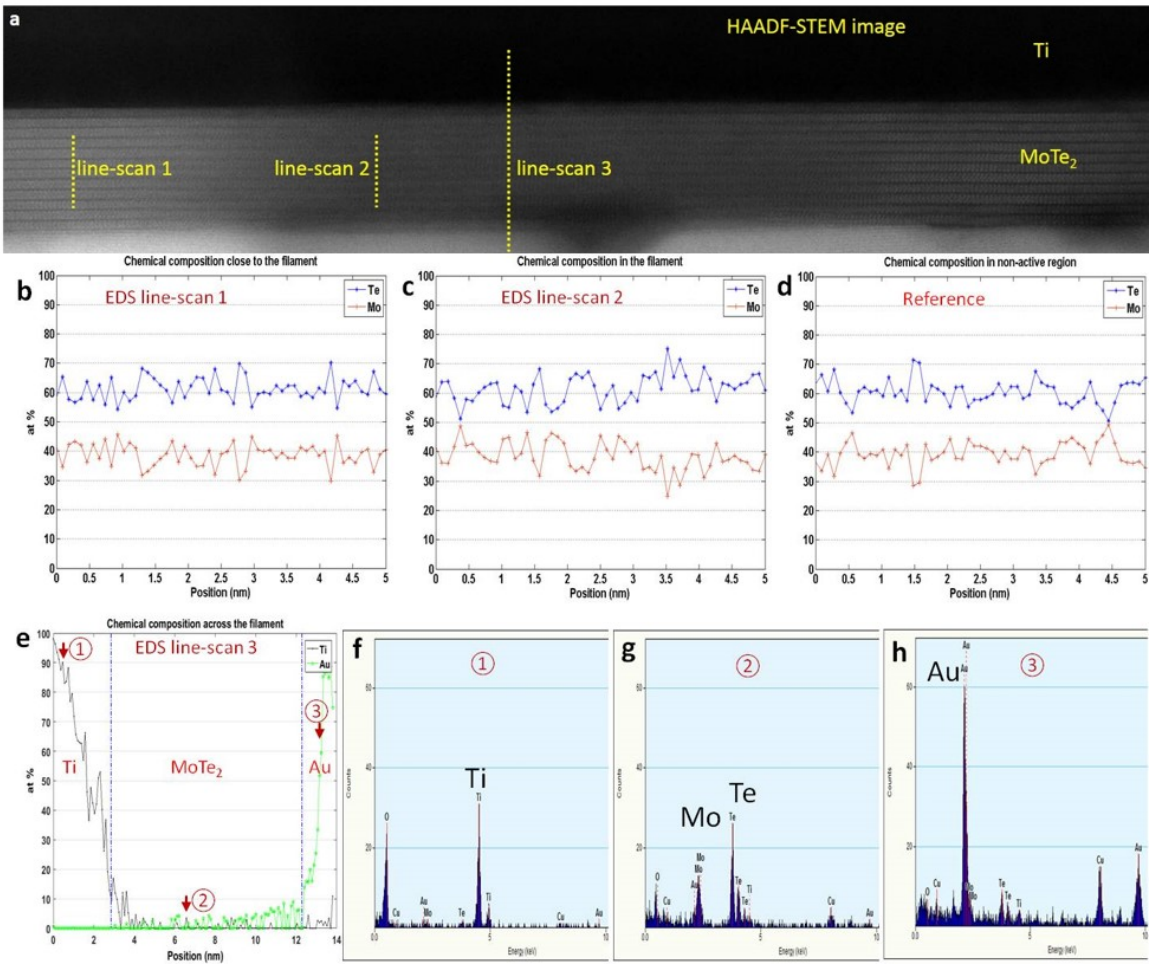
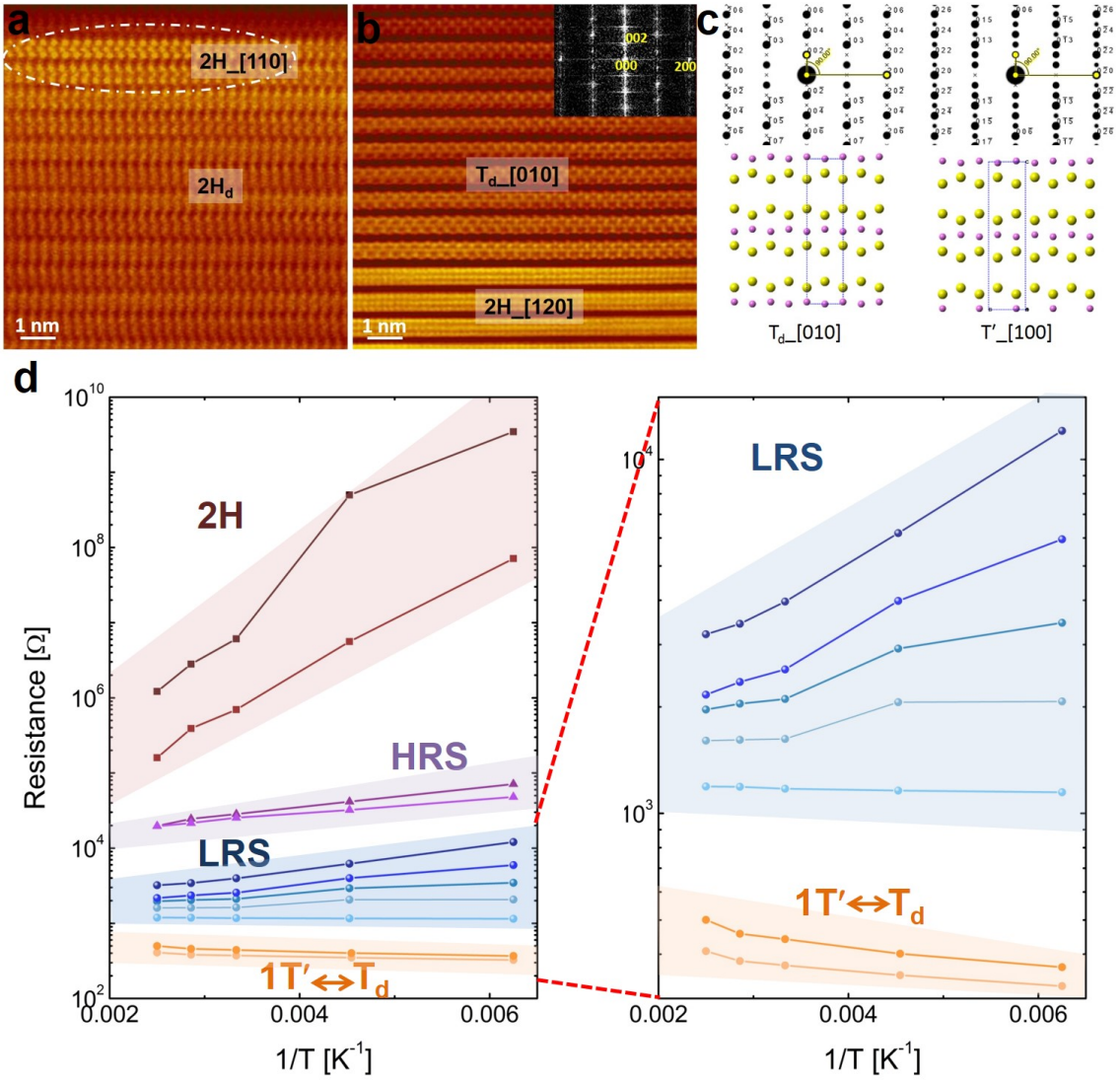


Fig. 3.8. EDS line-scan analysis on a device in its low resistive state (LRS) after repeatedly cycling the device from the HRS to the LRS. (a) HAADF-STEM image showing a filament and the line-scan positions in an active region. (b) Line-scan close to the filament. (c) Line-scan in the filament. (d) Reference line-scan from a non-active region. (e) Line-scan across the filament showing no evidence of Ti or Au presence in the $MoTe_2$ layer. Blue lines showing the interfaces of the Ti/$MoTe_2$ and $MoTe_2$/Au layers. The red arrows and numbers indicate the positions where individual single pixel raw EDS spectra were extracted for figures (f-h), respectively.

Fig. 3.8 shows EDS line-scan results for $MoTe_2$ based RRAM devices. The devices underwent multiple cycles from the HRS to the LRS. A detailed comparison of the elemental distribution of Te and Mo in the filament and close to the filament regions with the Te to Mo distribution of the pristine structure in the non-active region (Fig. 3.8(a-d)) suggests almost no change in the Mo:Te stoichiometry. However, the existence of vacancies cannot be entirely ruled out due to the limited resolution of the EDS scans. Moreover, the EDS line scan analysis shows that metal ion diffusion is not the reason for the observed RRAM behavior in $MoTe_2$ devices. It should be noted that the weak Ti and Au signals detected in the $MoTe_2$ layer near the Ti/$MoTe_2$ and $MoTe_2$/Au interfaces (Fig. 3.8(e-h)), arise most likely from sputtering contamination during FIB ion milling, as well as from multi-scattering of a small amount of electrons and X-rays which were re-directed into the neighboring sample area. For example, a Cu signal from the copper TEM sample grid was typically present in the TEM EDS spectrum, as observed in Fig. 3.8(g-h). Our EDS analysis further supports the above statement that the RRAM behavior is not related to the metal ion diffusion mechanism.

Most of the devices studied in the way described above exhibited similar behavior: 2H structure in the matrix and $2H_d$ structure in the filament. However, one device as shown in Fig. 3.9(b) displayed a filament consisting of the 2H phase together with the orthorhombic T_d phase. This is an unexpected finding, since 1T′ $MoTe_2$ should be more stable than the T_d phase at room temperature and above (although the T_d phase can be formed from the 1T′ phase at temperatures below ≈240 K [57]). This observation, which is substantiated by the fast Fourier transform (FFT) pattern in the inset of Fig. 3.9(b) and the matching atomic structure model in Fig. (c), is a clear indication that phases that are typically not stable in a bulk state can be stabilized in a heterostructure due to the particular boundary conditions. This finding and the fact that we had observed a span of LRS values for different compliance settings and scanning conditions prompted us to perform temperature dependent electrical measurements. We carefully compared the temperature dependent electrical

Fig. 3.9. STEM images and resistance of vertical $MoTe_2$-based devices versus temperature in their respective 2H, HRS, LRS and 1T′. (a) Atomic-resolution HAADF image taken along $[110]_{2H}$ zone-axis from the filament area, showing coexistence of $2H_d$ and 2H. (b) Atomic-resolution HAADF image taken along $[120]_{2H}$ zone-axis an orthorhombic T_d phase is clearly observed together with the 2H phase. Inset in the right top corner is the corresponding FFT image. (c) Structural projections of two corresponding variants of orthorhombic T_d and monoclinic 1T′ phases of $MoTe_2$ (in the bottom) and simulated electron diffraction patterns (in the top). (d) Semiconducting behavior is observed for the 2H intrinsic state and for the HRS state. The $1T'/T_d$ device at the bottom shows clear metallic behavior as apparent from the decrease in sample resistance towards lower temperatures. The LRS temperature dependent results show a gradual change in their slope indicating a transition from semiconducting to metallic behavior. Note that each line is obtained from an individual device which was set to the corresponding state at room temperature before the temperature dependent measurements were performed.


a
2H_[110]
2H_d
1 nm
b
002
000
200
T_d_[010]
2H_[120]
1 nm
c
T_d_[010]
T′_[100]
d
2H
HRS
LRS
1T′↔T_d
Resistance [Ω]
1/T [K^-1]
LRS
1T′↔T_d
1/T [K^-1]

properties of the intrinsic 2H phase with the HRS and LRS states, as well as with reference devices fabricated from 1T′ $MoTe_2$. The test devices were set to the HRS and the LRS respectively at room temperature and then characterized as a function of temperature from 160 K to 400 K at a voltage of 0.5 V. Devices kept their original state (either LRS or HRS) during the full temperature cycle. Fig. 3.9(d) shows the result of our temperature dependent characterization. Both, the intrinsic 2H state and the HRS show a distinctly higher resistance at lower temperatures, which is consistent with semiconducting behavior. On the other hand, for the LRS devices there is a clear spread in the temperature dependent resistance slopes with a decreasing slope for decreasing sample resistance in the LRS. Interestingly, the lowest resistance values that we observed in the LRS and the corresponding slopes as a function of inverse temperature are approaching what was measured for reference 1T′ $MoTe_2$ samples. Moreover, as shown in the Fig. 3.10, the device with the T_d phase shown in Fig. 3.9(b) exhibited the lowest observed resistance values after setting. The sum of these observations in conjunction with the observed $2H_d$ structure and T_d phase from STEM after setting provides experimental evidence that the observed $2H_d$ structure is a transitional structural state between 2H and 1T′ or T_d. Devices that exhibit lowest LRS values are electrically more similar to the 1T′ or T_d phase, while devices with higher LRS exhibit a transient $2H_d$ state.

3.4 Model description of the transition from 2H to $2H_d$

While the 2H structure is based on the -AbA-BaB- stacking of hexagonal layers with $MoTe_6$ prismatic coordination, the stacking sequence in the 1T′ and T_d phases changes to -AbC-BcA- with octahedral coordination. Since 2H is a higher-symmetry structure ($P6_3/mmc$) in comparison to 1T′/T_d, its transformation into latter with preserved 2D-layers coherency should result in possible six variants of 1T′/T_d that are related by nearly-60° rotation around the $[001]_{2H}$ axis. Our simulation of electron diffraction patterns in Fig. 3.11(a) shows that 2 out of 3 orientational variants of

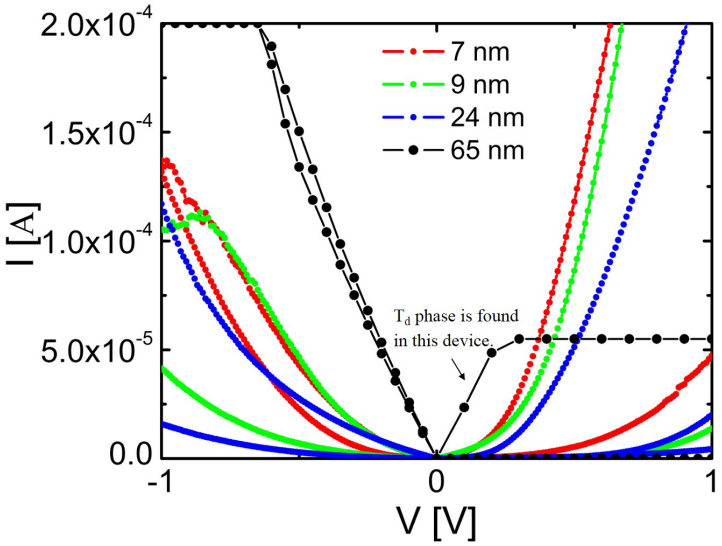


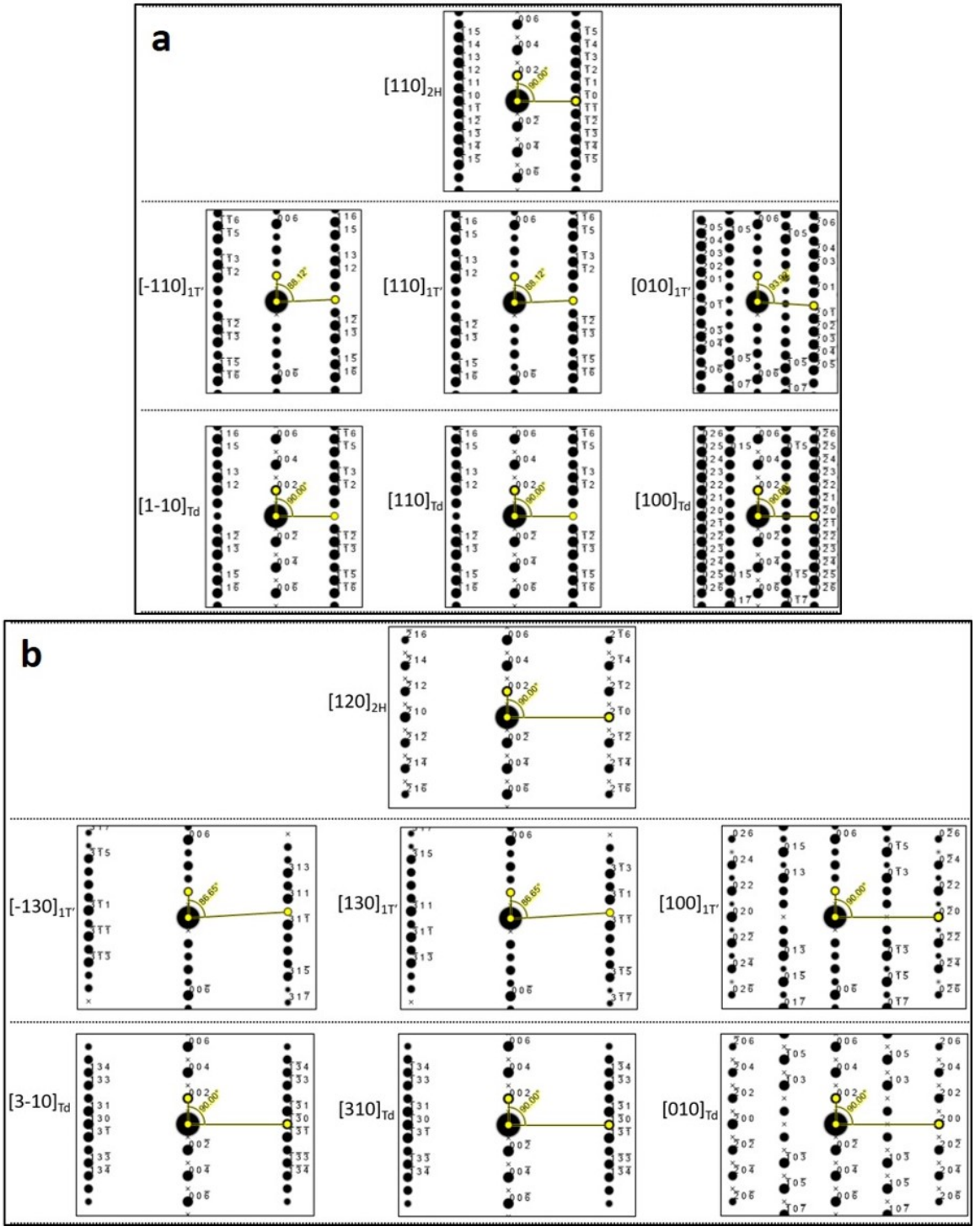
Fig. 3.10. Linear scale I-V curves of vertical $MoTe_2$ RRAM devices after forming.

1T′/T_d have patterns similar to 2H in [110] zone-axis. One can indeed expect very similar electron diffraction patterns of 2H in [110] zone-axis (as well as its equivalent [100] and [010] zone-axes) and the 2-out-of-3 corresponding variants of 1T′ ($P2_1/m$, a = 0.633 nm, b = 0.3469 nm, c = 1.386 nm, $\alpha = 90°$, $\beta = 93.92°$, $\gamma = 90°$) and T_d ($Pmn2_1$, a = 0.3477 nm, b = 0.6335 nm, c = 1.3889 nm, $\alpha = 90°$, $\beta = 90°$, $\gamma = 90°$) phases. It would be difficult to differentiate the three phases by analyzing the diffraction patterns in this particular orientation within the experimental error. However, 1T′ and T_d phases can be easily differentiated from 2H in appropriate crystallographic orientation. Fig. 3.11(b) shows that all the corresponding patterns of 1T′ and T_d phases produce additional reflections compared with that of 2H in [120] zone-axis, which means that in this particular orientation 1T′ and T_d phases can be differentiated from the 2H phase. As mentioned above (see Fig. 3.7(g, h)), no such additional reflections have been observed in the distorted $2H_d$ region.

The STEM findings strongly suggest that the regions designated as $2H_d$ are the filaments responsible for the LRS with the following structural characteristics: (1) $2H_d$ is a structural derivative of 2H, as can be judged from the similarity of their reciprocal lattices, i.e. electron diffraction patterns, and from a correspondence of van-der-Waals gaps in both structures; (2) the identity of 2H and $2H_d$ elemental compositions suggests that the 2H $\rightarrow$ $2H_d$ transition is polymorphic, with structural changes due to local atomic displacements. In order to understand the $2H_d$ structure, we consider the possibility of its structural relation with the known polymorphs of 2H-$MoTe_2$, i.e. 1T′ and T_d phases, which are both electrically conducting. In fact, T_d phase inclusions have been observed in the 2H matrix (see Fig. 3.9(b)). Hereinafter, we corroborate that the $2H_d$ filament is a transient state representing an incomplete process of switching from 2H to 1T′ or T_d phase structurally.

By a carefully analysis of the distorted atomic images of $2H_d$, we have constructed a P1 structure (see Fig. 3.12(a)) as a derivative of 2H with atomic displacements to match the major zone axes high-resolution images, e.g., in Fig. 3.7(d, f). This P1 structure also gives the diffraction patterns that match experimental NBDs in Fig.

Fig. 3.11. Simulated electron diffraction patterns of 2H, 1T′ and T_d phases. Simulated electron diffraction patterns of 2H phase in (a) [110] zone-axis and (b) [120] zone-axis, together with the patterns of their corresponding variants of 1T′ and T_d phases. Note that 2-out-of-3 patterns of the variants of 1T′ and T_d depicted in (a) show similarity with that of 2H in [110] zone-axis, unlike the [120] zone-axis case depicted in (b).


a
[110]2H
[-110]1T'
[110]1T'
[010]1T'
[1-10]Td
[110]Td
[100]Td
b
[120]2H
[-130]1T'
[130]1T'
[100]1T'
[3-10]Td
[310]Td
[010]Td

3.7(g, h) (see Fig. 3.12(b)). Fig. 3.12(a) lists the crystallographic parameters of the P1 structure derived from matching HAADF images from $2H_d$ regions. The structure represents a change of flat atomic layers of 2H to corrugated ones with a shift of atoms along the c-direction, but without changing the -AbA- stacking sequence. Analysis of the structural models of 1T′, T_d and P1 shows many similarities not only in diffraction patterns, but also in structural projections. With this proposed 2H $\rightarrow$ $2H_d$ $\rightarrow$ 1T′/T_d transition model in mind, we suggest that the $2H_d$ filament is a transient state representing an incomplete process of switching from 2H to 1T′/T_d phase structurally and electronically. Therefore, the distorted $2H_d$ region can be interpreted as a transient state, with atoms displaced from 2H toward one of the lower symmetry structures, with the presence of local 1T′- or T_d-type regions. With a sufficient fraction of such regions in the filament and their inter-connectivity, the electrically conductive pathways, comparable with characteristics of 1T′ and T_d phases, become possible.

3.5 Performance of $Al_2O_3/MoTe_2$ based low programming current RRAMs

For device applications, the LRS resistance should be sufficiently large so that the voltage drop across the interconnects is negligible to ensure proper write/read operation. In addition, the current ratio between the LRS and HRS has to be as large as possible to allow fabricating sizable memory arrays. In this context the above-mentioned performance specs are not ideal and a modified TMD-based memory cell needs to be developed. In order to limit the current through the cell, a tunneling barrier (Al_2O_3) was added into the stack. Fig. 3.13(a) shows multiple I-V measurements on an $Al_2O_3/MoTe_2$ RRAM cell indicating a stable and reproducible memristive switching of this device. Different from the previously discussed $MoTe_2$-only RRAM cells, modified $Al_2O_3/MoTe_2$ stacks immediately transitioned into a LRS when the applied bias reached 2.9 V without the previously observed electroforming process. Moreover, no current compliance through an external circuitry is needed, another de-

Fig. 3.12. P1 model. (a) Crystallographic parameters of the proposed $2H_d$ structure derived from matching HAADF images from $2H_d$ regions, together with detailed projection of the atomic model. The structure represents a change of flat atomic layers of 2H to corrugated, with shift of atoms along the c-direction, but without changing the -AbA- stacking sequence. (b) Simulated diffraction patterns showing 2/3 of the variants of $2H_d$ have similar patterns as that of 2H both in $[110]_{2H}$ and $[120]_{2H}$ zone-axes.

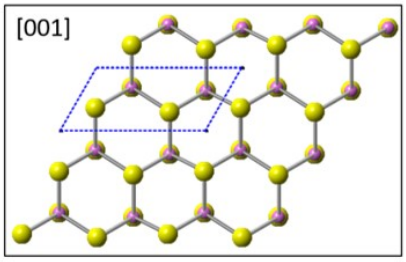
a

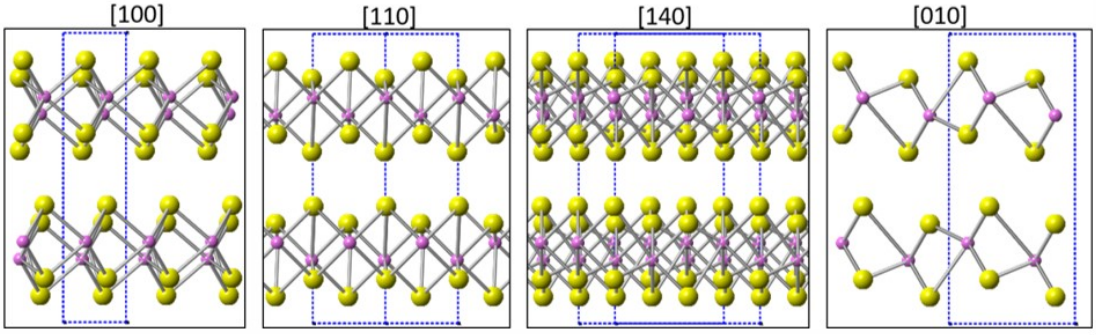
Fractional Coordinates for $2H_d$ unite cell

Unit cell parameters:

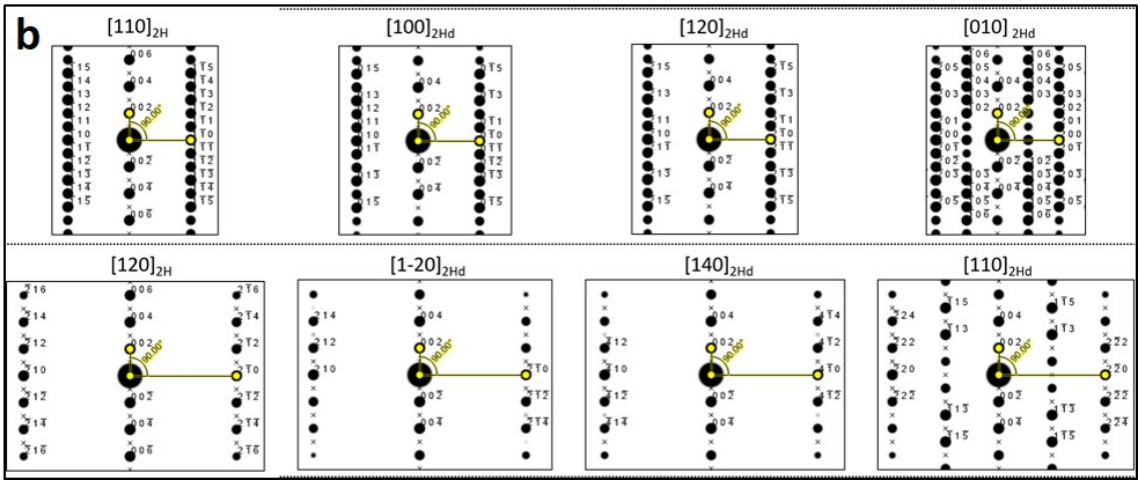
a = 7.038 Å; b = 3.519 Å ;
c = 13.964 Å
α = 90°; β = 90° ; γ = 120°
Space group: P1

Element	X	Y	Z
Mo	0.848300	0.363300	0.720000
Mo	0.151700	0.636700	0.280000
Mo	0.318300	0.303300	0.780000
Mo	0.681700	0.696700	0.220000
Te	0.151700	0.636700	0.655000
Te	0.151700	0.636700	0.905000
Te	0.318300	0.303300	0.155000
Te	0.318300	0.303300	0.405000
Te	0.681700	0.696700	0.595000
Te	0.681700	0.696700	0.845000
Te	0.848300	0.363300	0.095000
Te	0.848300	0.363300	0.345000





b



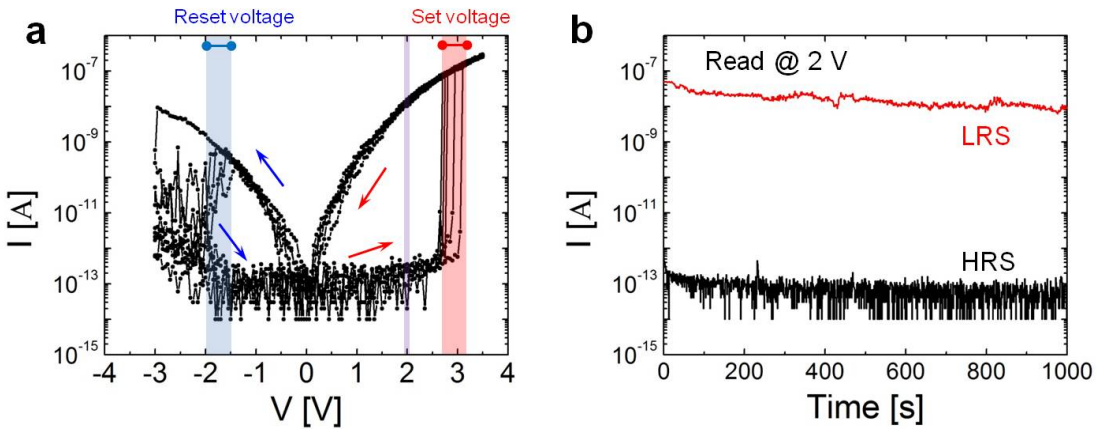


Fig. 3.13. LinPerformance of 2H-Al_2O_3/$MoTe_2$ based RRAM (a) Multiple I-V measurements on a vertical metal-Al_2O_3/$MoTe_2$-metal RRAM cell with a flake thickness of 12 nm and an area of 360 nm x 390 nm. The set voltage is 2.90.25 V and the reset voltage is -1.75±0.25 V. A clear memristive behavior is visible with the arrows indicating the sweep direction. (b) Read disturb measurement of the same RRAM cell at 2 V at room temperature. Copyright © (2019) Springer Nature.

sirable feature in RRAM cells. The stability of the RRAM cell is further underlined through Fig. 3.13(b). The extended stack also gave rise to a much larger current ratio between the LRS and HRS of 10^5 to 10^6 and nonlinearities ($I_{Voperation}/I_{1/2Voperation}$ based on a V/2 scheme) of about 100 for the LRS, and a resistance in the HRS state larger than 10 TΩ (limited by our measurement equipment). The latter is critical for reduced static leakage power consumption and allows increasing the maximum RRAM array size. Moreover, the low current level in the HRS and LRS may eliminate the need for selector devices [58]. All of the above is highlighting the relevance of this structure for sub-1 μA programming currents for selectorless RRAM applications. Notably, Al_2O_3 is one of the early materials that were investigated for RRAM applications. However, in our preliminary testing of vertical Ti/Au/Al_2O_3/Ti/Ni device structures, repeated voltage sweeps did not result in any filament formation and instead led to destructive breakdown at voltages in the 1.35 V range (see Fig. 3.14).

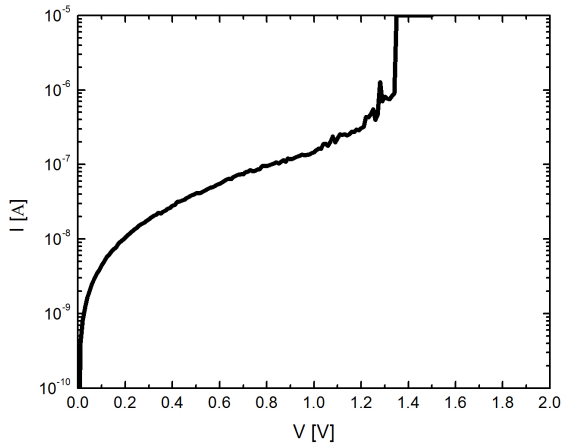


Fig. 3.14. I-V curve of a metal-Al_2O_3-metal device with an area of 330 nm x 400 nm. Note that the Al_2O_3 film breaks down at about 1.35 V. Copyright © (2019) Springer Nature.

While we cannot entirely exclude the possibility of filament formation in the Al_2O_3 layer of the $Al_2O_3/MoTe_2$ stack, the electrical data can be qualitatively understood if filaments are only formed in $MoTe_2$, but do not reach through the Al_2O_3 layer, in this way limiting the LRS conductivity to a much lower, more desirable value of about 10 Mω as compared to the $MoTe_2$-only RRAM cells. In fact, the current levels reached in the LRS of the $Al_2O_3/MoTe_2$ RRAM cell are consistent with the maximum current levels achievable before breakdown in the $Ti/Au/Al_2O_3/Ti/Ni$ stack.

It is apparent that the observed phase transition is unique in that it is reversible and does not involve a change from an amorphous to a crystalline state as in conventional phase change materials (PCMs) [39]. Instead, $MoTe_2$ and $Mo_{1-x}W_xTe_2$ remain crystalline when undergoing the local semiconductor-to-metal transition from a semiconducting 2H to a metallic $2H_d$ phase. In comparison to e.g. VO_2 that can also undergo an insulator-to-metal phase transition under an electric field [59] but requires a hold current and exhibits a unipolar switching behavior, the $MoTe_2$ phase transition reported here is bipolar, nonvolatile and it occurs at room-temperature.

3.6 Conclusion

In this paper, an electric field induced reversible semiconductor (2H)-to-metal ($2H_d$) phase transition in vertical 2H-$MoTe_2$ and $Mo_{1-x}W_xTe_2$ has been achieved experimentally. Conductive filaments were created during electric field application as shown by C-AFM, STM, STS and STEM measurements. Atomic resolution images support that a distorted metallic $2H_d$ phase is created after voltage modification and that this crystalline phase is responsible for the observed RRAM behavior in $MoTe_2$ and $Mo_{1-x}W_xTe_2$. Programming voltages are tunable by the $MoTe_2$ flake thickness and partial substitution of Mo by W in $MoTe_2$ reduces the critical electric field for the phase transition in qualitative agreement with DFT calculations. Our work indicates the possibility to locally and selectively engineer the phases in TMDs by electric fields, and demonstrates the potential of TMDs for novel types of RRAM applications.

3.7 Methods

3.7.1 Devices fabrication and electrical measurement

First a layer of Ti/Au (10 nm/25 nm) which acts as a bottom electrode was deposited onto a 90 nm silicon dioxide (SiO_2) layer located on top of a highly doped silicon wafer. Next, TMD flakes from either (i) $MoTe_2$ (2D Semiconductors and NIST), and (ii) $Mo_{1-x}W_xTe_2$ (NIST) were exfoliated onto this electrode using standard scotch tape technique, followed by a thermal evaporation of 55 nm SiO_2 acting as an insulating layer. The device fabrication was finished by depositing Ti/Ni (35 nm/50 nm) top electrode. For Ti/Au/Al_2O_3/$MoTe_2$/Ti/Ni vertical devices, a 3 nm thick aluminum layer was deposited onto the bottom electrode prior to its oxidation in an oxygen rich environment at 250 °C for 6 h. This process formed a 4.5 nm thick Al_2O_3 layer. Then, $MoTe_2$ flakes were peeled onto the Al_2O_3 covered bottom electrodes. The isolation and top electrode formation were identical to the original process flow discussed above for vertical TMD RRAM devices.

Electrical characterization of the devices was performed at room temperature using a parameter analyzer (Agilent 4156C). A Keysight B1500A semiconductor device analyzer was used for switching speed measurements.

3.7.2 TMDs synthesis and characterization

Both 1T′- and 2H-$Mo_{1-x}W_xTe_2$ crystals (x = 0, 0.03, 0.04, 0.07, 0.09, where x is atomic fraction of W) were produced at NIST using the Chemical Vapor Transport (CVT) method. First, polycrystalline $Mo_{1-x}W_xTe_2$ powders were synthesized by reacting stoichiometric amounts of molybdenum (99.999 %), tungsten (99.9 %) and tellurium (99.9 %) at 750°C in a vacuum-sealed quartz ampoule. Next, $Mo_{1-x}W_xTe_2$ crystals were grown at 950°C to 1000 °C using approximately 1 g of poly-$Mo_{1-x}W_xTe_2$ charge and a small amount of iodine (99.8 %, 5 mg/cm^3) sealed in evacuated quartz ampoules. The ampoules were ice-water quenched after 7 days of growth yielding $Mo_{1-x}W_xTe_2$ crystals in the metallic 1T′ phase. The 1T′-$Mo_{1-x}W_xTe_2$ alloy crystals were then converted to the semiconducting 2H phase by annealing in vacuum-sealed ampoules at 950°C (750°C) for 24 h (72 h) followed by cooling to room temperature at a 10°C/h rate. 2H-$MoTe_2$ crystals were also obtained by CVT growth at 800°C for 140 h using $TeCl_4$ (99.9 %, 5.7 mg/cm^3) as a vapor transport agent. At this temperature, which in accordance with the Mo-Te phase diagram [60] is below 1T′ $\rightarrow$ 2H phase transition temperature, $MoTe_2$ crystals grow directly in the 2H phase.

Crystal structure and composition of $Mo_{1-x}W_xTe_2$ samples were determined by powder X-ray diffraction and energy-dispersive X-ray spectroscopy in SEM, respectively. More detailed information on crystal preparation and characterization can be found elsewhere [61].

3.7.3 Conductive AFM measurement

C-AFM was performed in a Veeco Dimension 3100 AFM system. All AFM images were taken in the contact mode using SCM-PIT tips (Bruker). The conductive tip consists of 0.01 - 0.025 Ω·cm antimony-doped Si coated with PtIr.

3.7.4 TEM/STEM structural characterization

FEI Nova NanoLab 600 DualBeam (SEM/FIB) was employed to prepare cross-sectional TEM samples. Electron-beam induced deposition of 1 μm thick carbon was initially deposited on top of the device to protect the samples surface, then followed by 2 μm ion-beam induced Pt deposition. To reduce Ga-ions damage, in the final step of preparation the TEM samples were thinned with 2 kV Ga-ions using a low beam current of 29 pA and a small incident angle of 3 degree. An FEI Titan 80-300 probe-corrected STEM/TEM microscope operating at 300 keV was employed to acquire both nano-beam diffraction patterns and TEM images in TEM mode as well as atomic-resolution high-angle annular dark field (HAADF) images in STEM mode.

4. AN ULTRA-FAST MULTI-LEVEL $MOTE_2$-BASED RRAM

We report multi-level $MoTe_2$-based resistive random-access memory (RRAM) devices with switching speeds of less than 5 ns due to an electric-field induced 2H to $2H_d$ structural transition. Different from conventional RRAM devices based on ionic migration, the $MoTe_2$-based RRAMs offer intrinsically better reliability and control. In comparison to phase change memory (PCM)-based devices that operate based on a change between an amorphous and a crystalline structure, our $MoTe_2$-based RRAM devices allow faster switching due to a transition between two crystalline states. Moreover, utilization of atomically thin 2D materials allows for aggressive scaling and high-performance flexible electronics applications. Multi-level stable states and synaptic devices were realized in this work, and operation of the devices in their low-resistive, high-resistive and intrinsic states was quantitatively described by a novel model.

4.1 Introduction

RRAM has promises of being an emerging technology due to its potential scalability, high operation speed, high endurance and ease of process flow. However, reliable and repeatable operation is a potential challenge in future applications since switching involves the uncontrollable motion of individual atoms. In this work, we present a new switching mechanism for $MoTe_2$-based RRAM. An electric field induces the

structural transition from the stable semiconducting 2H phase to a more conductive $2H_d$ state, which provides a potential path towards better stability. The newly formed $2H_d$ is structurally close to the 2H phase, which holds the promise for faster switching if compared with the significant migration of ions in conventional RRAM [18] or the amorphous-to-crystalline transition in PCM [39] (see Fig.4.1). Initial pulse measurements show impressive switching speed of less than 5 ns. Moreover, multi-level states can be programmed into the devices by applying proper set/reset voltages, which allows for gradually changing the device resistance with multiple pulses, creating a synaptic device.

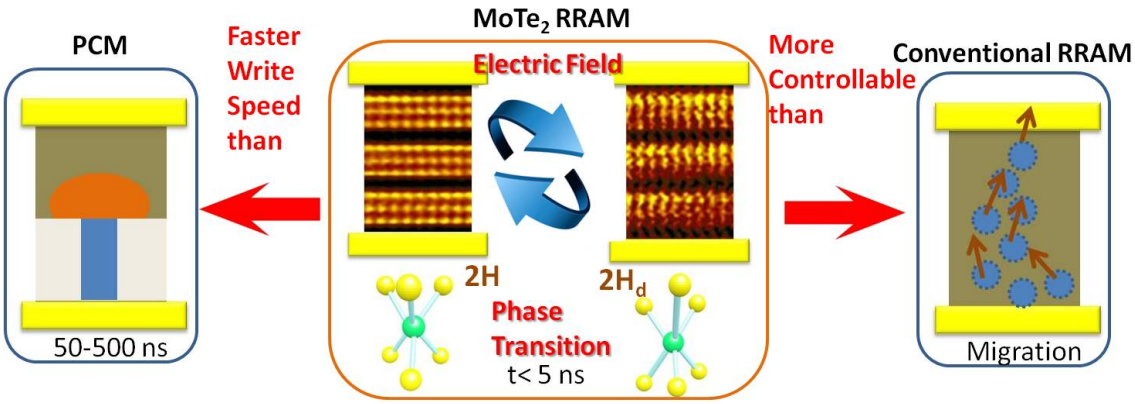


Fig. 4.1. Highlight features of the $MoTe_2$ based RRAM. Copyright © (2018) IEEE.

4.2 Switching in $MoTe_2$ RRAM devices

Fig. 4.1 illustrates the advantages of this new type $MoTe_2$-based RRAM as compared to conventional RRAM and PCM due to switching by an electric-field induced structural transition. Fig. 4.2(a) shows schematically a vertical $MoTe_2$ device. First, a bottom electrode Ti/Au (10 nm/25 nm) was deposited onto a 90 nm silicon dioxide (SiO_2) layer covering a highly doped silicon wafer. Next, $MoTe_2$ (2D Semiconductor)

layers were exfoliated onto this electrode using standard scotch tape techniques, followed by thermal evaporation of 55 nm SiO_2 insulating layer. The device fabrication was finished by the deposition of a Ti/Ni (35 nm/50 nm) top electrode. Different from previously reported CVD grown 2D material based RRAM devices whose operation is mediated by uncontrollable defects/grain boundaries in the device structure [47, 63], our active material is a single-crystalline layer, where the observed RRAM behavior is due to the intrinsic properties of $MoTe_2$. Fig. 4.2(b) shows an AFM image of a $MoTe_2$ vertical device. The active region is about 0.1 μm^2. Fig. 4.3(a) displays I-V curves of a pristine device, the device forming process and successive cycling through its high resistive state (HRS) and low resistive state (LRS). Stable and reproducible bipolar RRAM behavior was observed. Fig. 4.3(b) shows the I-V curves for $MoTe_2$ devices with different layer thicknesses, and Fig. 4.3(c) summarizes how the forming and set voltages scale with the $MoTe_2$ layer thickness.

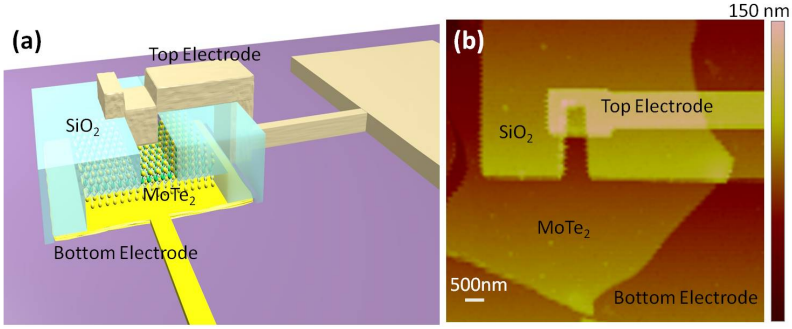


Fig. 4.2. Highlight features of the $MoTe_2$ based RRAM. Copyright © (2018) IEEE.

Thermoreflection microscope images were acquired to map the location of the filament on the device after forming. Surface temperature maps with 50 mK temperature resolution and submicron (diffraction limited) spatial resolution can be acquired within a few minutes. Fig. 4.4(a) and (b) show self-heating hotspots on the nickel electrode surface superimposed with optical images for two representative devices, indicating the position of the filaments. The occurrence of a single hotspot for each

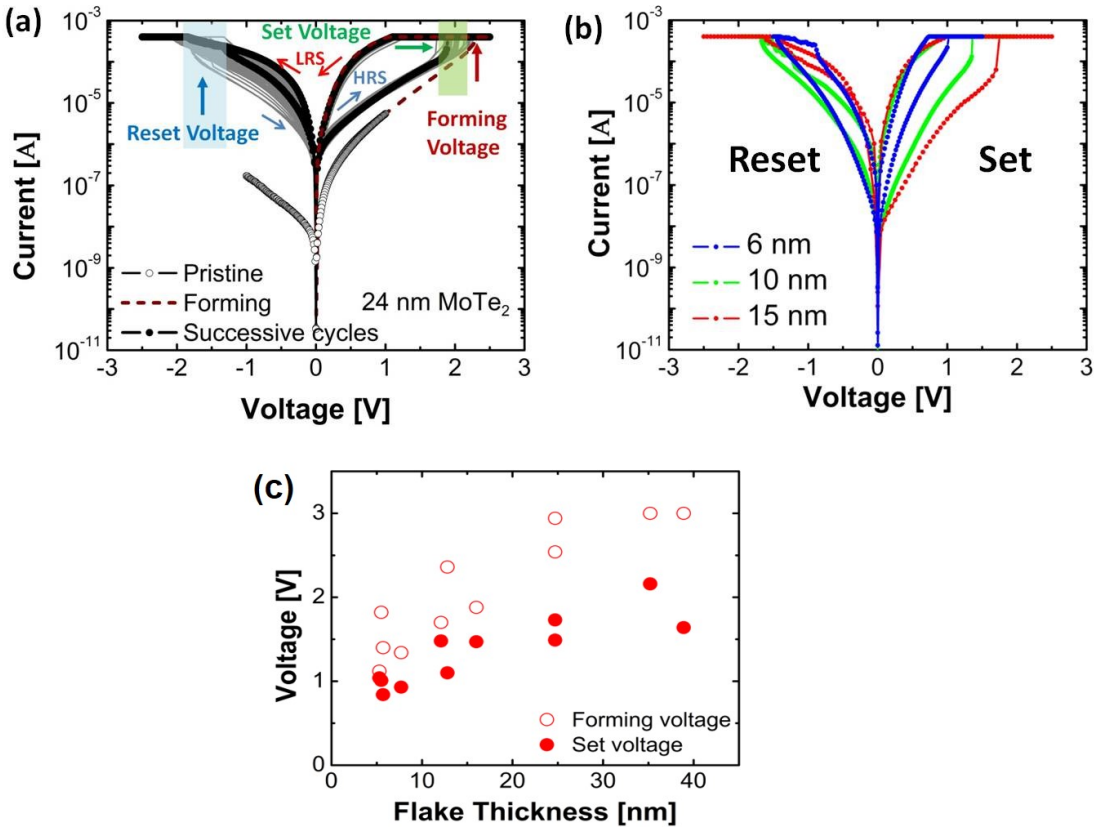


Fig. 4.3. (a) I-V curves of a 24 nm $MoTe_2$ device with an active area of 330 nm x 500 nm. 40 cycles are shown in the grey line curves. Current compliance is set to 400 μA. (b) I-V curves of vertical $MoTe_2$ RRAM devices from 6 nm, 10 nm, and 15 nm $MoTe_2$ layers with active areas of 502 nm x 360 nm, 522 nm x 330 nm and 500 nm x 330 nm respectively. (c) Forming/Set voltage values scale with the $MoTe_2$ thickness.

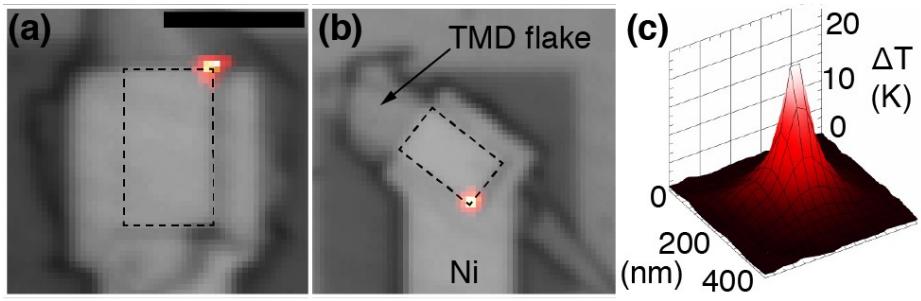


Fig. 4.4. (a-b) Thermoreflectance images showing the location of the filament. The scale bar is 5 μm. (c) The calibrated temperature change map for the filament in the device (b). Copyright © (2018) IEEE.

device with characteristic hotspot full-width-at-half-maximum of ∼200 nm is consistent with joule self-heating from a source as small as a $MoTe_2$ filament. In six out of eight devices imaged the hotspot was located at the edge or corner of the active region as can be seen in Fig. 4.4(a) and (b). We speculate that this preferential occurrence is a result of stronger electric fields at sharp topological features due to patterning during the fabrication that enhances the filament formation. Fig. 4.4(c) shows the calibrated temperature change map for the hotspot in device (b). The detected temperature change on the filament portion is ∼15 K.

In order to understand the filament formation mechanism in $MoTe_2$, scanning transmission electron microscopy (STEM) of cross-sectional samples was utilized. As Fig. 4.5 shows, in the LRS, a distorted 2Hd state was identified in the regions extending vertically throughout the $MoTe_2$ layer. The $2H_d$ state was identified as a distorted modification of the 2H structure a transient state with atoms displaced to the sites of a lower symmetry, but still within atomic arrangements of the 2H structure. A detailed analysis of the structure can be found in ref. [33]. Fig. 4.6 shows an energy dispersive spectrometry (EDS) scan along the filament region of a device in its LRS. Almost no Ti and Au signals were detected within the filament, which in particular when also considering the unavoidable ion-milling contamination during FIB sample preparation implies that the switching mechanism is not related

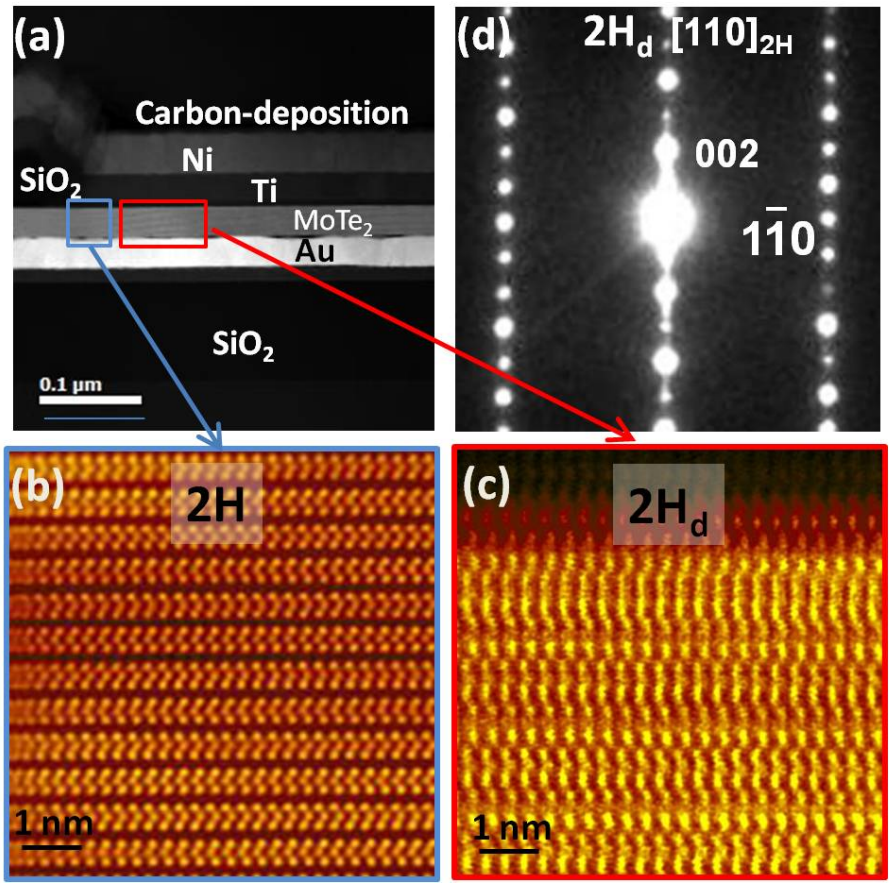


Fig. 4.5. (a) HAADF-STEM image showing the cross-section of a $MoTe_2$ device. Higher magnification HAADF image from the region defined by the blue/red box in (a) showing (b) 2H and (c) a distorted structure ($2H_d$) taken along the $[110]_{2H}$ zone-axis. (d) Corresponding nano-beam diffraction pattern taken from the distorted $2H_d$ area.

to the migration of metal ions. To further confirm this point, graphene was used to replace the metal top and bottom electrodes. Fig. 4.7 shows the typical bipolar RRAM behavior observed here in a Graphene-$MoTe_2$-Graphene device. Note that this is the first demonstration of an entirely 2D materials structural transition based RRAM. Based on previous studies, graphene is a good diffusion barrier for metal ions. This 2D RRAM excludes completely the possibility of migration of metal ions as a source for the resistive switching observed by us. Based on these results, an electric-field induced structural transition from 2H to a more conductive 2Hd state is believed to be responsible for the RRAM behavior in vertical $MoTe_2$ devices.

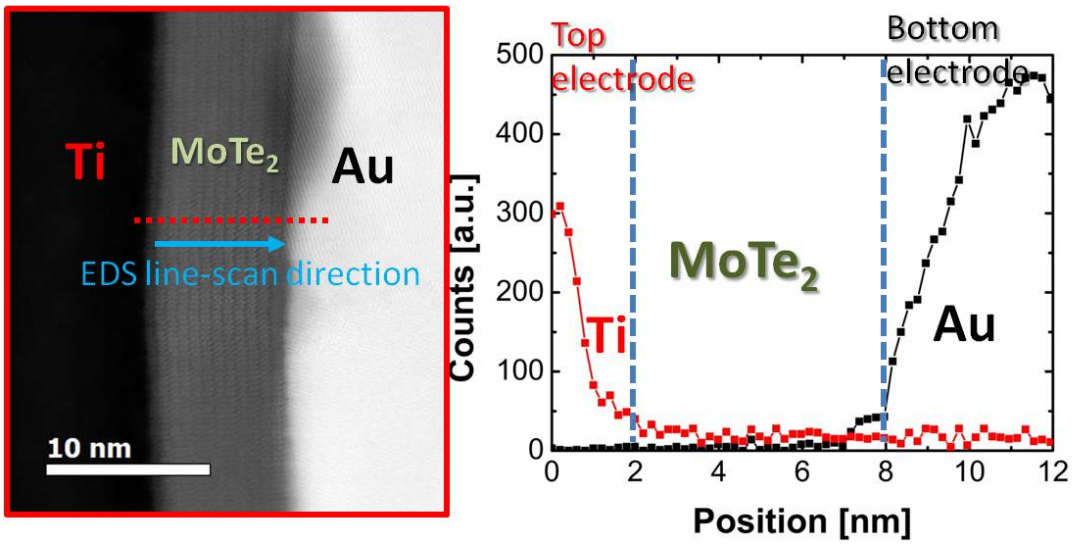


Fig. 4.6. EDS line-scan analysis of the filament region of a device in its LRS. Little Ti/Au signals were detected in the filament region due to ion-milling contamination during sample preparation. Copyright © (2018) IEEE.

4.3 A physical model

To fully understand the vertical transport through the pristine, LRS and HRS states in $MoTe_2$ devices and to explore the properties of the new $2H_d$ state, a physical

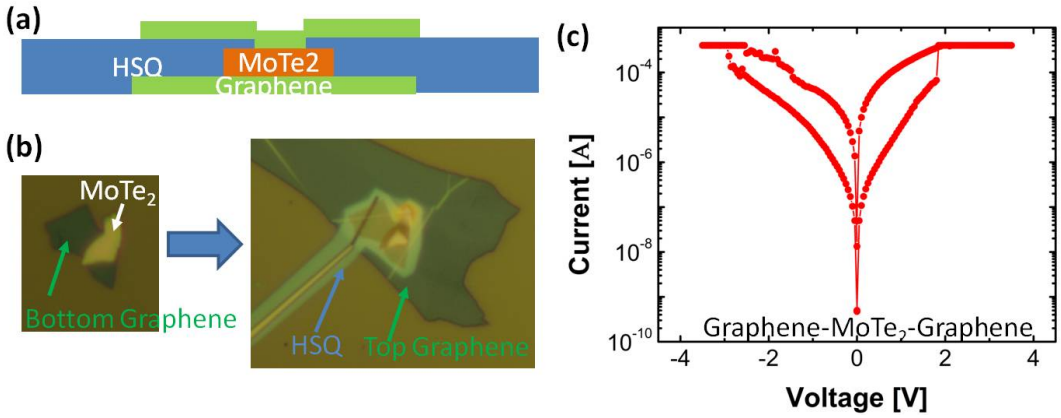


Fig. 4.7. (a) Schematic and (b) optical images of a Graphene-$MoTe_2$-Graphene device. (c) I-V curve of the RRAM device in (b). Copyright © (2018) IEEE.

model was constructed. The barrier height Φ_{2H} and $2H_d$ shown in figure 4.8 were extracted by utilizing the numerical model from ref. [8]. In this model, two different transport mechanisms are considered: thermal diffusion at low voltages and Fowler-Nordheim (FN) tunneling at higher voltages, as illustrated for a pristine data set in Fig. 4.8(b). In our model the 2H phase has a larger barrier height than the $2H_d$ state as evident when their current values in the low voltage range are compared. An excellent fit can be obtained for the pristine I-V characteristics (Fig. 4.8(b)), as well as for the LRS and HRS (Fig. 4.8(c)) by employing the band diagrams and parameters shown in Fig. 4.8(a). In the pristine state, the $MoTe_2$ is in its 2H phase with a large barrier height of $\Phi_{2H} = 0.38$ eV. On the other hand, in the LRS, a filament of $2H_d$ was created through the setting process with an extracted barrier height of Φ_{2Hd}= 0.07 eV. The HRS is characterized by formation of the $2H/2H_d$ heterojunction due to rupture of the $2H_d$ filament during the reset process. The thickness of newly formed 2H segment in the filament can be estimated to be ∼1.8 nm. Thus, the simulation results are consistent with the notion that a new semiconducting $2H_d$ state with a

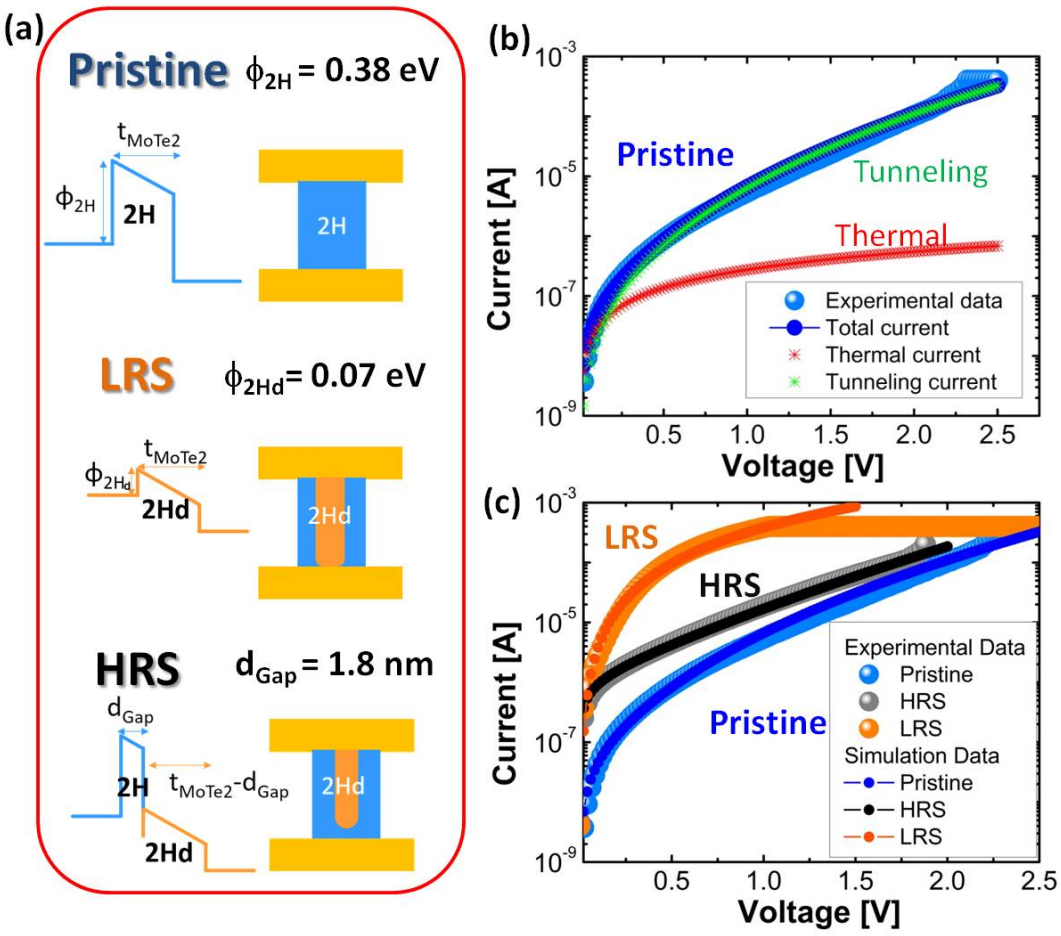


Fig. 4.8. (a) Schematic band diagrams of the RRAM in its various states. (b) Experimental and simulation data of a pristine device. (c) Experimental and simulation data for the LRS, HRS and pristine state. Copyright © (2018) IEEE.

smaller barrier height is formed during the set process that is responsible for the higher conductivity of the LRS compared with the HRS.

4.4 Performance study

Fig. 4.9 illustrates the pulse switching behavior in $MoTe_2$ based RRAM devices. The pulse width is 80 s. By applying set/reset pulses, the device can switch between

the LRS and HRS. Fig. 4.9(c) shows the read out current per cycle in the LRS and HRS. Fig. 4.9(d) is a retention measurement. All performance studies indicate stable and reproducible RRAM behavior. In order to test the high temperature retention

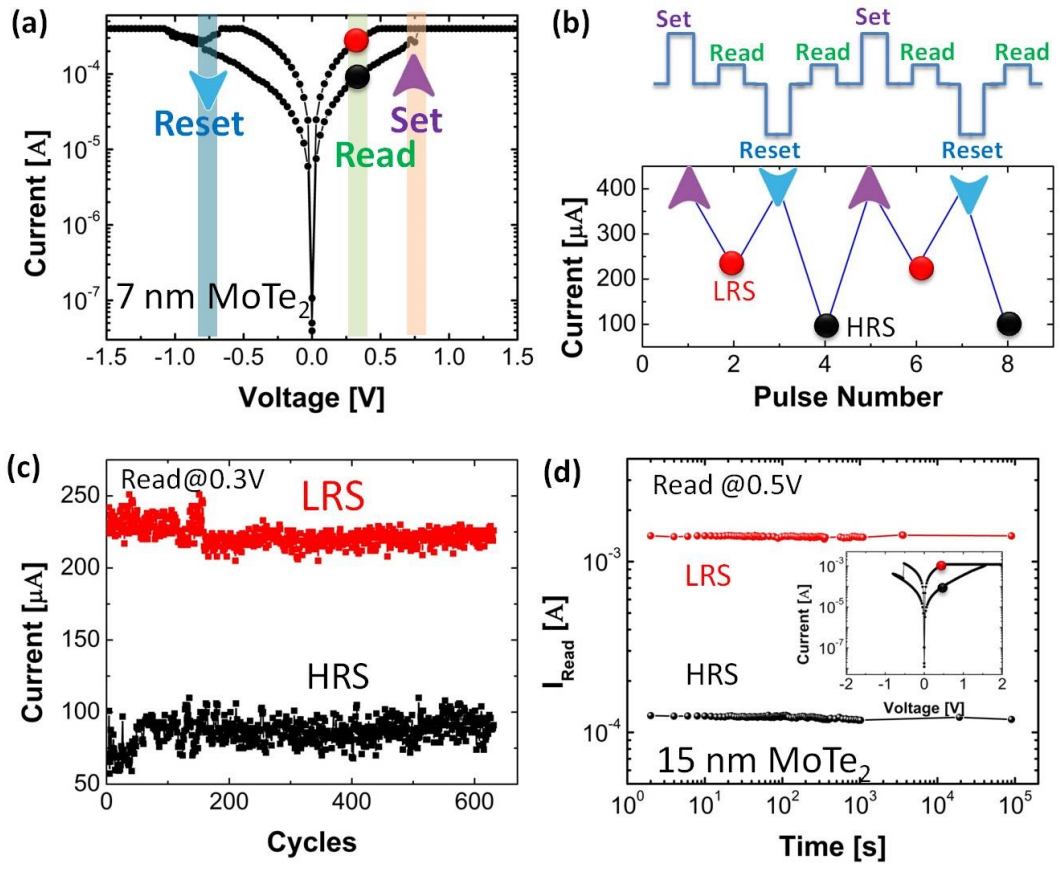


Fig. 4.9. (a) DC characteristic of a 7 nm thick $MoTe_2$ layer RRAM device. (b) shows the various current levels after pulse switching. (c) Current versus cycle in the LRS and HRS at a read voltage of 0.3 V. Current compliance is set to 400 μA. (d) Retention of the HRS and LRS for a 15 nm thick $MoTe_2$ RRAM device. Current compliance is set to 1.2 mA. Copyright © (2018) IEEE.

properties of the $2H_d$ structure, devices were set to their LRS, and annealed and read at 400 K. An exemplary result is shown in Fig. 4.10(a). 6 devices were monitored - none of them showed a change of resistance when annealed at 400 K for 24 h,

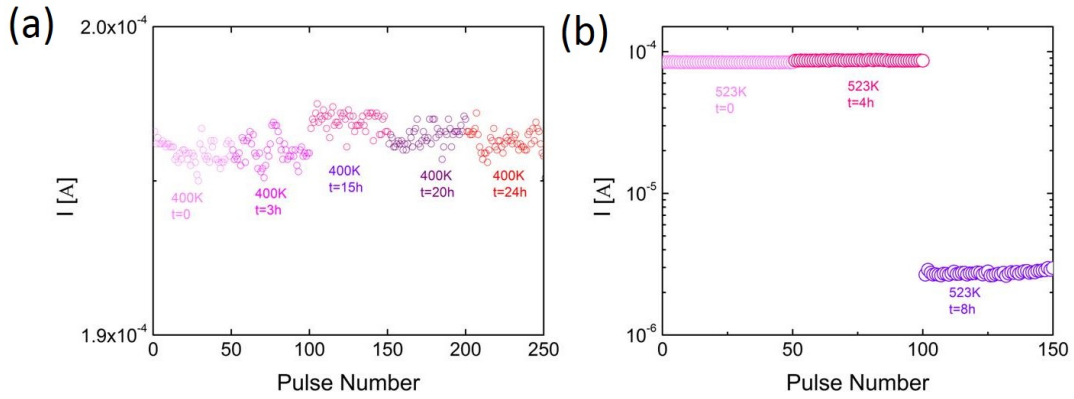


Fig. 4.10. (a) DC characteristic of a 7 nm thick $MoTe_2$ layer RRAM device. (b) shows the various current levels after pulse switching. (c) Current versus cycle in the LRS and HRS at a read voltage of 0.3 V. Current compliance is set to 400 μA. (d) Retention of the HRS and LRS for a 15 nm thick $MoTe_2$ RRAM device. Current compliance is set to 1.2 mA. Copyright © (2019) Springer Nature.

indicating the $2H_d$ structure is stable at 400 K. Next, these devices were annealed at 523 K (250 °C) (Fig. 4.10(b)), and re-measured at room temperature. After 8 h of annealing, 3 out of 6 devices dropped back to their HRS, which indicates that the $2H_d$ is not stable at these elevated temperatures. Thermal perturbation at 523 K made the $2H_d$ phase back to 2H.

4.5 Pulse Measurements

To test the switching speed of our $MoTe_2$ RRAM devices, the experimental measurement setup shown in the inset of Fig. 4.11(b) was utilized. The current through the device was measured using a 50 Ω termination at the oscilloscope [64]. Note that no current compliance was used in this setup. The switching was controlled by varying the pulse width or pulse amplitude. A current and voltage versus time (t) plot of one such SET operation is shown in Fig. 4.11(a). The full width at half max

(FWHM) of the applied voltage pulse is 5 ns. Fig. 4.11(b) shows the same data as in Fig. 4.11(a) but plotted as the current versus voltage. This clear change in resistance during the 5 ns voltage pulse is further evidence that the switching speed in $MoTe_2$ based RRAM is less than 5 ns.

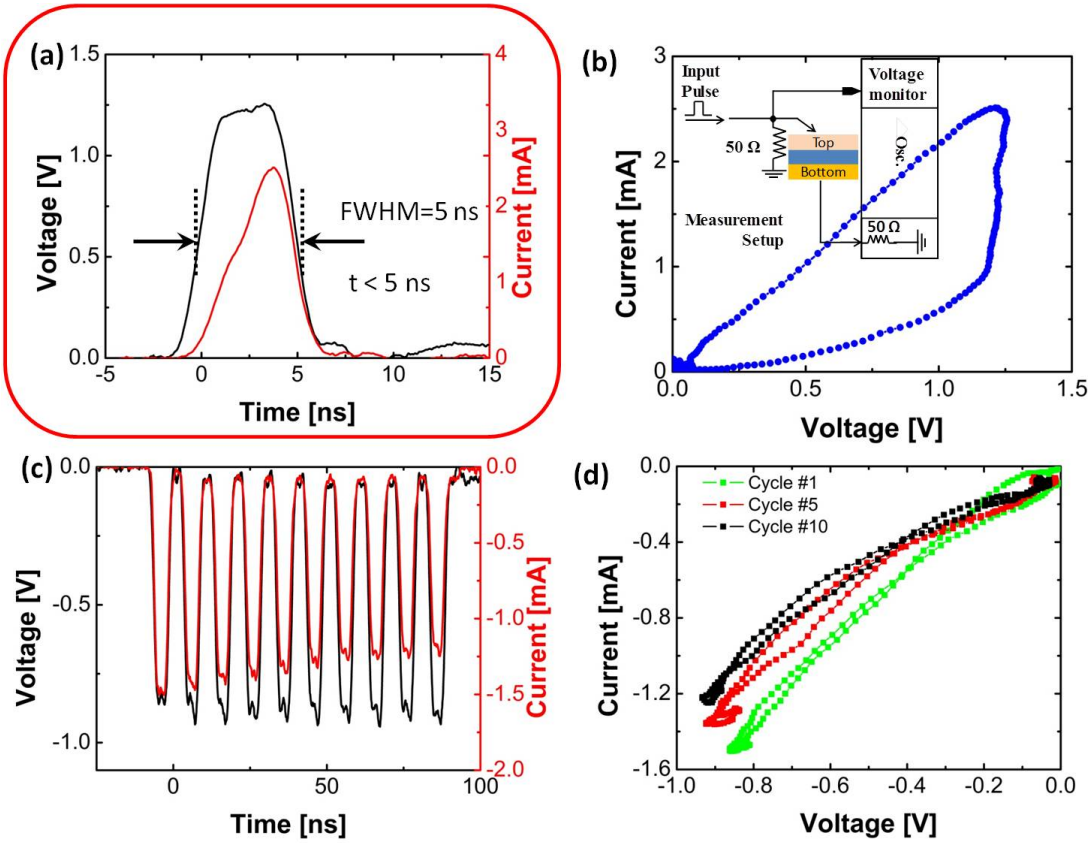


Fig. 4.11. (a) I/V vs. time plot showing switching of the device within a 5 ns voltage pulse. (b) I-V plot of the data shown in (a) to show the change in resistance during the applied pulse. The inset figure displays the experimental setup for the pulse measurement. (c) I/V vs. t plot of 10 reset pulses. (d) I-V plot of data plotted in (c) of pulses 1, 5 and 10. Copyright © (2018) IEEE.

The devices were reset (switched OFF) using negative pulses. Multiple pulses were required for a gradual reset process. Fig. 4.11(c) shows 10 pulses used to reset the device. Current versus voltage plots of cycle 1 (1st pulse), cycle 5 (5th pulse) and

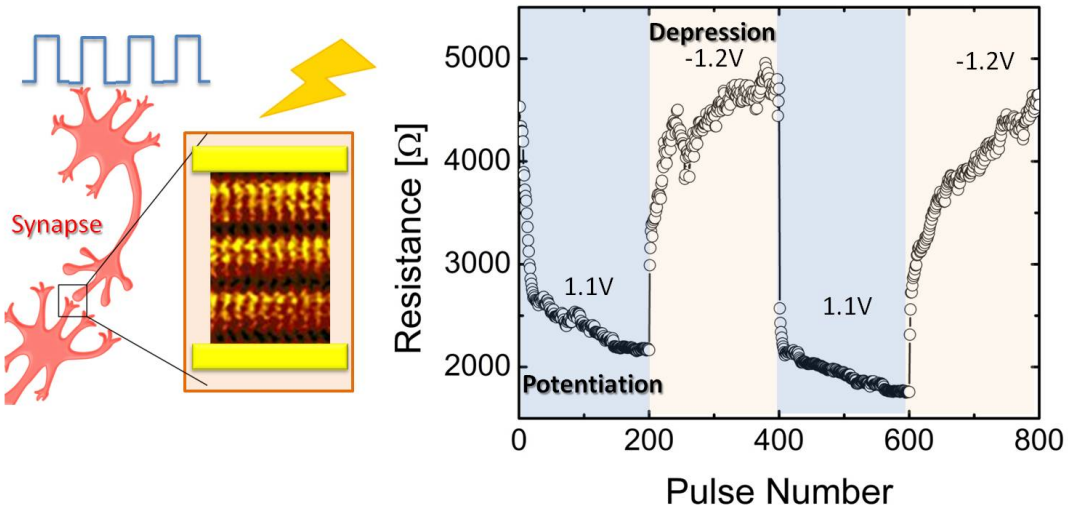


Fig. 4.12. Synaptic device from an $MoTe_2$ RRAM. Copyright © (2018) IEEE.

cycle 10 (10th pulse) are shown in Fig. 4.11(d). The gradual resistance change is a desirable feature for neuromorphic computing. Fig. 4.12 shows the characteristics of a device that was programmed by a series of positive pulses (1.1 V, 80 μs) followed by a series of negative voltage pulses (-1.2 V, 80 μs). The resistance of the $MoTe_2$ device gradually decreased and increased, which is similar to the potentiation and depression of biological synapses.

By carefully tuning the set/reset voltages, multi-level states can be programmed into the devices. Fig. 4.13(a) shows stable resistive states after various short (80 μs) and long (560 μs) voltage pulses that were read at a 0.2 V level. Long pulses result in a more substantial change (training) of the resistive state of the system. Fig. 4.13(b) shows the switch on/off behavior in each state. All the pulse measurements hint at an additional application space of this class of vertical TMD devices in the realm of neuromorphic computing.

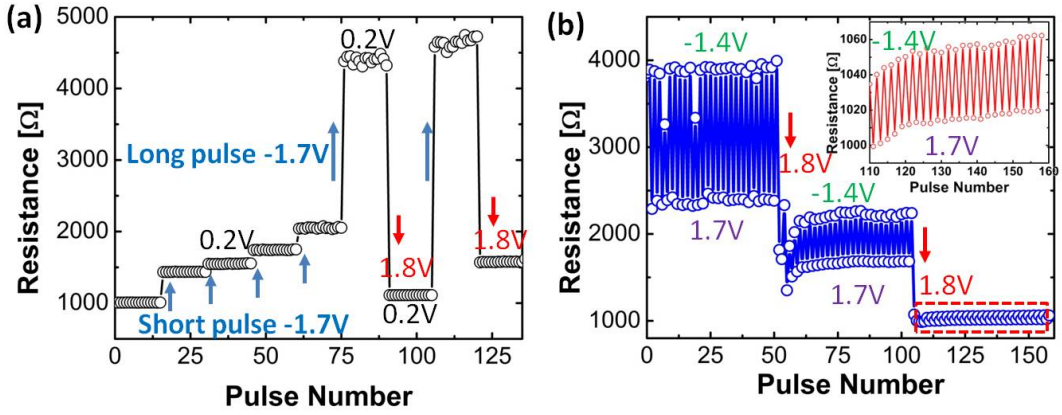


Fig. 4.13. (a) Multiple stable states of a device after various set and reset voltage pulses had been applied. Read out occurs at a voltage of 0.2 V. Every state is characterized by 15 subsequent read outs. A short pulse (80 μs) and longer pulse (560 μs) of a reset voltage of -1.7 V result in different changes of the resistance. (b) Multi-level characteristics of a vertical $MoTe_2$ device. Each level exhibits stable switch on/off at set/reset voltages of 1.7 V and -1.4 V respectively. A third state can be dialed in through yet another 1.8 V pulse. The inset figure is the zoom-in of the red dashed part. Copyright © (2018) IEEE.

4.6 Conclusion

Multi-level $MoTe_2$-based RRAM devices with switching speeds of less than 5 ns were achieved. The switching mechanism is an electric-field induced 2H to $2H_d$ structural transition. Compared with the conventional RRAM, which depends on the uncontrollable motion of metal ions or oxygen vacancies, $MoTe_2$-based RRAM devices offer intrinsically better reliability and control, structural transition switched by electric field; Compared with phase change memory, which changes between amorphous and crystalline structure, $MoTe_2$-based RRAM devices switch between two crystalline structures, allowing for faster switching speed. Moreover, the atomic thin nature of 2D material fundamentally provide the possibility for aggressive scaling, making it

even appealing in the real application. The synaptic behaviors in the $MoTe_2$ device also show the great potential in the neuromorphic computing.

5. TUNABILITY OF SHORT-CHANNEL EFFECTS IN MOS_2 FIELD EFFECT DEVICES

MoS_2 transistors have been electrically characterized and analyzed in terms of their vulnerability to short channel effects and their response to various environments. We find that the electrical performance of MoS_2 flakes is governed by an unexpected dependence on the effective body thickness of the device which in turn depends on the amount of intercalated water molecules that exist in the layered structure. In particular, we observe that the doping stage of a MoS_2 field-effect transistor (FET) strongly depends on the environment (air/vacuum). Most importantly, our results indicate that device characteristics of MoS_2 can be substantially impacted by tuning the device electrostatics. This can be accomplished by controlling the effectively active body thickness of the MoS_2 FET employing intercalation and engineering of the effective barrier between individual MoS_2 layers.

5.1 Introduction

MoS_2 transistors have been electrically characterized and analyzed in terms of their vulnerability to short channel effects and their response to various environments. We find that the electrical performance of MoS_2 flakes is governed by an unexpected dependence on the effective body thickness of the device which in turn depends on the amount of intercalated water molecules that exist in the layered structure. In particular, we observe that the doping stage of a MoS_2 field-effect transistor (FET)

strongly depends on the environment (air/vacuum). Most importantly, our results indicate that device characteristics of MoS_2 can be substantially impacted by tuning the device electrostatics. This can be accomplished by controlling the effectively active body thickness of the MoS_2 FET employing intercalation and engineering of the effective barrier between individual MoS_2 layers. In order to evaluate the occurrence of short-channel effects (SCEs) in any device structure, characteristic length scales that determine the electrostatics gate control and the actual channel length L (the gated segment of the device) have to be compared. In a bulk device this typically implies comparing a doping dependent screening length $\lambda_{bulk} = \sqrt{\frac{\varepsilon_{body-x}}{\varepsilon_{ox}} W_{DM} t_{ox}}$ with the channel length [66].Here W_{DM} denotes the maximum doping dependent depletion width, t_{ox} the gate dielectric thickness, ε_{ox} the value of the dielectric constant of the gate oxide, and ε_{body-x} the dielectric constant (in direction of the transport direction) of the channel material used. Typically, L has to be a few (3-6) times larger than the characteristic length scale λ_{bulk} in order for short channel effects to be suppressed. The situation is different however in an ultra-thin body structure like a transition metal dichalcogenide (TMD) field-effect transistor (FET). Here λ_{bulk} is replaced by $\lambda_{TMD} = \sqrt{\frac{\varepsilon_{TMD-x}}{\varepsilon_{ox}} t_{TMD} t_{ox}}$ if the channel thickness t_{TMD} (the total layer thickness involved in transport) becomes smaller than the doping related depletion width W_{DM}. In other words, the electrostatics in the channel are always determined by the smaller of t_{TMD} and W_{DM} making few layer TMD devices a viable choice for aggressively scaled FETs even without the introduction of doping in the channel [67, 68].

What makes the situation in case of TMDs more complicated than for many other ultra-thin body devices like nanowires and nanotubes is their layered structure. We had pointed out that the on-state performance in MoS_2 depends on the details of where the current flows in a few layer device [67]. Here we discuss how short-channel effects and MoS_2 FETs scaling properties are significantly impacted by their environment (see in this context also references [69–72]). Based on our findings and the common understanding that intercalation is a prominent phenomenon in layered MoS_2 [73, 74], we submit that water molecules in the air can diffuse in between the

individual layers of the MoS_2 device, resulting in a) *p-doping* [75] and b) *a decrease in the effective body thickness of the layer stack*. The experimental evidence provided here for the first time is consistent with this picture, indicating an opportunity to tune device characteristics of MoS_2 substantially by impacting the environment of the structure.

5.2 Device fabrication and experimental results

A large number of back-gated MoS_2 FETs with different channel lengths have been fabricated on flakes with various thicknesses. In many instances the same flake was used to create channels with different L to ensure a reliable comparison between device data. Fig. 5.1(a) shows an optical and an SEM image of back-gated MoS_2 FETs on an 8.2 nm thick flake, exfoliated onto a 90 nm silicon dioxide (SiO_2) substrate with underlying highly doped silicon using standard scotch tape techniques. For all devices the layer thickness has been determined by atomic force microscopy (AFM). Flake thicknesses varied between 1.2 nm and 30 nm for channel lengths between 100 nm and 1.4 μm. In total 125 devices were characterized. Fig. 5.1(b) displays the device structure schematically. Ni (65 nm) was used to create source/drain contacts employing e-beam lithography, metal deposition and conventional lift-off.

Electrical characterization of the devices was performed at room-temperature using a parameter analyzer. We first focus on the impact of layer thickness on the subthreshold characteristics ($\log[I_{ds}]$-V_{gs}) by examining MoS_2 FETs with different channel lengths on the same flake in air. Fig. 5.2(a) shows the typical gate and drain voltage dependence of devices that are under gate control, i.e. devices that do not show short-channel effects (SCEs) that are associated with the drain field impacting the electrostatics in the device. The exponential change of current in the off-state (below threshold) and the power law dependence in the on-state (above threshold) are clearly visible as a function of gate voltage. Independent of L, the $t_{body} = 8.7$ nm thick device shows the behavior of a well-tempered device in air. For thicker flakes

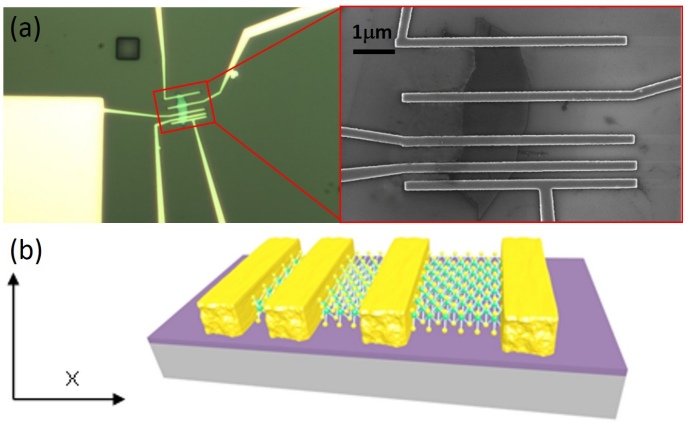


Fig. 5.1. (a) Optical and SEM images and (b) 3-D cartoon of back-gated MoS_2 FETs with different channel lengths. Copyright © (2014) American Chemical

however, devices with very similar channel length show a different behavior once L becomes sufficiently small. In fact, flakes with a thickness t_{body} = 13.3 nm show a strong drain voltage dependence in the device off-state for L = 245 nm. At the same time the gate loses control and can no longer turn the device entirely off. This behavior is consistent with the above discussion about $\lambda_{TMD} = \sqrt{\frac{\varepsilon_{TMD-x}}{\varepsilon_{ox}} t_{TMD} t_{ox}}$ becoming too large in comparison with L for large enough t_{TMD}-values and reported here for the first time. Since the geometric screening length λ_{TMD} in comparison with the channel length L defines the onset of SCEs, for undoped (or lowly doped) channels, a $L^2 \propto t_{TMD}$ dependence is expected to define the transition between devices with and without SCEs (As will be discussed, t_{body} and t_{TMD} are not identical but instead denote the physical flake thickness and the electrically active thickness of the TMD respectively). Considering in addition a finite doping level one would expect that for t_{TMD}-values larger than W_{DM}, which is inversely proportional to the square of this doping level (see equation (1) below) [76], the transition between SCEs and no-SCEs is no longer flake thickness dependent. Fig. 5.3 summarizes our expectations based on these arguments.

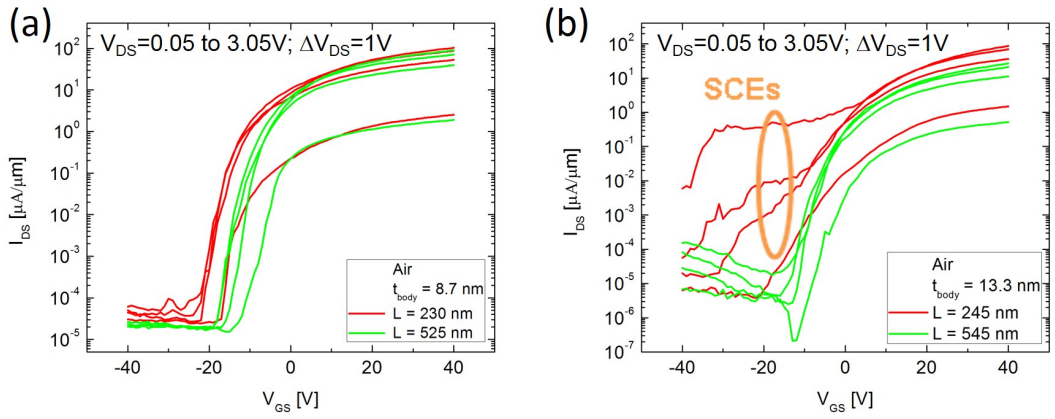


Fig. 5.2. Transfer characteristics measured in air for (a) a 8.7 nm thick and (b) a 13.3 nm thick back-gated MoS_2 FET for different channel lengths. SCEs show a typical L and t_{TMD} dependence. Copyright © (2014) American Chemical

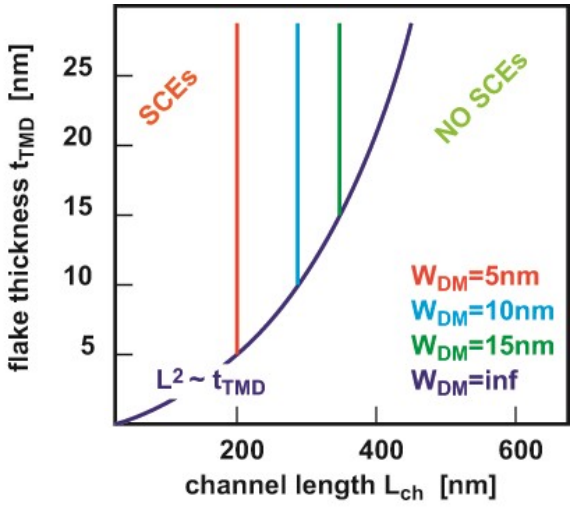


Fig. 5.3. Schematic of expected transition between short-channel and NO short-channel effects in TMD FETs with different body (flake) thickness, channel length and doping related maximum depletion width W_{DM}. Copyright © (2014) American Chemical

Next, we have performed the same set of measurements under vacuum conditions. For this purpose the probe station was pumped to a pressure of about 2.3 $\times 10^{-6}$ torr.

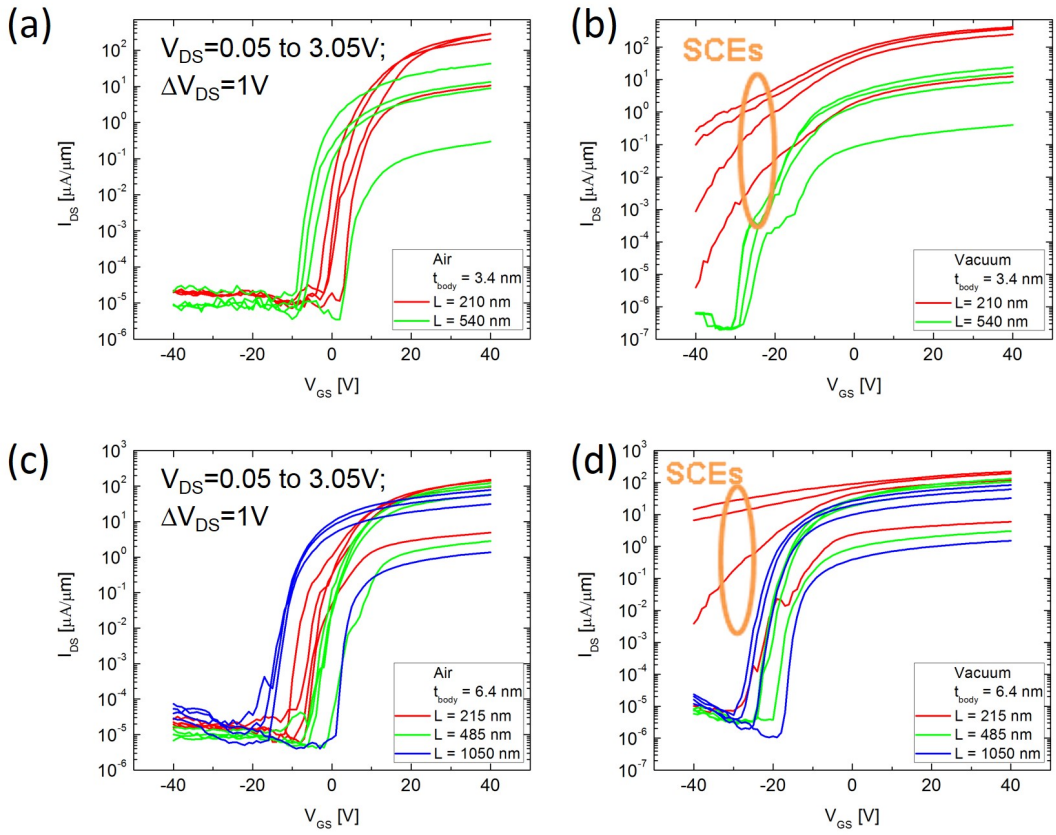


Fig. 5.4. Transfer characteristic of (a), (b) 3.4 nm and (c), (d) 6.4 nm thick back-gated MoS_2 FETs with different channel lengths. (a), (c) measured in air and (b), (d) measured in vacuum. SCEs are more pronounced in vacuum if compared to air. Copyright © (2014) American Chemical

Interestingly, the electrical measurements did not show the same behavior under vacuum as they did in air. In fact, different from many nano-devices that show improved device characteristics when the impact of moisture in the air is eliminated [77–80], MoS_2 FETs show deteriorated off-state characteristics in vacuum if compared to their counterparts in air. Fig. 5.4 shows a direct comparison of a number of different devices. Note that the film thicknesses and channel lengths chosen do not show any SCEs in air (a) and (c). On the other hand a clear signature of short channel effects

can be observed for the 3.4 nm and the 6.4 nm thick MoS_2 devices for the shortest channel lengths in vacuum Fig. 5.4(b) and (d) indicating that the electrostatics in the device have been substantially altered without changing the device geometry. This curious observation has, to the best of our knowledge, never been reported before. It is NOT a result of device-to-device variations or non-reproducible device characteristics but instead, as we will argue below, a result of the modified electrostatic conditions in a MoS_2 FET due to the intercalation of water molecules. We also submit that our observation should not be limited to H_2O but is expected to be visible also for other substances that can result in intercalation in the case of MoS_2.

Fig. 5.5 summarizes our experimental observations for all devices in air and in vacuum. Green data points indicate the absence of SCEs, red dots the presence of SCEs. The expected general trend of NO SCEs for long channel lengths L and thin flakes is clearly observed for both, measurements in air and vacuum. However, Fig. 5.5 also reveals a clear difference between devices that are characterized in air and those that were measured in vacuum. As discussed in the context of Fig. 5.4, SCEs are apparent in vacuum at smaller channel lengths L for a given film thickness if compared with devices in air. Before we start analyzing the experimental data quantitatively, it is useful to take a closer look at the device characteristics in air and in vacuum in terms of their respective threshold voltages. Fig. 5.6(a) shows representative results obtained for a flake with a thickness of 4.7 nm as measured by AFM. The absence of any strong drain voltage dependence in the device off-state (below threshold) is indicative of a device under good electrostatic gate control. In addition, Fig. 5.6(a) also contains a measurement of the same device after extensive soaking in water and subsequent measurement in air. It is apparent that the threshold voltage V_{TH} (The threshold voltage is defined as the gate voltage V_{GS} at which the devices transitions from its off-state that is characterized by an exponential change of current with V_{GS} into the device on-state.) shows a monotonic trend towards more positive gate voltages from vacuum to air to water. From this fact we conclude that

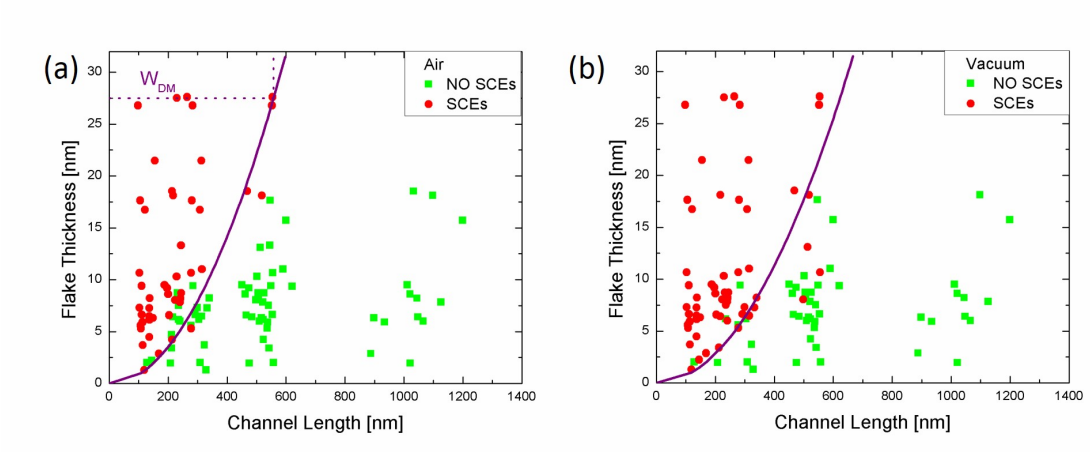


Fig. 5.5. Appearance of SCEs in air (a) and vacuum (b) as a function of channel length L and MoS_2 flake thickness. The purple lines are fits using Eq. 5.3 with parameters as discussed in the text. The only difference in the fits for air and vacuum lies in the use of an effective body thickness t_{TMD} that is about 1.25 times larger in case of the vacuum data. Copyright © (2014) American Chemical

it is the water in the air that gives rise to the difference between the vacuum and the air curve.

5.3 Analysis

With these pieces of evidence in place, we next discuss a coherent picture that captures all of the above observations. The body thickness dependence of the SCEs clearly indicates that for small film thicknesses the screening length λ is determined by t_{body} rather than W_{DM}. In fact from the plot in air (Fig. 5.5(a)) one can conclude that $W_{DM-air} > 27.5$ nm (using arguments made in the context of Fig. 5.3) defining an upper limit for the doping level in air of $N_{Aair} < 1.55\times10^{18}$ cm^{-3} if we assume a constant $\varepsilon_{MoS2-yair} = 8.9$ [81]. Here we used:

$$W_{DM} = \sqrt{\frac{4\varepsilon_{MoS2-yair}\Psi_B}{qN_A}} \tag{5.1}$$

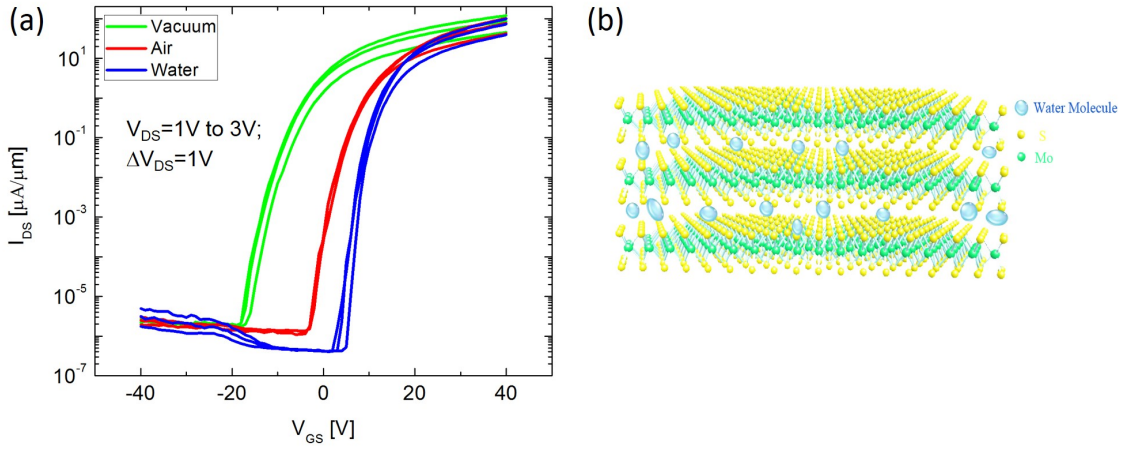


Fig. 5.6. (a) Representative transfer characteristics of a MoS_2 FET measured in air, vacuum and after soaking in water. The thickness of the flake is ∼4.7 nm. The green curve is measured after pumping for 100 min. The red curve is measured in air. After soaking the chip in water for 5 min and blow drying with nitrogen gas, the blue curve is obtained. V_{TH} in vacuum is -2 V, V_{TH} in air is 8 V, and V_{TH} after soaking in water is 13 V. (b) 3-D cartoon of MoS_2 flake in air. Copyright © (2014) American Chemical

with $\Psi_B = \frac{kT}{q} ln \frac{N_A}{n_i}$ and assuming $n_i = 1.6{\times}10^8$ cm^{-3} for MoS_2 [82]. At the same time the shift of the threshold voltage towards more negative gate voltages for a measurement in vacuum as shown in Fig. 5.6 implies either (i) a higher n-doping level or (ii) a lower p-doping level for MoS_2 FETs in vacuum than in air.(We did in fact also consider a change in ε_{MoS2-y} to explain the threshold voltage shifts observed but did not find enough evidence to make this a point of our arguments.) Water molecules are known to result in p-doping [75, 83–85]. We thus conclude that removing water molecules through the creation of a vacuum, reducing the p-doping level and resulting in a situation where $N_{A-vacuum} < N_{A-air} < N_{A-water}$, is qualitatively consistent with our data. Excluding thus scenario (i) we calculate for scenario (ii) from an average threshold voltage shift of V_{TH-air} - $V_{TH-vacuum} \approx 10$ V and $V_{TH-water}$ - V_{TH-air}

$\approx$ 5 V (see Fig.5.6), $\varepsilon_{MoS2-y-air} = \varepsilon_{MoS2-y-vacuum} = \varepsilon_{MoS2-y-water} = 8.9$ and the highest possible doping level $N_{A-air} = 1.55\times10^{18}$ cm^{-3} from above using: (Here we have assumed that the flat band voltage V_{FB} does not change substantially with the environment.)

$$\Delta V_{TH} = V_{TH1} - V_{TH2} = 2(\Psi_{B1} - \Psi_{B2}) + \frac{4\varepsilon_{MoS2-y}q}{C_{ox}}(\sqrt{N_{A1}\Psi_{B1}} - \sqrt{N_{A2}\Psi_{B2}}) \quad (5.2)$$

$N_{A-vacuum} = 3.28\times10^{17}$ cm^{-3} and $N_{A-water} = 2.49\times10^{18}$ cm^{-3} as an upper limit! Note that a lower doping level in vacuum could in principle result in more severe short channel effects [86, 87]. However, this explanation does not apply in our case since λ is defined by t_{TMD} and not W_{DM} as apparent from Fig. 5.5 if compared with Fig. 5.3.

Last, we perform a quantitative analysis of the experimental data in Fig. 5.5 in terms of the apparent difference between measurements in air and in vacuum. In order to understand the apparently more pronounced SCEs in vacuum, one needs to evaluate $\lambda_{MoS2} = \sqrt{\frac{\varepsilon_{MoS2-x}}{\varepsilon_{ox}} t_{MoS2} t_{ox}}$. To explain the observed trend $\lambda_{MoS2-air}$ ¡ $\lambda_{MoS2-vacuum}$, ε_{MoS2-x} and t_{MoS2} have to be evaluated. Since adding a high-k dielectric like water cannot result in an effectively decreased ε_{MoS2-x}, t_{MoS2} must have decreased for air compared to vacuum. However, since swelling of MoS_2 is known to occur in water [73], it again sounds as if $t_{MoS2-air}$ cannot be smaller than $t_{MoS2-air}$. Here we submit that in fact the presence of water between the MoS_2 layers does not only result in p-doping as discussed above, but also creates a stronger confinement of the electron wave function inside the MoS_2 layers. We believe that it is the dipolar water layer that effectively suppresses the hybridization between layers and thus results in an effectively thinner body the portion of the MoS_2 stack that is contributing to current flowing from source to drain. To explore the validity of this hypothesis, we have used:

$$L = a\sqrt{\frac{\varepsilon_{MoS2-x}}{\varepsilon_{ox}} t_{MoS2} t_{ox}} \quad (5.3)$$

to describe the transition between SCEs and NO-SCEs in vacuum (Fig. 5.5(b)). With $t_{ox} = 90$nm, $\varepsilon_{ox} = 3.9$, $t_{MoS2} = t_{body}$, and ε_{MoS2-x} =17 [81], we determine (see

purple curve in Fig. 5.5(b)) a in Eq. 5.3 to be about 6 in agreement with our earlier statement about the occurrence of short channel effects in general (see introductory section). With the same set of values for t_{ox}, ε_{ox}, and ε_{MoS2-x} and a = 6, we can obtain an excellent fit of the transition between SCEs and NO-SCEs now as well for the case in air (Fig. 5.5(a)) if only the effective electrical body thickness is assumed to have decreased by 20% as evident from the purple curve in Fig. 5.5(a). While it is at this stage unclear how water molecules exactly impact the band structure of few-layer MoS_2, our experimental data provide first evidence of a significant impact of water intercalation on the doping level as well as the electrostatics in MoS_2 FETs.

5.4 Conclusion

In summary, we have provided first time experimental evidence of a change in the two-dimensional electrostatics in MoS_2 FETs as a function of the device environment. Water in the air was found to result in both, a higher p-doping level of the transistors as well as a reduction in effective body thickness, presumably due to a stronger confinement of carriers in the individual layers of the structure in the presence of intercalated water molecules. Our observations are believed to be of relevance to better understand the transport in MoS_2, but more importantly hint at the opportunity to tune the electrostatics in MoS_2 FETs by means of intercalated species.

6. EXPLORATION OF CHANNEL WIDTH SCALING AND EDGE STATES IN TRANSITION METAL DICHALCOGENIDES

We explore the impact of edge states in three types of transition metal dichalcogenides (TMDs), metallic T_d-phase WTe_2 as well as semiconducting 2H-phase $MoTe_2$ and MoS_2, by patterning thin flakes into ribbons with varying channel widths. No obvious charge depletion at the edges is observed for any of these three materials, which is different from what has been observed in graphene nanoribbon devices. Semiconducting ribbons are characterized in a three-terminal field-effect transistor (FET) geometry. In addition, two ribbon array designs have been carefully investigated, showing higher current levels that are higher than conventional one-channel devices. Our results suggest that device structures with a high number of edges can improve the performance of TMD FETs, since i) edges result in a higher local electric field, which increases the effective number of charge carriers and ii) due to the absence of any detrimental edge-related scattering.

6.1 Introduction

In order to increase the computational speed and device density, reduce power consumption and the cost per function, integrated circuit (IC) logic technology has been following Moores Law with a particular focus on silicon as the channel material.

Scaling as the driving force behind this successful approach has been complemented over the last years by introducing an increasing amount of non-traditional elements from the periodic table. This has opened the door for the exploration of novel channel materials beyond germanium or III-V semiconductors. In particular, two-dimensional (2D) layered materials such as transition metal dichalcogenides (TMDs) including MoS_2, $MoTe_2$, WS_2, WSe_2, and many more are recently under careful investigation by the scientific community for various future nanoelectronics applications. However, many critical aspects of this new class of materials needs to be better understood before any verdict on their usefulness can be made. In this context we have previously discussed the impact of contacts [89], layer thickness [67,90], and tunability of short-channel effects in MoS_2 field-effect transistors (FETs) [65]. Another scaling aspect of TMDs is related to their channel width W and is studied here experimentally through transport measurements down to ribbons of W = 25 nm for the first time. For small channel width devices from 2D materials, edge state effects and quantum confinement become increasingly relevant. For example, first-principles computations indicate that zigzag nanoribbons of MoS_2 should show metallic behavior [91] and armchair nanoribbons are semiconducting with a smaller bandgap if compared to the bulk [92]. In addition, it has been noted that the electronic properties of narrow structures can also be affected by the nanoribbon edge chemical structure [91,93–95]. In this context, Bollinger et al. [96] observed a brim of highly conductive metallic edge states in single-layer MoS_2 nanostructures by using scanning tunneling microscopy (STM). Liu et al. [97] found that the channel conductance scales linearly with channel width, indicating no evidence of edge damage for MoS_2 nanoribbons with widths down to 60 nm. Zhang et al. [98] observed a bending of the conduction and valence bands at the edge of single-layer MoS_2 on graphite by STM, and recently Cheng et al. [99] reported the controlled growth of $MoSe_2$ ultra-narrow ribbons ($\sim$0.7 nm) which showed metallic behavior, while wider ribbons (>2 nm) showed a transition from metallic to semiconducting behavior from the edge towards the center of the

ribbon as measured by STM. All of this implies that edge states need to be carefully considered in ultimately scaled TMD devices.

If comparing the above with the situation in the most well-known 2D material graphene one notices that tight-binding calculations indicate interesting properties of the graphene edges similar to those mentioned for TMDs [100, 101]. However, most experiments just revealed deteriorated current carrying capabilities supposedly due to enhanced backscattering at the ribbon edges introduced through structural disorder caused by the etching process [102–105] and the bandgap induced by edge states. The main difference between graphene and semiconducting TMDs lies in the fact that for TMD devices semiconducting or metallic edge states are expected to exhibit a smaller or no bandgap compared to bulk, while in case of graphene the absence of a bandgap in the bulk only makes the graphene edge states less conductive. Thus, in semiconducting TMD devices more conductive edges parallel to the bulk channel might be expected to enhance the on-state performance of an FET even when scattering is present if a band structure change occurs. On the other hand, creating actual edges through an etch approach might result in the opposite behavior as in case of graphene due to diffusive boundary scattering or a charge depletion layer. As will be discussed in the following sections, this article provides a comprehensive study on various TMD materials, including semimetallic T_d-phase WTe_2 and semiconducting 2H-phase $MoTe_2$ and MoS_2 that are analyzed with respect to the impact of edge effects in various TMD ribbon geometries.

6.2 Device fabrication and experimental results

Device characteristics presented in the following experimental sections are based on three TMD materials, i.e. WTe_2, $MoTe_2$, and MoS_2. As will be discussed next, while the general trends observed are similar for all materials, the semimetallic phase of WTe_2 makes the gate capacitance that plays an important role for the semiconduct-

ing TMDs irrelevant, and the lower contact resistance in case of MoS_2 if compared to $MoTe_2$ makes the analysis for the former more quantitative.

Fig. 6.1(a) shows a 3D cartoon device structure of three back-gated TMD field-effect transistors (FETs) for different channel widths W. All devices in a set were fabricated on the same TMD flake, have the same channel length L and the same contact width W_C. Channels are parallel to each other in one set of devices. Fig. 6.1(b) displays an SEM image of four back-gated FETs on the same TMD flake, exfoliated onto a 90 nm silicon dioxide (SiO_2) substrate with underlying highly doped silicon using standard scotch tape techniques. After the flake transfer, e-beam lithography was used to define the channel width, followed by plasma dry etching (SF_6: 10 sccm; Ar: 10 sccm; pressure: 3 Pa; RF source power: 50 W; RF bias power: 50 W; time: 17 s). After dry etching, there is usually a residue issue after removing PMMA, which is probably due to the thermo-activated dehydrogenation of PMMA macro-molecules after plasma ions bombardment. To resolve this residue problem, an inorganic layer - omnicoat is added before coating PMMA layer. The residue layer will be removed with omnicoat, keeping the TMD surface clean. Ni (65 nm) was deposited as source/drain contacts. Electrical characterization of the devices was performed at room-temperature in vacuum using a parameter analyzer (Agilent 4156C).

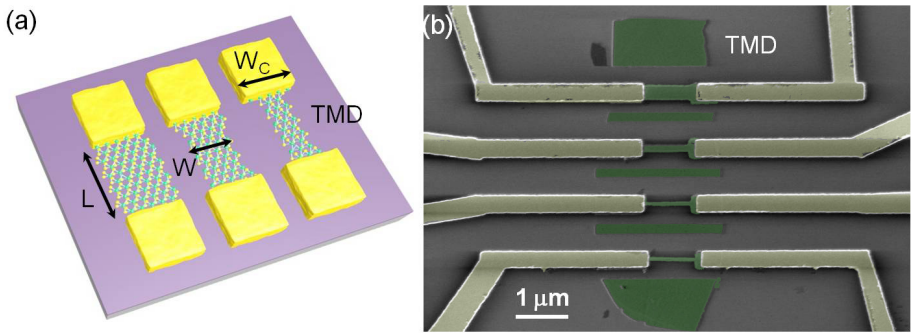


Fig. 6.1. (a) 3D cartoon of back-gated TMD FETs with different channel widths on one flake and (b) SEM image of TMD FETs with varying widths on the same flake. Copyright © (2018) Springer Nature

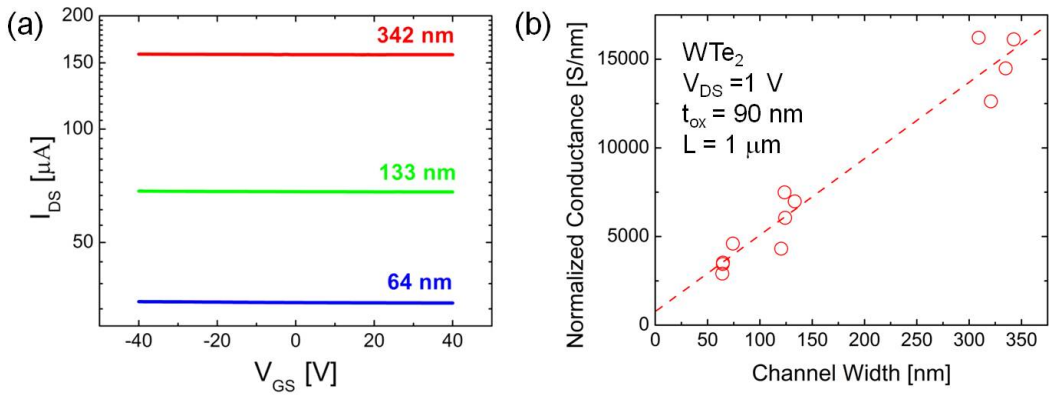


Fig. 6.2. (a) Transfer characteristics of 9.8 nm thick back-gated WTe_2 FETs measured at V_{DS}=1V for different channel widths on one flake metallic behavior with almost no gate voltage response is observed as expected. (b) Conductance normalized by channel flake thickness for different channel widths. The dashed line is a least square fit.

Using the device layout shown in Fig. 6.1, we first explored the impact of channel width scaling in semimetallic T_d phase WTe_2 devices. Fig. 6.2(a) shows transfer characteristics of 9.8 nm thick back-gated WTe_2 FETs for different channel widths. As expected, only a weak gate modulation is observed for the three devices. Since the Fermi energy in WTe_2 is expected to be substantially smaller than in 3D metals ($E_F \sim 120$ meV) [106], a small impact of the gate is indeed expected. Irrespective of channel thickness, a very similar response to the gate is observed with higher current levels achieved for thicker flakes. Fig. 6.2(b) summarizes our findings for WTe_2 ribbons with widths from 60 nm to around 340 nm indicating a clear linear trend as a function of channel width W. The resistivity ρ_{3D} of WTe_2 is found to be around 2.1 mΩ·cm without correcting for any contact resistance impact, a value that is almost half of what has been previously reported in reference [107] owing to the careful sample preparation, low contact resistance of below 425 $\Omega \cdot \mu$m and clean removal of residuals after the ribbon etch. Also note that this resistivity is only about

22 times larger than values reported for graphene [108]. Extrapolating the linear W-trend downwards to zero conductance does not show any apparent intersection with the x-axis, which would indicate the presence of a dead layer. Since for conventional metals one would typically expect a trend of the type shown in Fig. 6.2(b), while the boundary conditions for semiconductor-to-vacuum interfaces frequently result in a depletion layer, we next explored ribbons from semiconducting TMDs.

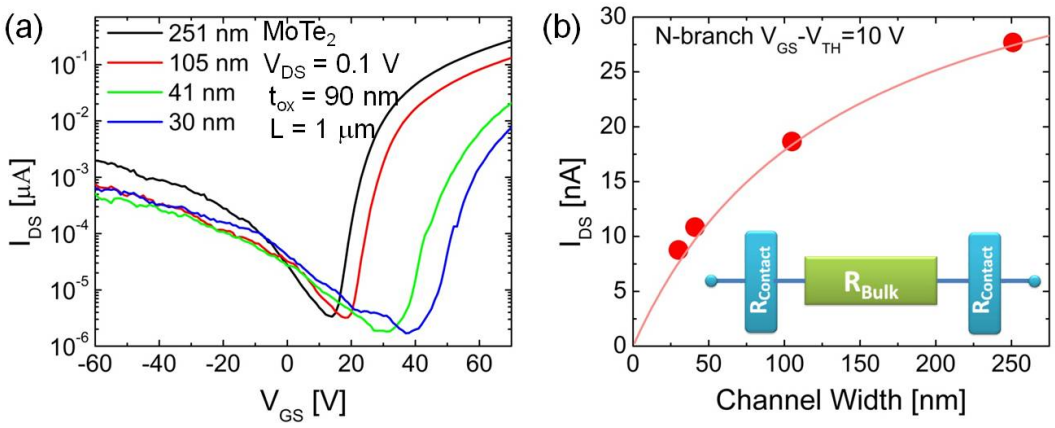


Fig. 6.3. (a) Transfer characteristics of 7 nm thick back-gated $MoTe_2$ FETs for different channel widths on one flake. (b) N-branch on-state current for different channel widths. The solid line is a fit using equation (1) with parameters as discussed in the text. The inset figure displays the resistor network. Copyright © (2018) Springer Nature

Fig. 6.3(a) shows transfer characteristics of 7 nm thick back-gated $MoTe_2$ FETs for different channel widths.Note that the threshold voltage V_{TH} shifts to positive voltages when the channel width is trimmed. However, applying a pulse-type measurement, the $V_{TH-shift}$ becomes less pronounced, which suggests that the $V_{TH-shift}$ is associated with charges introduced in the silicon dioxide layer by the dry etching process (see Fig. 6.4). Fig. 6.3(b) shows the extracted on-state current at V_{GS-VTH} = 10 V in the so-called n-branch (dominated by electron transport) of the transfer characteristics. Notice that the device is in its on-state under these gate voltage con-

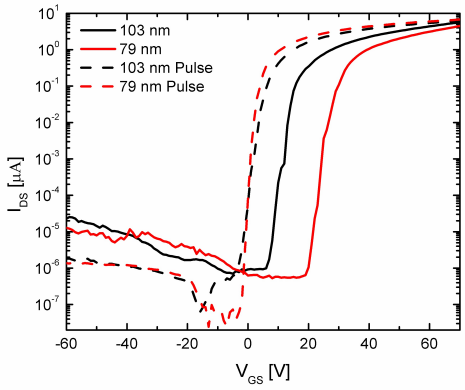


Fig. 6.4. MoS_2 transfer characteristics for different channel widths. The solid lines are measured while continuously sweeping V_{GS} while the dash lines are obtained by performing a pulse measurement where the voltage is removed after every current read out process. In the continuous measurement, the threshold voltage V_{TH} shifts to positive voltages when the channel width is trimmed. However, applying a pulse-type measurement, the $V_{TH-shift}$ is almost entirely removed, indicating that the $V_{TH-shift}$ in the continuous measurement is associated with charges introduced in the silicon dioxide layer by the dry etching process. Copyright © (2018) Springer Nature

ditions and operates in the linear region of the output characteristics (I_{DS}-V_{DS}) for the chosen V_{DS} = 0.1 V. Since the contact layout is identical for devices with different ribbon widths, the contact resistance RC is the same if we ignore device-to-device variations. Then,

$$I_{DS} = \frac{V_{DS}}{2R_C + \frac{a}{W}} \tag{6.1}$$

where a = ρ_{2D}·L and ρ_{2D} is the sheet resistivity (see inset of Fig. 6.3(b) for the resistor network). Using the current levels of the 250 nm and 105 nm wide devices, we extract a contact resistance of $R_C = 1.2{\cdot}10^6$ Ω (0.3 MΩ · µm) for a contact width of W_C = 250 nm, and an a-value of a=0.3 Ω·m using Eq. 6.1. Note that the high R_C-value is a result of the Fermi level line-up between the source/drain Ni contacts and the $MoTe_2$ bands, which as we reported before lies around 350 meV below the $MoTe_2$ conduction band edge [53]. With these values, the fit in Fig. 6.3(b) is obtained showing a good

agreement between all experimental data and Eq. 6.1. Noting that the two devices with 41 nm and 30 nm channel width show a slightly higher current drive, our results clearly do not show obvious indication of a negative impact on electron transport due to scattering at the ribbon edges or a depletion layer that would diminish the current drive. However, we also realized at this point that the too high R_C-value was the major obstacle in studying the effect of edges in semiconducting ribbons in greater details and because of this fact, started focusing on MoS_2 that as we showed before [89] exhibits a much closer line-up between the Fermi level of Ni contacts and the TMD conduction band of about 150 meV. [53]

Sets of $\sim$ 6 nm thick MoS_2 devices with the same design as shown in Fig. 6.5 were characterized. Channel widths varied between 25 nm and 260 nm. Fig. 6.5(b) is a summary of 25 MoS_2 device currents obtained from the n-branch of the I_{DS} - V_{GS} characteristics deep in the on-state (V_{GS} - V_{TH} = 49 V) at drain voltages where I_{DS} is proportional to V_{DS}. Fig. 6.5(a) shows an exemplary set of transfer characteristics. Employing the same method as discussed above, applying Eq. 6.1 to the current of the devices, we extract a contact resistance $R_C = 1.7{\cdot}10^4$ Ω(4.3 k$\Omega \cdot \mu$m) for W_C = 250 nm and a = 0.017 Ω·m. The dashed purple curve in Fig. 6.5(b) displays the resulting fit according to Eq. 6.1 which is apparently not a good description of data from devices with W $<$ 100 nm (All channel widths are characterized by a scanning electron microscope (SEM) after the transport measurements were performed. The error bar for each device is smaller than the size of the circle.). When the aspect ratio of channel width to the back gate silicon oxide thickness (90 nm) becomes smaller than one, the field lines between the channel and the gate deviate from that of a parallel-plate capacitor, resulting in an increase of back gate capacitance, which also boosts the current.

$$C = \frac{\frac{\varepsilon_{eff}}{t_{ox}}}{\frac{2}{\pi} arctan\frac{W}{4t_{ox}} + \frac{W}{4t_{ox}\pi} ln(1 + \frac{16t_{ox}^2}{W^2})} \tag{6.2}$$

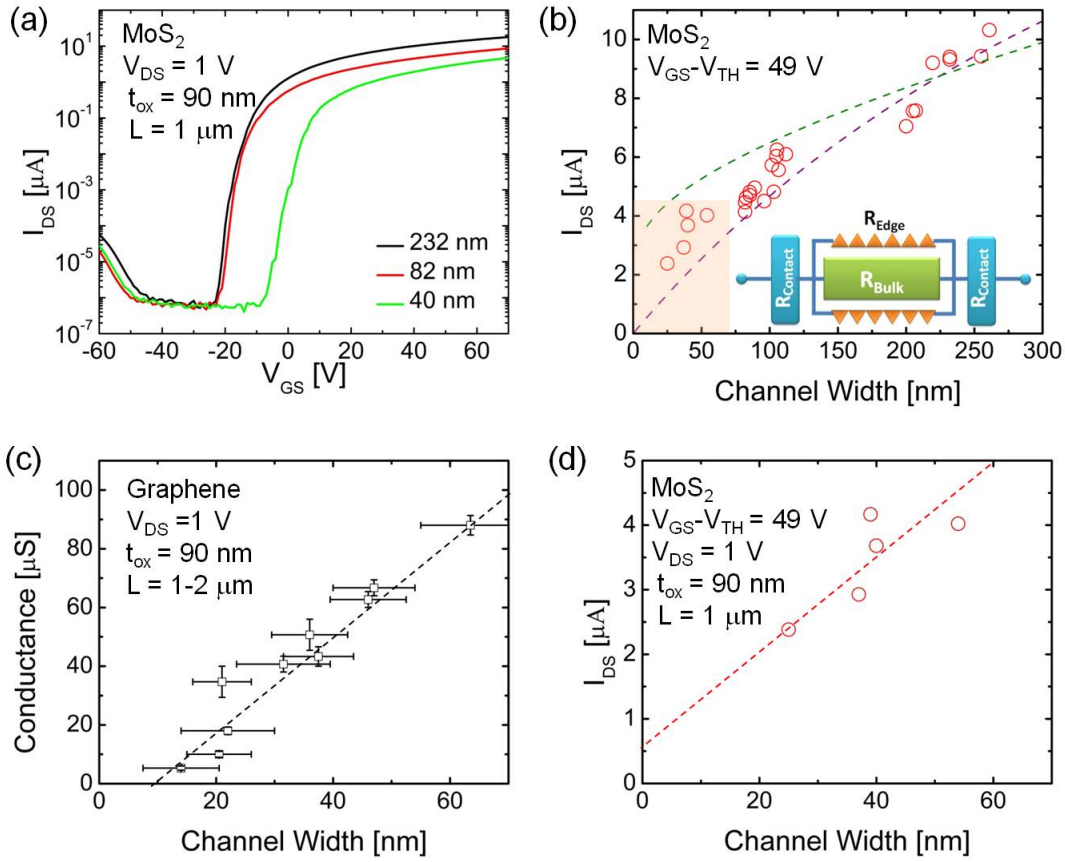


Fig. 6.5. (a) Transfer characteristics of 6 nm thick back-gated MoS_2 FETs for different channel widths on one flake. (b) On-state current levels of 6 nm thick MoS_2 FETs for different channel widths. The dashed purple line is a fit using Eq. 6.1 with parameters as discussed in the text. The green line from cross symbols is a fit considering the increase of capacitance using Eq. 6.2. (c) Conductance vs. width of parallel graphene nanoribbons measured at V_g - V_{Dirac} = -50 V according to data extracted from figure 2 in reference [82]. From the intersection with the x-axis, a finite depletion width can be inferred. (d) shows a zoom in of the orange/red region in (b). Comparing (c) and (d), MoS_2 devices display no obvious depletion. Note that the dashed line in (d) is a linear interpolation of the data points displayed in (d) and not the same as the fitted curve in (b) using Eq. 6.1.

where W is the channel width, t_{OX} = 90 nm. Since the field lines reach through both, SiO_2 and air, we are assuming in the following an effective dielectric medium with $\varepsilon_{eff} = (\varepsilon_{OX} + \varepsilon_{air})/2$.

$$a = \rho_{2D} L = \frac{L}{nq\mu_{eff}} = \frac{L}{C(V_{GS} - V_{TH}\mu_{eff})} \tag{6.3}$$

where n is the sheet carrier concentration in the TMD in units of $1/cm^2$. L = 1 μm, V_{GS} - V_{TH} = 49 V and t_{OX} = 90 nm in our case.

Next, we determine μ_{eff} using Eq. 6.3 for devices with channel widths W > 90 nm, since the capacitance C is close to C_{OX} in this case. We calculate for the bulk portion of the TMD FET an effective mobility of μ_{eff} = 31 cm^2/Vs at V_{GS} - V_{TH} = 49 V (corresponding to a carrier concentration of $1.2 \cdot 10^{13}/cm^2$), which is consistent with the mobility value of 27 cm^2/Vs obtained from the linear region of the output characteristics at V_{GS} - V_{TH} = 49 V for a device with W = 232 nm. For the same device a field-effect mobility of μ_{FE} = 29 cm^2/Vs is extracted, indicating that the carrier mobility is rather independent of gate voltage in the device on-state for wider channels. The green line from cross symbols in Fig. 6.5(b) is a fit considering the increase of capacitance according to Eq. 6.2 using the extracted constant effective mobility μ_{eff} = 31 cm^2/Vs. It is apparent that for small width channel (< 90 nm) the fitted green line gives rise to current levels beyond the experimental findings. This discrepancy may be due to an overestimation in gate capacitance, since Eq. 6.2 from above assumes a ribbon of width W separated from a 2D counter electrode by t_{OX}, while in reality, the adjacent nanoribbons and source/drain metal pads will screen some of the field lines. Also, it cannot be excluded at this point that some mobility degradation has occurred in the ribbon devices. Last, we cannot exclude the possibility that contributions from the ribbon edges are partially responsible for the improved performance relative to the purple fit line. As for the two other materials mentioned before, MoS_2 ribbons again do not show any depletion layer as evident from Fig. 6.5(d) if compared with Fig. 6.5(c) according to reference [82], a main difference to the situation in graphene.

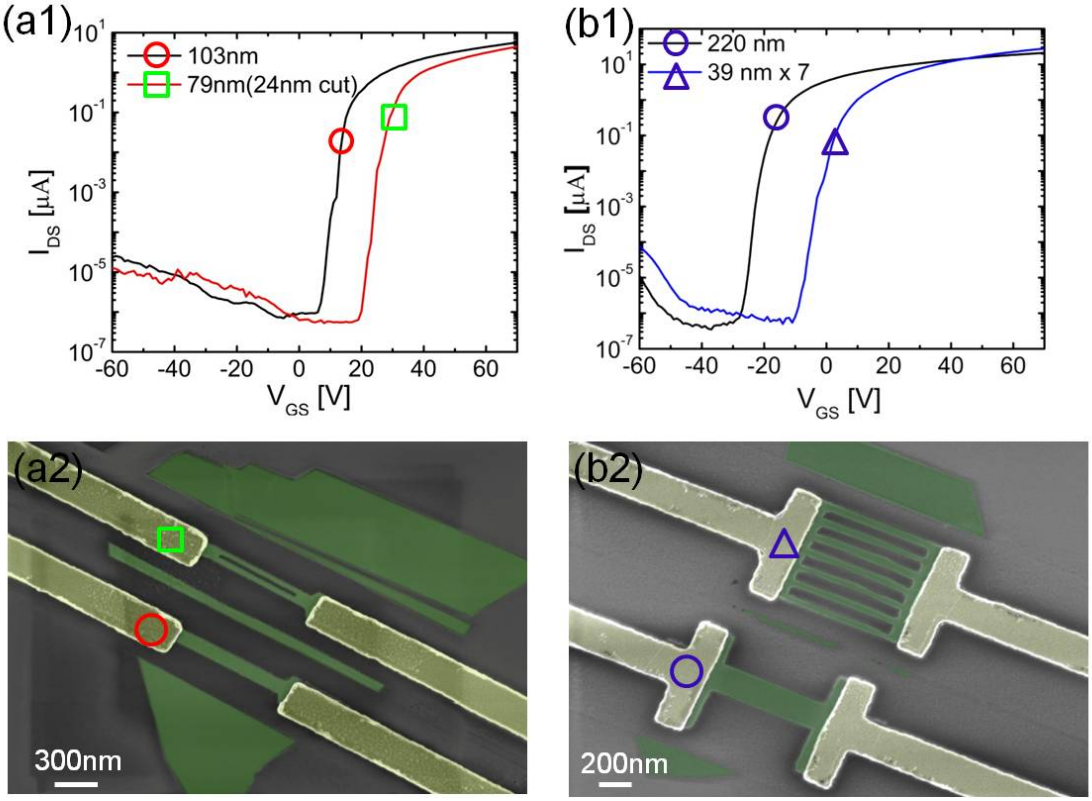


Fig. 6.6. (a1, b1) display transfer characteristics of back-gated MoS_2 FETs (∼6 nm thickness) with different designs corresponding to the SEM images in (a2, b2). Copyright © (2018) Springer Nature

Since the channel width scaling can enhance the current density due to the increase of the effective gate capacitance or potentially the presence of edge states, last, we have designed two different nanoribbon devices with layouts as shown in Fig. 6.6. In design 1, as illustrated in Fig. 6.6(a2), a 103 nm wide ribbon (red circle) is cut into two ribbons through an incision of 24 nm (green square). The contact layout is identical for the two devices. Comparing the two device characteristics in Fig. 6.6(a1), noticeably the device with a cut exhibits a higher current level if correcting for the apparent threshold voltage shift. The current data of this design (in total 6 devices) are added into Fig. 6.7 (green squares). For design 2, as shown in Fig. 6.6(b2), we have

fabricated arrays from ∼6 nm thick MoS_2 flakes comprising 7 nanoribbons in parallel (blue triangle). To further reduce the impact of R_C, a larger contact width of W_C' = 880 nm has been chosen for the blue circle and the blue triangle devices, if compared to our previous layout. Fig. 6.6(b1) shows the corresponding device characteristics for a one-channel (blue circle) and a 7 ribbons array (blue triangle) device. Note that the total channel width of these two device types is rather similar. Normalizing the channel width to the one-channel device with the same contact resistance by a factor of W_C/W_C', the blue circles and blue triangles data sets are obtained in Fig. 6.7. Interestingly, the blue triangles show higher current levels than normal one-channel device, indicating a current increase either from the enhancement in gate capacitance or contributions from edge states. We speculate that since the two array device designs force the electrical field lines to become more similar to the parallel-plate capacitor layout, part of the current enhancement may indeed stem from edge states, a statement that requires further careful characterization.

6.3 Ultra-scaled MoS_2 device

The number of defects in previously studied 2D device prototypes can reach 10^7 defects per device, as estimated from the measured bias temperature instability (BTI) drifts as shown in Fig. 6.8. However, characterization of individual defects requires devices with only about 10 active defects. The previous research allows us to achieve the required number of defects, scaling the device area L × W to be 50 nm × 50 nm. Fig. 6.9 shows the transfer and out characteristics of this device, and the SEM of this device is inset in Fig. 6.9(a). The ultra-scaled MoS_2 FETs has a channel length of L = 53 nm and width of W = 65 nm on a 20 nm thick SiO_2 gate dielectric. This work is collaborated with with Institute for Microelectronics (TU Wien) [109].

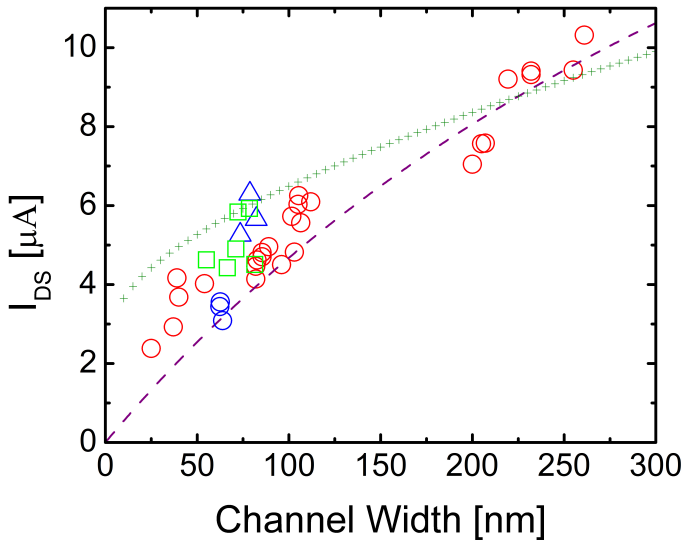


Fig. 6.7. Summary plot after normalization of the channel width for the array devices and considering the contact layouts as shown in Fig. 6.6. The current levels of the two array designs are consistently higher than those for the one-channel devices. The flake thickness of all the MoS_2 devices is ∼6 nm. Copyright © (2018) Springer Nature

6.4 Conclusion

In summary, we have explored in this article the impact of channel width scaling on the transport in three TMD materials, semimetallic T_d-phase WTe_2 and semiconducting 2H-phase $MoTe_2$ and MoS_2. No obvious depletion region was identified for channel widths down to 25 nm, which is different from graphene nanoribbon devices. When the channel width scales down, the increase of back gate capacitance masks the impact of edge states. No solid conclusion about the existence of edge states in TMDS with transport properties different from the bulk can be drawn at this stage. Last, by utilizing two different ribbon array designs, we have further validated the importance of edges in three-terminal TMD devices for enhanced current drive capabilities.

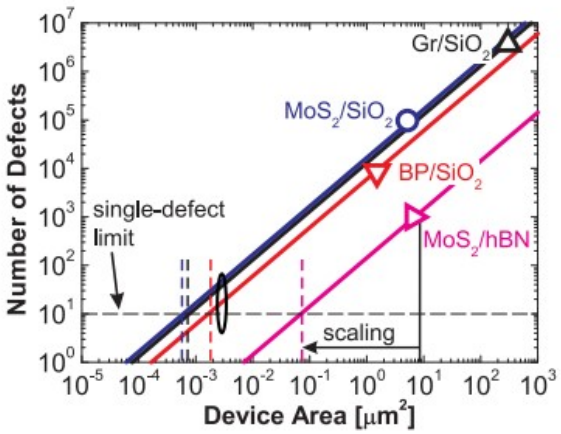


Fig. 6.8. Extrapolated number of defects per device area, starting from our prototypes. The single-defect limit of 10 defects per device can be achieved by scaling MoS_2/SiO_2 devices to about 10^3 m^2. Refer to [109] for details.Reprinted with permission from B. Stampfer, F. Zhang, Y. Y. Illarionov, T. Knobloch, P. Wu, M. Waltl, A. Grill, J. Appenzeller, and T. Grasser, Characterization of single defects in ultrascaled MoS_2 field-effect transistors,ACS nano, vol. 12, no. 6, pp. 5368-5375, 2018. Copyright © (2018) American Chemical Society

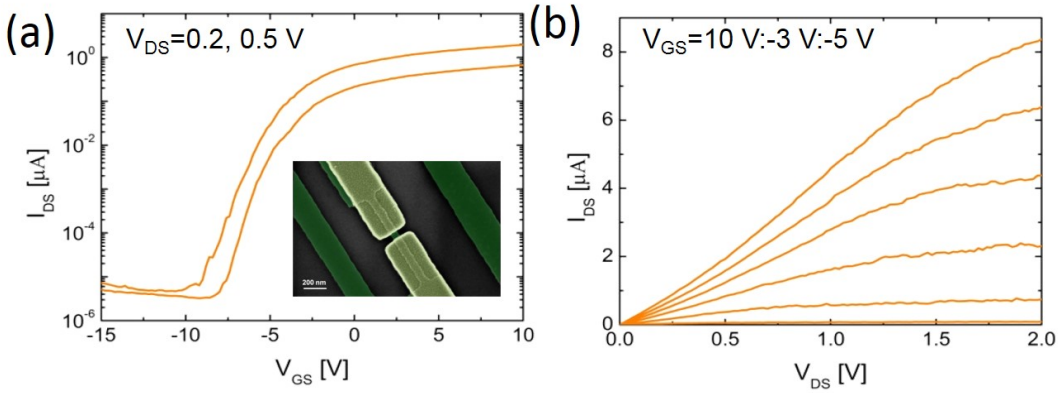


Fig. 6.9. (a) Transfer characteristics and (b) output characteristics of the ultra-scaled MoS_2 FET. The inset figure in (a) is the colored SEM image of this device. Copyright © (2018) American Chemical Society

7. SUMMARY

To continue the developments of science and technology, researchers are keeping working on the new materials, and exploring their new properties and novel applications. What will be the ultimate applications of 2D materials? This is no single answer. Do not block the ways and open more doors.

In this thesis, TMD based memory devices were studied and show promising performance. This research shines some light on the new application in the memory field with 2D materials. Chapter 2 presents TMD based selectors. They exhibit better overall performance compared with some traditional selectors, and the ultra atomic thin nature makes them even appealing in the real application. In Chapter 3, TMD working as a switching material for RRAM was explored. $MoTe_2$ and $Mo_{1-x}W_xTe_2$ alloy based vertical RRAM cells were fabricated to demonstrate clear reproducible and controlled switching with programming voltages that are tunable by the layer thickness. The switching mechanism is fully explored by C-AFM, thermoreflectance microscopy, STM, STS and STEM, which experimental demonstrated the electric field induced the structural transition from semiconducting 2H phase to a more conductive $2H_d$ structure,a transitional structural state between 2H and 1T′ or T_d. The $MoTe_2$ based RRAM performances were studied in Chapter 4, and it showed stable and reproducible performance. The switching speed is less than 5 ns. Different from conventional RRAM devices based on ionic migration, the $MoTe_2$-based RRAMs offer intrinsically better reliability and control. In comparison to phase change memory (PCM)-based devices that operate based on a change between an amorphous and a crystalline structure, our $MoTe_2$-based RRAM devices allow faster switching due to a transition between two crystalline states. Moreover, utilization of atomically thin 2D materials allows for aggressive scaling and high-performance flexible electronics applications.

Chapters 5 & 6 discuss the channel length scaling and channel width scaling in TMD based field effect transistors. The electrical performance of MoS_2 flakes is governed by an unexpected dependence on the effective body thickness of the device which in turn depends on the amount of intercalated water molecules that exist in the layered structure. The impact of edge states in three types of TMDs, metallic T_d-phase WTe_2 as well as semiconducting 2H-phase $MoTe_2$ and MoS_2, by patterning thin flakes into ribbons with varying channel widths. No obvious charge depletion at the edges is observed for any of these three materials.

All these studies in this thesis shine light on the promising future of TMD based devices in logic and memory application.

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VITA

VITA

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