INTEGRATION OF FERROELECTRICITY INTO ADVANCED 3D GERMANIUM MOSFETS FOR MEMORY AND LOGIC APPLICATIONS

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To my family and my wife, Jiwon

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SYMBOLS

α_p	Potentiation non-linearity coefficient
α_d	Depression non-linearity coefficient
C	Capacitance
C_{ox}	Oxide capacitance
C_p	Parasitic capacitance
C_{fr}	Fringing capacitance
C_{eff}	Effective capacitance
C_{FE}	Ferroelectric capacitance
C_{PC}	Positive capacitance
C_S	Substrate capacitance
D_{it}	Interface trap density
D	Displacement field
E_C	Coercive field
E_F	Fermi Level
E_i	Intrinsic fermi level
ϵ_r	Relative permittivity
g_m	Transconductance ($\mathrm{dI}_D/\mathrm{dV}_G$)
g_{max}	Maximum transconductance
G	Conductance
G_{max}	Maximum conductance
G_{min}	Minimum conductance
H_{NW}	Nanowire height
IC	Integrated circuit
I_G	Gate leakage current

I_{OFF}	Off current
I_{ON}	On current
J_G	Gate leakage current density
k	dielectric constant
k_B	Boltzmann constant
l_0	Critical length
L_{NW}	Nanowire length
λ	Mean free path
μ	Carrier mobility
ρ_C	Contact resistivity
ψ_s	Surface potential
P	Polarization
P_r	Remnant polarization
q	Elementary charge
Q	Charge
R	Resistance or Channel back scattering coefficient
R_S	Source series resistance
R_{SD}	Source/Drain resistance
R_{sh}	Sheet resistance
R_D	Drain series resistance
T	Transmission coefficient
V_D	Drain voltage
V_{DD}	CMOS drive voltage
V_{FB}	Flat band voltage
V_{FE}	Voltage across ferroelectric oxide
V_G	Gate voltage
v_{inj}	Source injection velocity
V_T (V_{TH})	Threshold voltage
W_{NW}	Nanowire width

W_{SB}	Schottky barrier width
U	Gibbs free energy
χ	Electric susceptibility

ABBREVIATIONS

ALD	Atomic Layer Deposition
AM	Accumulation Mode
BE_{sat}	Saturation Ballistic Efficiency
BDE	Branson Digital Etching
BJT	Bi-polar Junction Transistor
BOX	Buried Oxide
CMOS	Complementary Metal Oxide Semiconductor
CNL	Charge Neutrality Level
DIBL	Drain Induced Barrier Lowering
DNN	Deep Neural Network
e-NVM	Emerging Nonvolatile Memory
EOT	Equivalent Oxide Thickness
FeFET	Ferroelectric Field Effect Transistor
FeRAM	Ferroelectric Random Access Memory
FinFET	Fin Field Effect Transistor
FLP	Fermi Level Pinning
GAA	Gate All-Around
GeOI	Germanium on Insulator
HKMG	High-k Metal Gate
ICP	Inductive-coupled plasma
IM	Inversion Mode
JDE	Jipelec Digital Etching
JLFET	Junctionless FET
L-K	Landau-Khalatnikov

MIGS	Metal Induced Gap States
MLP	multilayer perceptron
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MRAM	Magnetic Random Access Memory
NBTI	Negative Bias Temperature Instability
NC	Negative Capacitance
NCFET	Negative Capacitance Field Effect Transistor
NDR	Negative Differential Resistance
NW	Nanowire
NWFET	Nanowire Field Effect Transistor
PBTI	Positive Bias Temperature Instability
PCM	Phase Change Memory
PCRAM	Phase Change Random Access Memory
PDA	Post Deposition Annealing
PMA	Post Metallization Annealing
PG	Pulse Generator
RRAM	Resistive Random Access Memory
RSU	Remote-sense and Switch Unit
RTA	Rapid Thermal Annealing
SBH	Schottky Barrier Height
SCE	Short Channel Effect
SEM	Scanning Electron Microscope
S/D	Source and Drain
SOI	Silicon-on-Insulator
SS	Subthreshold Slope (or Subthreshold Swing)
TCAD	Technology Computer-Aided Design
TNL	Trap Neutrality Level
TLM	Transfer Length Measurement (or Transmission Line Measurement)

WGFMU	Waveform Generator and Fast Measurement Unit
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray diffraction

ABSTRACT

Chung, Wonil Ph.D., Purdue University, December 2019. Integration of Ferroelectricity into Advanced 3D Germanium MOSFETs for Memory and Logic Applications. Major Professor: Peide D. Ye.

Germanium-based MOS device which is considered as one of the promising alternative channel materials has been studied with well-known FinFET, nanowire structures and HKMG (High-k metal gate). Recent introduction of ferroelectric (FE) Zr-doped HfO_2 ($Hf_xZr_{1-x}O_2$, HZO) has opened various possibilities both in memory and logic applications.

First, integration of FE HZO into the conventional Ge platform was studied to demonstrate Ge FeFET. The FE oxide was deposited with optimized atomic layer deposition (ALD) recipe by intermixing HfO_2 and ZrO_2. The HZO film was characterized with FE tester, XRD and AR-XPS. Then, it was integrated into conventional gate stack of Ge devices to demonstrate Ge FeFETs. Polarization switching was measured with ultrafast measurement set-up down to 100 ps.

Then, HZO layer was controlled for the first demonstration of hysteresis-free Ge negative capacitance (NC) CMOS FinFETs with sub-60mV/dec SS bi-directionally at room temperature towards possible logic applications. Short channel effect in Ge NCFETs were compared with our reported work to show superior robustness. For smaller widths that cannot be directly written by the e-beam lithography tool, digital etching on Ge fins were optimized.

Lastly, Ge FeFET-based synaptic device for neuromorphic computing was demonstrated. Optimum pulsing schemes were tested for both potentiation and depression which resulted in highly linear and symmetric conductance profiles. Simulation was done to analyze Ge FeFET's role as a synaptic device for deep neural network.

1. INTRODUCTION

1.1 Devices with higher performance: Scaling

It is not enough to emphasize the importance of semiconductor technology in modern society since it has tremendously influenced all aspects of human lives. Introduction of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) has replaced its predecessor, the Bi-polar Junction Transistors (BJT). Integration of Silicon platform with exponential technological advance in fabrication process yielded in unprecedented leap in processing capability of modern CPUs and memory devices. Abiding by the famous Moore's law, density of transistor has doubled approximately every 2 years reaching hundreds of millions per mm^2 as shown in Fig. 1.1 [1].

Until now, the performance upgrades were possible mainly by scaling down the device sizes. Channel length, gate oxide thickness, implantation depths and other various device parameters were scaled down to yield higher on-current, better gate controllability and thus better performance metrics. With smaller physical dimensions, various non-ideal effects such as short-channel effects or increased leakage currents became problematic.

1.2 Alternative channel material: Germanium and its challenge

Faced with the physical limitations in device dimensions, More than Moore (MtM) strategies are being discussed nowadays to continue the legacy of the successful guideline in the upcoming years [2–4]. Evidently, scaling alone cannot serve as the only winning strategy. Another aspect that needs to be considered is possibility of incorporating different materials into conventional silicon platform. Silicon has been successfully serving the microelectronic industry ever since its emergence, but it is not

widely known that the first transistor developed in 1948 at Bell Labs were based on germanium substrate [5]. However due to its inferior interface quality and difficulties in fabrication processes, germanium was not used for the mainstream industries.

Fortunately, germanium is equipped with superior electron and hole (electron: 1900 $cm^2/V \cdot s$, hole: 3900 $cm^2/V \cdot s$) mobility than Silicon (electron: 1500 $cm^2/V \cdot s$, hole: 450 $cm^2/V \cdot s$). Therefore, if appropriate fabrication and implementation strategies could be developed, germanium transistor might have its chance to exhibit better performance than the conventional silicon devices. It is also noteworthy to mention that silicon and germanium both are in the same group IV (periodic table) which gives

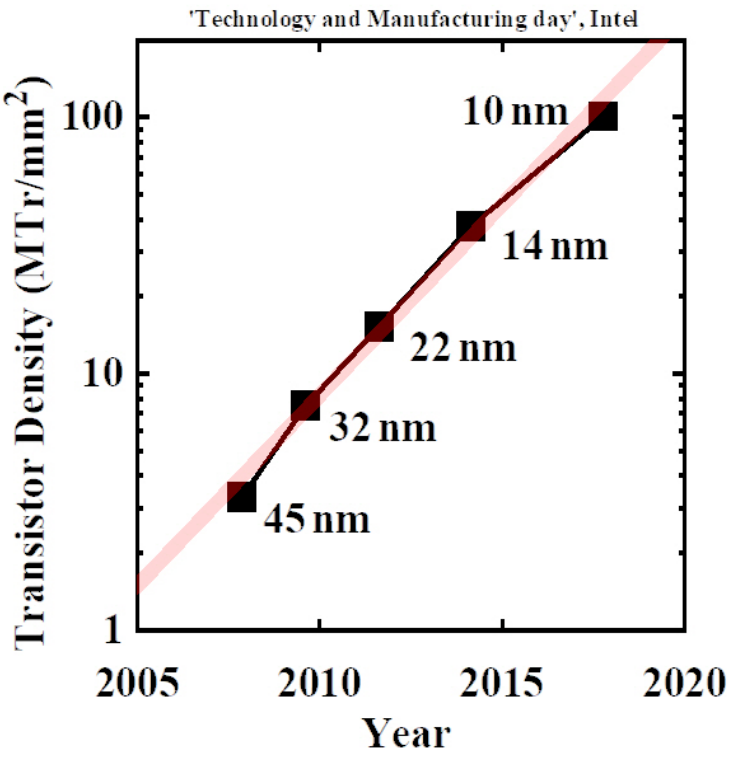

Fig. 1.1. Transistor density with respect to year. Density calculation is based on Mark Bohr's proposed method in Intel's 2017 Technology and Manufacturing day [1].

higher process compatibility within the current mainstream CMOS process technology.

However, there are several issues that must be resolved for germanium to show off its advantages such as high-quality contact formation, stable gate stack formation with good interface quality and integration of afore-mentioned technologies into a single working device without compromising the each other.

1.2.1 Interface Engineering: Gate stack

Unlike the blessed SiO_2 which is a perfect material as a gate insulator on Si substrate (excellent insulator, high break down field, well-studied oxidation behavior and low interface trap density with Si), germanium oxide (GeO_2) is not only volatile beyond certain temperature ($\sim$ 430 °C) [6, 7] but also hygroscopic [8]. GeO_2 reacts with Ge in the interface through redox reaction ($GeO_2 + Ge = 2GeO$) and GeO (g) diffuses through GeO_2 [6]. Diffusion of GeO (g) into the high-k oxide is not preferred since it degrades the overall gate stack's performance in terms of leakage current and EOT (Equivalent oxide thickness). Furthermore the dielectric constant of GeO_2 is not high enough (approximately $4 \sim 6$ [9, 10]) when compared to widely used high-k dielectrics (> 20). Therefore, it is important to form a stable gate stack that would not deteriorate the gate stack but still yield decent EOT and interface quality.

Although it is possible to achieve extreme EOT ($\sim$ 0.6 nm) using GeO_x-free gate stack [11], more widely adapted strategy in forming the gate oxide stack in germanium transistors is inserting ultrathin GeO_x layer in between the Ge channel and the main gate dielectric (usually high-k oxide) through post-oxidation [12, 13]. With superior interface quality, gate stacks with ultrathin GeO_x layer has proven to show good device performances [14–16]. Based on the common goal of improving the overall gate stack's performance, various oxides were integrated into germanium devices such as HfO_2, ZrO_2, Y, Y_2O_3, $YScO_3$, La_2O_3 and $LaLuO_3$ [11, 16–22]. Also various integration methods such as vacuum annealing [11], Si interfacial layer passivation [23–25], Ge

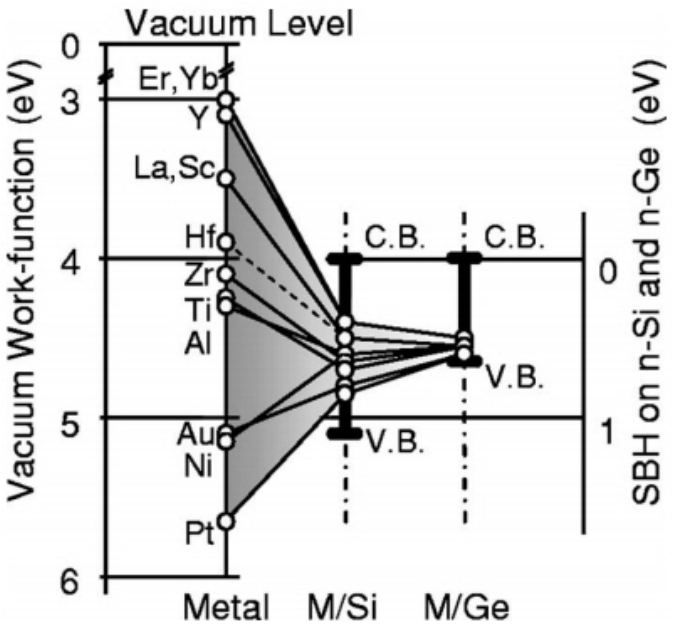

Fig. 1.2. Schottky barrier heights (SBH) extracted from n-Si and n-Ge versus various metal work functions. In case of n-Ge, strong pinning effect can be seen [32].

(oxy)nitridation [26, 27], sulfur passivation [28, 29], high pressure O_2 oxidation and plasma (or O_3) post oxidation (PPO or OPO) [16, 30] were studied for improved results.

1.2.2 Contact Engineering: Source and Drain

Contact engineering is also a critical part in germanium devices due to inferior metal-nGe contact arising from strong fermi level pinning (FLP). In metal-nGe contact, the location of charge neutrality level (CNL) is only 0.1 eV above the valence band edge and the pinning factor (S) is extracted to be only 0.05 [31–33]. As shown in Fig. 1.2, even if various metals with different work functions are contacted with n-Ge, SBH is almost constant [32]. This results in degraded drain current due to high barrier in Ge NMOS.

Exact mechanism behind fermi-level pinning is not clear yet but MIGS (metal induced gap states) or effect of electric dipole are thought to be the possible reasons behind it. MIGS theory claims that the decay of metal's electron wave function tail into the substrate causes the FLP and therefore inserting an insulating layer in between the metal and the germanium substrate is helpful in mitigating FLP since it pushes away the metal's electron wave function from the interface [32, 34]. It also implies that FLP should be weakly related to the interface characteristics as it is only caused by the incoming metal electron wave function. Another suspected origin for the FLP is the effect of electric dipole [35, 36]. By varying the interface dipole characteristics, it was reported that SBH was alleviated significantly [35].

One strategy to alleviate the FLP in metal-nGe junction is by reducing the barrier width as shown in Fig. 1.3 (a). Reducing the barrier width increases the tunneling efficiency instead of modulating the barrier height. Etching the top surface (approx. 12 nm) of nGe with BCl_3/Ar based inductive-coupled plasma (ICP) etch recipe after ion implantation and making a contact at the recessed location helped enhance the contact properties. Sheet resistance (R_{SH}) was found to be similar but contact resistance (R_C) was reduced by approximately 80 % [37].

1.3 Better performance: Lower power and steeper slope

Although the device dimension scaling has successfully served as an effective way to improve the device performances over the last few decades, it wasn't too efficient in reducing the supply voltage of the devices as shown in Fig. 1.4 (a), (b). Unfortunately, supply voltage (V_{DD}) is directly related to the power consumption of the integrated circuit (IC) chips.

$$DynamicPower \propto C_{eff} \times V_{DD}^2 \times f \tag{1.1}$$

$$StaticPower \propto V_{DD}^2 \times I_{OFF} \tag{1.2}$$

Power consumption consists of 2 different powers (dynamic and static power) which can be expressed in (1.1) and (1.2) where C_{eff} is the effective capacitance, f

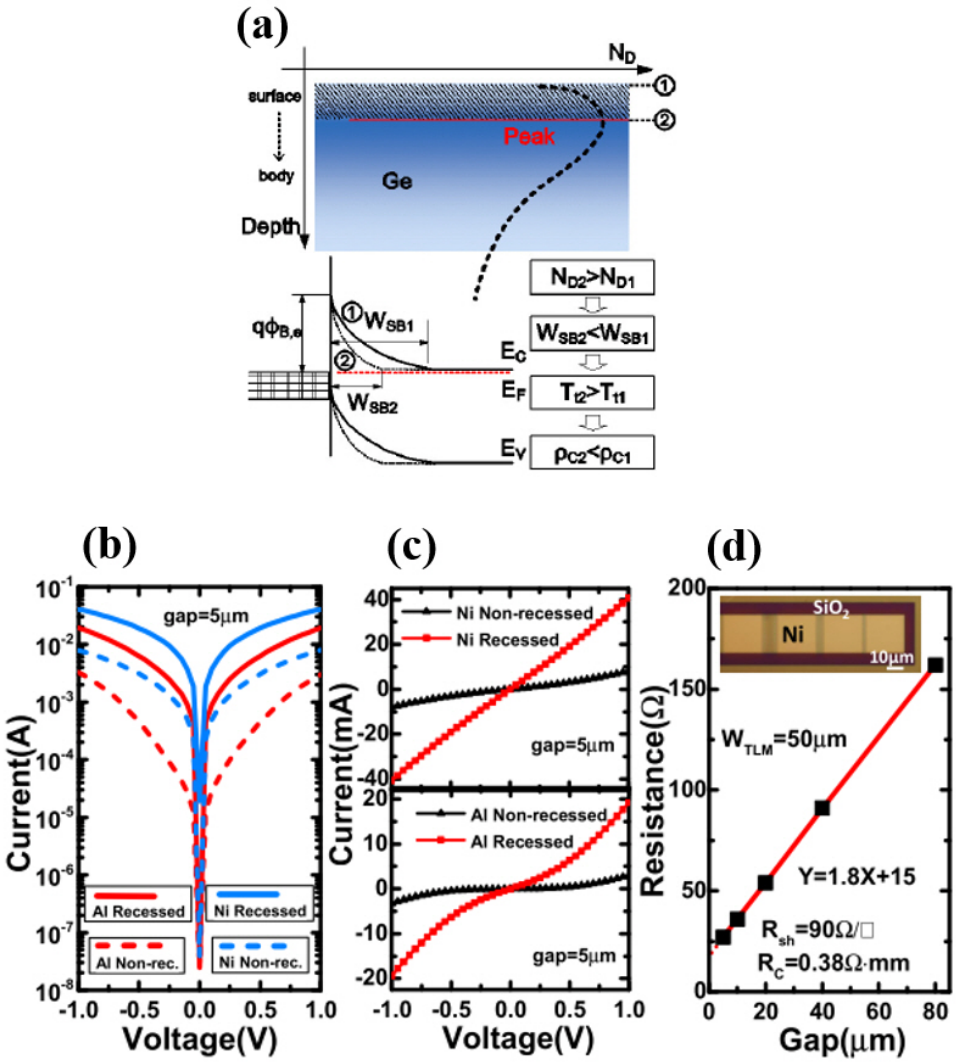

Fig. 1.3. (a) Recessed S/D structure enhances the electron tunneling efficiency by reducing barrier width (W_{SB}) which lowers the resistivity. (b) IV curves from TLM pads before and after S/D recess etching on n-Ge. (c) Linear scale representation of (b). (d) Measured resistance from the TLM pattern (inset) with Ni-nGe contact [37].

is the working frequency of the chip and I_{OFF} is the off-current. The reason why the V_{DD} has not been scaled accordingly is related to the lower limit of subthreshold slope (SS) at room temperature.

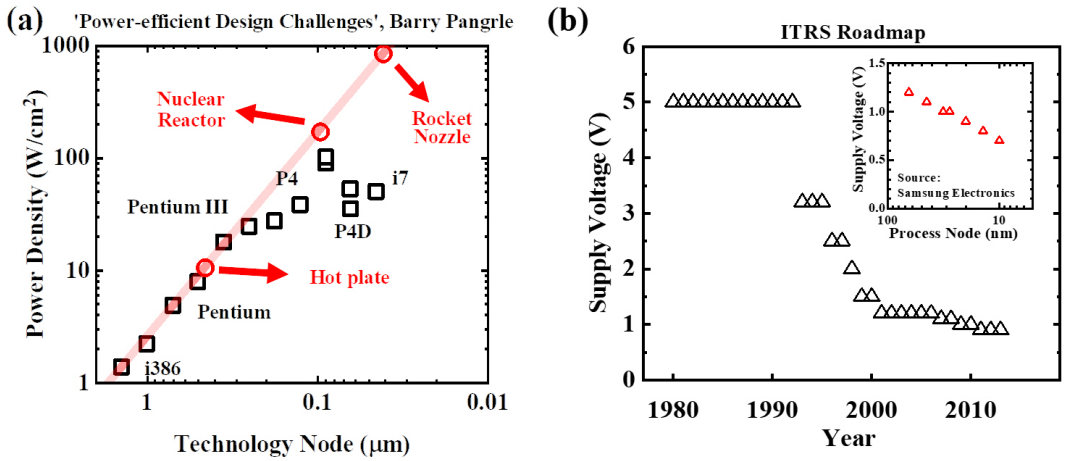

Fig. 1.4. (a) Power density with respect technology node has increased rapidly. (b) Supply voltage was not scaled accordingly. Inset graph shows most recent trend in supply voltages.

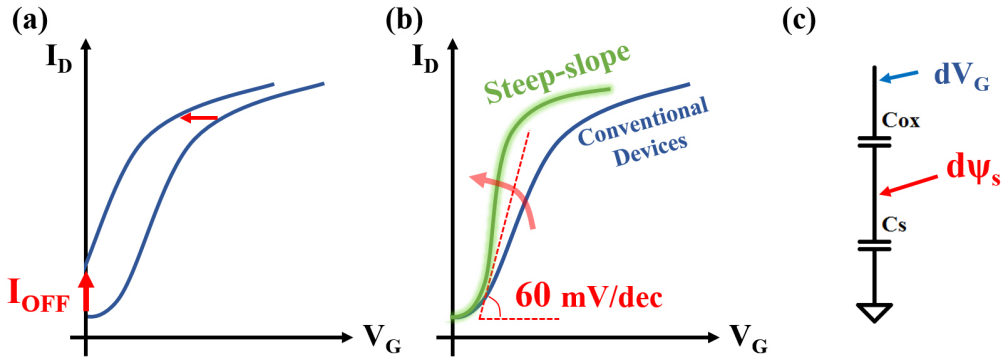

Fig. 1.5. (a) In conventional devices, reducing the supply voltage results in exponential increase in I_{OFF} due to lower limit of SS (60 mV/dec at room temperature). As shown in (b), an ideal steep slope device exhibits lower SS (below 60 mV/dec at room temperature) and therefore can produce larger current with smaller voltage. (c) A simple capacitance network in a MOS transistor showing the body factor, $d\Psi_S/dV_G$.

The SS having the lower limit of 60 mV/dec at room temperature is often referred to as *Boltzmann's tyranny* because no matter how the transistor was fabricated, the absolute minimum SS can't be further scaled below the limit as long as the transistor operates under the thermionic-emission-based-MOS mechanism. In other words, if the slope is stuck at certain value, it is impossible to suppress the I_{OFF} increase with respect to reduction in operating voltage as shown in Fig. 1.5 (a). The goal of steep-slope devices would to result in a transfer curve as depicted in Fig. 1.5 (b). A simple capacitance network in a typical MOS transistor shown in Fig. 1.5 (c) includes Ψ_S, C_S and C_{ox} which are surface potential, semiconductor capacitance and oxide capacitance, respectively. SS then can be expressed as,

$$SS = m \times n = \left[\left(\frac{d\Psi_S}{dV_G} \right) \times \left(\frac{dlog_{10} I_D}{d\Psi_S} \right) \right]^{-1} \tag{1.3}$$

$$m = \left(\frac{d\Psi_S}{dV_G} \right)^{-1} = \left(\frac{C_{ox}}{C_{ox} + C_S} \right)^{-1} = 1 + \frac{C_S}{C_{ox}} > 1 \tag{1.4}$$

$$n = ln10 \times \frac{k_B T}{q} \approx 60mV/dec \tag{1.5}$$

As (1.3) and (1.4) imply, physical meaning of m (body factor) is the voltage division ratio between the applied differential gate voltage and the differential surface potential. When a gate voltage is applied, only partial fraction of it is delivered to the surface potential which modulates the energy band of the channel surface. Since the capacitance values of well-known, conventional dielectrics are positive, m is always larger than 1. The coefficient n in (1.5) is related to the current mechanism (how the surface potential modulates the barrier height in the source-end of the channel which allows the carriers to be injected into the channel) and this is a fixed value at a given temperature as long as the mechanism is maintained. Therefore, to reduce the SS, changing the current mechanism might seem the only way since capacitance values are usually positive.

Among the proposed strategies, tunneling FET (TFET), impact ionization MOSFET (IMOS) and negative capacitance FET (NCFET) are most widely known. TFET changes the n by modulating the tunneling probability of carriers with gate voltage.

Although it can achieve sub-60mV/dec SS, TFET usually suffers from low on-current due to the nature of tunneling current [38]. IMOS intentionally causes the carriers to undergo impact ionization (avalanche breakdown) for abrupt increase in current (and thus steeper slope) but it requires high electric field which weakens the initial motivation of V_{DD} reduction [39].

1.3.1 Ferroelectric oxide and its switching

After introduction of the negative capacitance (NC) concept [40], incorporation of ferroelectric (FE) oxide in gate stack of a MOSFET aiming to modulate the body factor (m) and thus lowering the SS has gained huge attention by the society. NCFET has been extensively discussed recently due to its possibility to pull down the SS below the 60 mV/dec limit while still maintaining high on current. NCFET is fully compatible with the conventional platform and since the channel conductance mechanism is not affected, it does not suffer from low on-current.

Thanks to active researches on ferroelectric HfO_2-based oxides [41], $Hf_{0.5}Zr_{0.5}O_2$ (HZO) layer deposited with ALD (atomic layer deposition) has been successful in realizing highly compatible oxide layer for FeFETs and NCFETs [42–47]. Studies on ferroelectric polarization and its speed is also another active field concerning FeFET and NCFET's capabilities [48–50].

Fig. 1.6 (a)-(c) depict the relationship between polarization and electric field. Polarization in dielectric material is linearly proportional to the electric field but paraelectric shows partially different dielectric constant ($k = \epsilon_r = 1 + \chi$, where χ is electric susceptibility) which can be seen from the slope of the curve. However, a ferroelectric material shown in Fig. 1.6 (c) exhibits hysteretic loop due to spontaneous polarization that still exists even when the applied electric field is removed. Beyond the coercive electric field (E_C), the polarization direction switches.

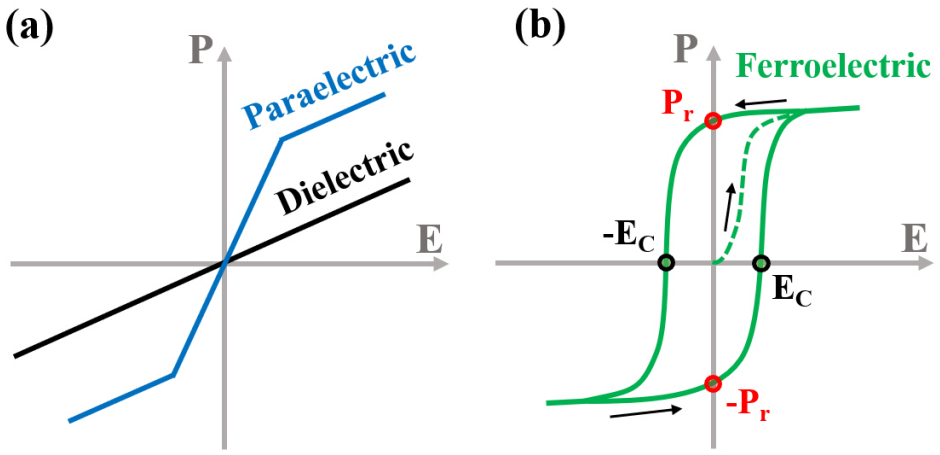

Fig. 1.6. Polarization as a function of electric field in a typical (a) dielectric and paraelectric and (b) ferroelectric material. Due to spontaneous polarization, ferroelectric material show remnant polarization (P_r) even after the external electric field is removed. Electric field beyond E_C is needed to switch the spontaneous polarization direction.

1.3.2 Hysteresis-free operation in a NCFET

In Fig. 1.7, since the $C = (d^2U/dQ^2)^{-1}$, region near $Q = 0$ (concave downwards) on dotted green curve represents the $C < 0$ region. The energy landscape (U-Q) in Fig. 1.7 is based on the Landau theory that expresses the Gibbs free energy of ferroelectric materials. It expands the free energy (U) in terms of power series of polarization (or Q) as in (1.6) where E_{FE} is the electric field across the ferroelectric material and α, β and γ are the expansion coefficients which can be experimentally fitted using the solution of Landau-Khalatnikov (L-K) equation shown in (1.7).

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - E_{FE} \times P \tag{1.6}$$

$$\rho \frac{dP}{dt} = -\frac{dU}{dP} \tag{1.7}$$

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \tag{1.8}$$

From (1.6) and L-K equation (1.7), solution can be derived as (1.8) assuming equilibrium condition ($dU/dP = 0$) resulting in another power series of external

field in terms of polarization. Since E_{FE} and P can be directly measured from a commercially available ferroelectric tester, coefficients can also be extracted from curve fitting.

Unfortunately, ideal negative capacitance doesn't exist as it is unstable. Therefore, ferroelectric oxides (dotted green curve) with energy landscape shown in Fig. 1.7 can be integrated into the positive capacitance gate dielectric (dotted black curve) to incorporate the NC effect which can give the overall series capacitance network (solid red line).

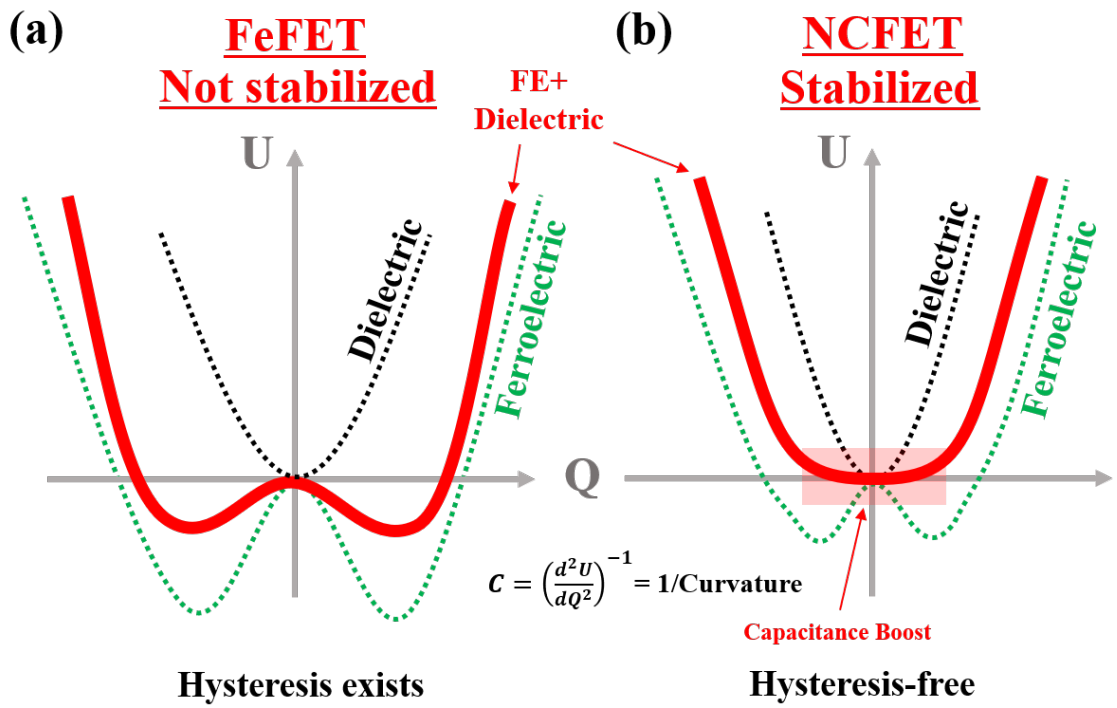

Fig. 1.7. Energy landscape (U) vs charge (Q) of a (a) FeFET and (b) NCFET. If ferroelectric oxide layer in series with positive dielectric layer is not stabilized appropriately, ferroelectric voltage hysteresis exists within the overall gate oxide resulting in ferroelectric FET (FeFET) depicted in (a). However, when the series capacitors are stabilized, hysteresis-free NCFET can be realized.

1.3.3 Short channel effects in NCFET

In NCFET, in addition to reduced subthreshold slope (SS), opposite trends in typical short channel effects (SCE) well known in conventional devices can be observed due to its NC nature [51]. As seen in Fig. 1.8 (a), with fixed V_G and increasing V_D, at first the current increases in linear region.

However, as V_D keeps increasing, channel charge decreases but due to negative capacitance, decrease in charge translates to increase in V_{FE} and thus lowers the

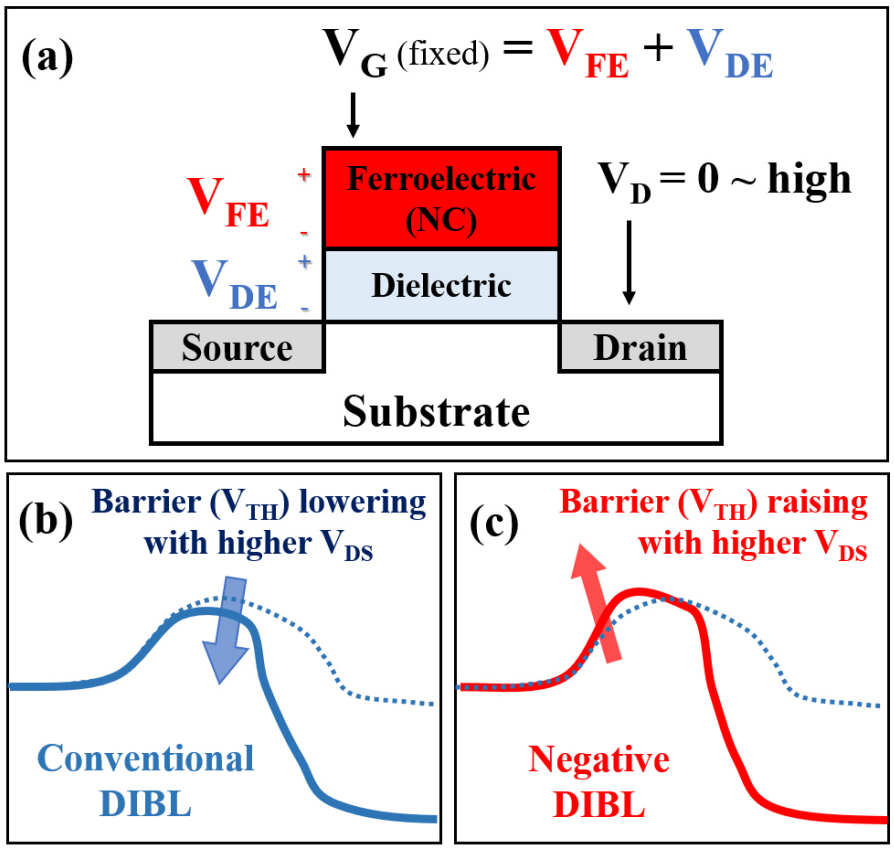

Fig. 1.8. (a) A simple series capacitance representation of a gate stack in a NCFET. Due to negative capacitance and drain to channel capacitance coupling, increasing V_D results in decrease in charge, increase in V_{FE}, decrease in V_{DE} and thus decrease in channel charge. Diagrams showing (b) DIBL in a conventional MOSFET and (c) negative DIBL in a NCFET.

voltage across normal dielectric layer which suppresses the channel charge again. This is opposite from DIBL observed in conventional MOSFETs (Fig. 1.8 (b)) and the negative DIBL effect (Fig. 1.8 (c)) continues until the carriers reach the saturation velocity. Fig. 1.9 (a) and (b) shows such negative differential resistance [51].

Surprisingly, NCFETs are reported to be more tolerant to short channel effects such as DIBL (drain induced barrier lowering), threshold voltage roll-off and SS increase with channel length scaling [52–54]. This opposite trend arises from drain to channel capacitance coupling and dominance of fringing capacitance (C_{fr}) over the dielectric and fin capacitance as channel length shortens [52]. From Fig. 1.9 (c)-(f), shorter channel lengths give smaller SS and increased V_T which are totally opposite trends from those of conventional MOSFETs. Role of fringing capacitance in NCFET was studied using steady-state and dynamic simulation [55].

1.4 Possible application as a neuromorphic synapse

Continuous development in device performance and parallel computing capability have introduced another major revolution in the field of machine learning. Brain-inspired synaptic devices have gained a huge attention in the field and deep neural network (DNN) has emerged. In the device point-of-view, emerging nonvolatile memory (e-NVM) devices are being considered as synapses in non-von Neumann architectures. These e-NVM neuromorphic networks have been reported based on various types such as phase change memory (PCM) [56], resistive random access memory (RRAM) [57, 58] and ferroelectric FET (FeFET) [59–61].

The biggest advantage of using the e-NVM as synaptic devices for online learning is the absence of need to save and access the data in the external memory. The synaptic device itself not only can do the multiplication (weight and the input data) but also retain the weight data locally after the weight updates. Multiplication and addition of processed data can be done through simple Ohm's law and Kirchhoff's current law. Currents acquired by applying input data (V_{Input}) to the e-NVM de-

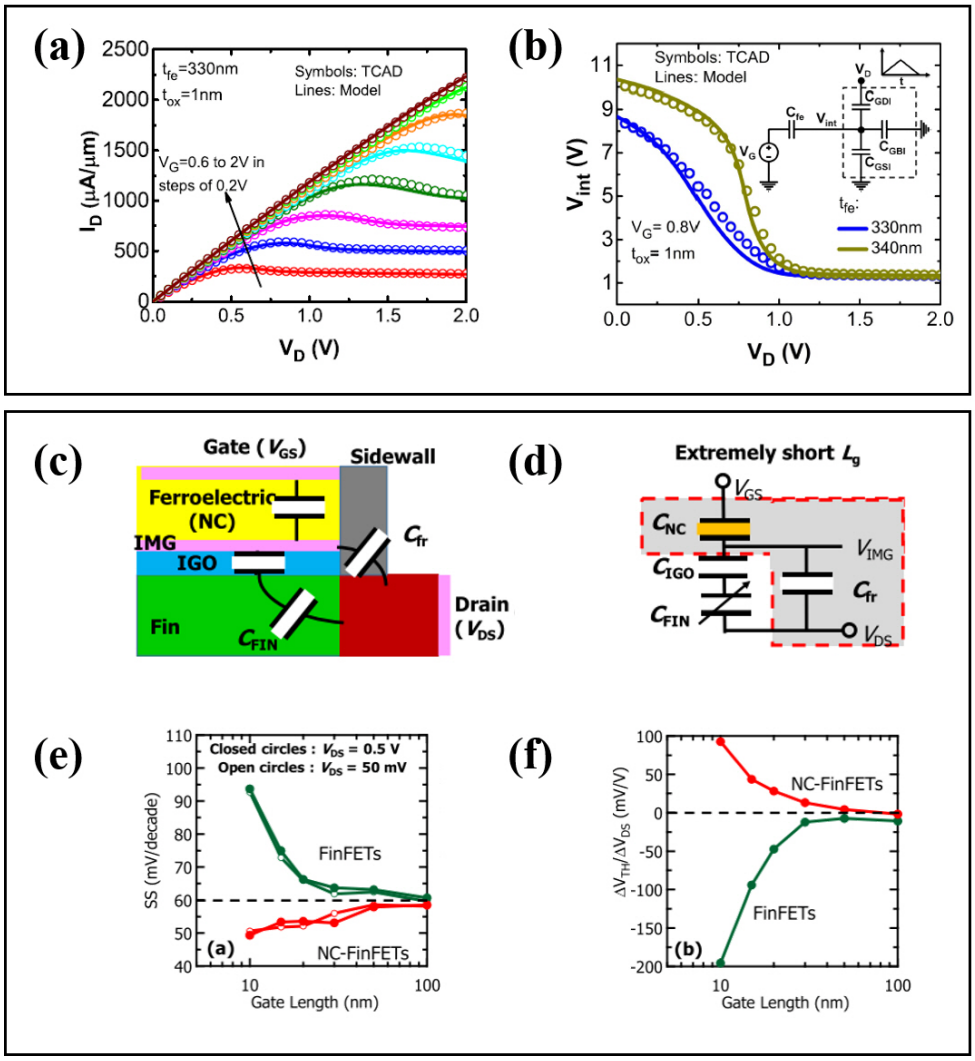

Fig. 1.9. (a) Negative differential resistance (NDR) can be observed with increasing V_D [51]. (b) Such negative DIBL is due to drain to channel capacitance coupling and negative capacitance of C_{FE} [51]. (c) and (d) show the effect of fringing capacitance (C_{fr}) within a NCFET. With shorter channel lengths, C_{fr} becomes more dominant and reduced V_{IMG} causes the opposite trends in (e) SS and (f) $\Delta V_T/\Delta V_{DS}$ with respect to channel length [52].

vices (programmed with respective weights in the form of conductance) are summed together and delivered to the next layer ($I = G \times V$).

As mentioned, weights are saved in the form of conductance ($G = 1/R$). Therefore, conductance profile should be equal in steps and symmetrically distributed during weight increase or decrease process. Also, the number of possible states that a weight data can have is also an important factor.

Fig. 1.11 (a) shows the conductance profile during potentiation process. Ideal conductance as a function of number of pulses should be linear (solid grey line) and the G_{max} should always be the same when maximum number of pulses are applied.

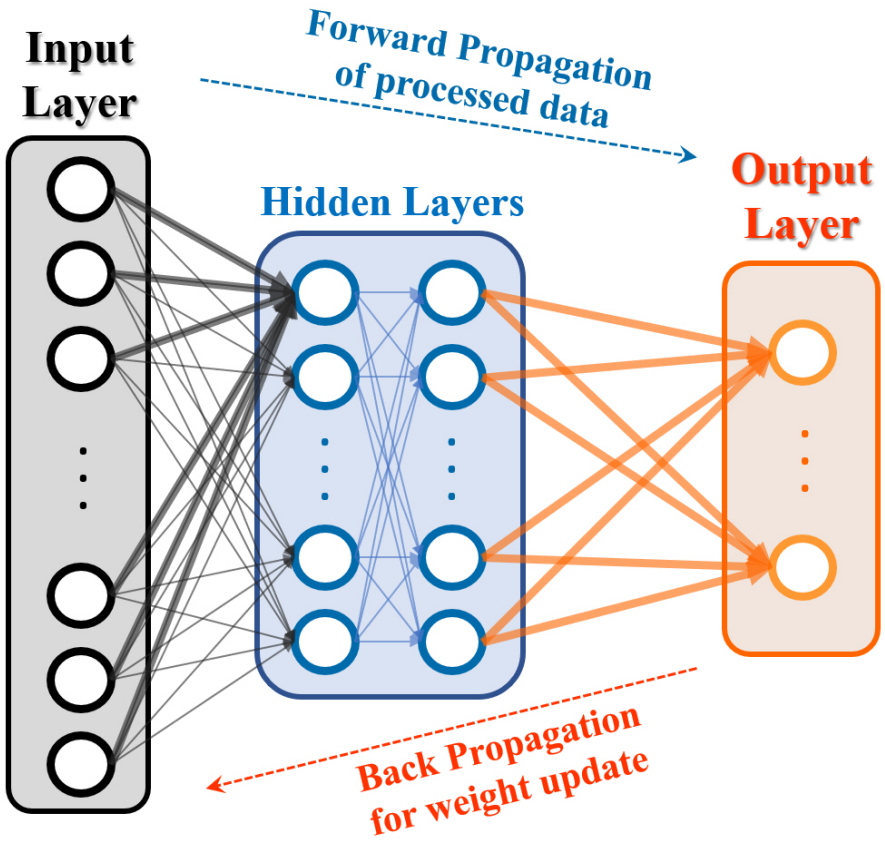

Fig. 1.10. A diagram that describes the operation of an online training scheme in a deep neural network including the back propagation for the weight updates. 2 hidden layers were depicted.

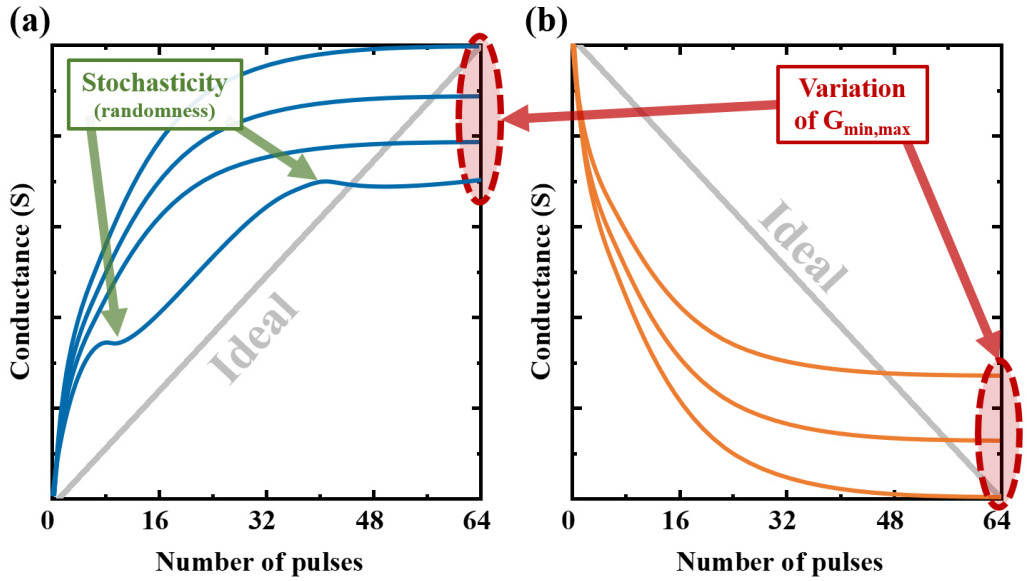

Fig. 1.11. Conductance profile during (a) potentiation and (b) depression process. Ideally, conductance profile should be linearly proportional to the number of applied pulses. Non-ideal features such as stochasticity (random conductance update) and variation in G_{max} or G_{min} is shown in both figures.

Depression process should also be similar to the potentiation process but only mirrored about y axis (symmetric) as depicted in Fig. 1.11 (b). G_{max}/G_{min} ratio is also another issue that should be addressed, where larger than 10 is needed for higher accuracy [58, 62].

1.5 Thesis Outline

In this thesis, a well-known alternative channel material, germanium-on-insulator (GeOI) wafers were used for various experiments. In device structure point-of-view, 3D FinFET and nanowire FET (NWFET) structures were fabricated. Experimental assessment of germanium nanowire nFET's ballistic efficiency was done to study the nanoscale Ge nFETs. Integration of ferroelectric oxide into the conventional germa-

nium 3D structure was studied to yield the first demonstration of bi-directional sub-60mV/dec germanium CMOS negative capacitance FinFET. Investigation on capability of germanium nanowire ferroelectric FET (FeFET) and its possible application towards the neuromorphic synaptic device are dealt in this thesis as well. Following chapters are arranged as follows.

- Chapter 2 covers the integration of ferroelectric oxide layer into the conventional high-k gate oxide stack for the demonstration of Ge FeFET. Since FeFET is one of the promising emerging non-volatile (e-NMV) devices for memory application, Ge FeFETs were studied further for real-time monitoring of drain current to probe the nanosecond polarization switching which is closely related with FeFET's operation speed.

- Chapter 3 continues towards realization of germanium NCFET on the basis of developed/studied ALD HZO from previous chapter. NCFET targets for the realization of steep slope logic devices by stabilizing the ferroelectric oxide with series connection of a regular dielectric oxide. Integration of ferroelectric material into conventional germanium transistor platform was studied and its short channel effects were statistically measured. In addition, digital etching technique was optimized for thinner fin structure on GeOI wafer.

- Chapter 4 explains the possible application of Ge FeFET towards a synaptic device that can be used in a deep neural network that executes on-line learning. Criteria for optimizing potentiation and depression pulses was studied experimentally to maximize the linearity and symmetry of conductance profile. Online learning simulation was executed to assess the accuracy of MNIST dataset training using the experimental parameters extracted from fabricated Ge FeFET.

- Chapter 5 summarizes the experimental research results described in this thesis and possible future research directions are stated.

2. GE FEFET TOWARDS MEMORY APPLICATION

2.1 Introduction

As mentioned in chapter 1, introduction of ferroelectric material has gained tremendous attention recently due to its application towards the negative capacitance FETs (NCFETs) [42–46, 63]. However, the ferroelectric materials and their properties have been studied for continuously for application in ferroelectric random access memory (FeRAM) devices and FeFETs [64–69], along with other emerging non-volatile memory (e-NVM) devices such as magnetic RAM (MRAM), resistive RAM (RRAM) or phase change RAM (PCRAM). In this chapter, integration of ferroelectric oxides deposited with atomic layer deposition (ALD) into conventional state-of-the-art germanium 3D devices will be discussed. Characterization of ferroelectric material's polarization as a function of electric field and its polarization switching time response are included using the germanium platform.

2.2 Ferroelectric $Hf_xZr_{1-x}O_2$ (HZO)

Before the introduction of the popular $Hf_xZr_{1-x}O_2$ (HZO) ferroelectric oxide, most ferroelectric applications employed the complex perovskite systems which suffer from difficulties in scaling and compatibility into conventional platform [70]. Perovskites share a structure of ABX_3, where A and B are positive cations and X is a negative anion such as $BaTiO_3$ or $LiNbO_3$. As these materials usually include heavy metallic components that are not usually compatible with the conventional platform, it is not preferable to include perovskites into modern CMOS devices.

Thanks to doped-HfO_2 ferroelectric materials, which are highly scalable, controllable and compatible material, integration of such materials into conventional devices

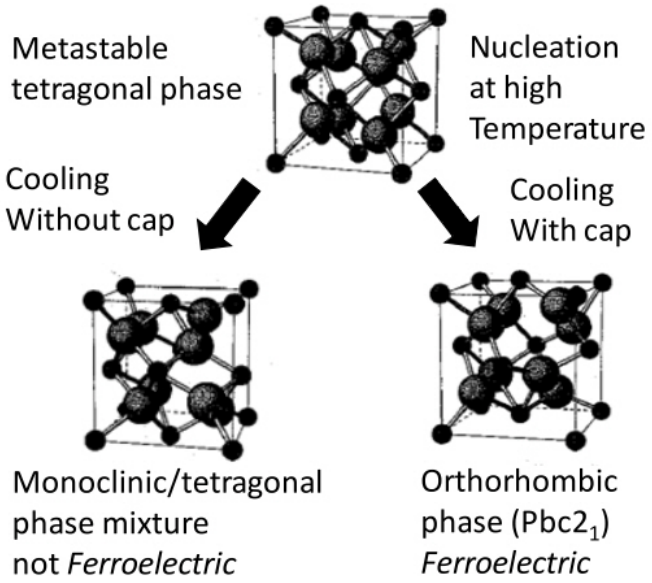

Fig. 2.1. Ferroelectricity induced due to transformation from tetragonal to orthorhombic crystal structure in doped HfO_2 layer [73]

are extensively being implemented [41, 49, 71–73]. Ferroelectricity in doped-HfO_2 material can be acquired by crystallization of the film above certain annealing temperature [97]. Different dopants such as Si [64,73–75], Y [76], Al [77] and Zr [41] were tested with HfO_2 which resulted in ferroelectricity. Since both Hf and Zr are widely used in mainstream CMOS platform, $Hf_xZr_{1-x}O_2$ (HZO) was chosen as the material for the germanium devices studied in the sections that will be discussed from now.

The ferroelectricity in doped HfO_2 is known to be due to non-centrosymmetric atomic structure such as orthorhombic structure as seen in Fig. 2.1. However, the as-dep HZO is not ferroelectric. Therefore, rapid thermal annealing (RTA) beyond the transformation temperature should be done to induce the ferroelectricity within the HZO. This transformation step can be verified through X-ray diffraction peaks shown in the following sections. In addition, polarization analysis on ferroelectric HZO can be found later in the chapter via polarization curves.

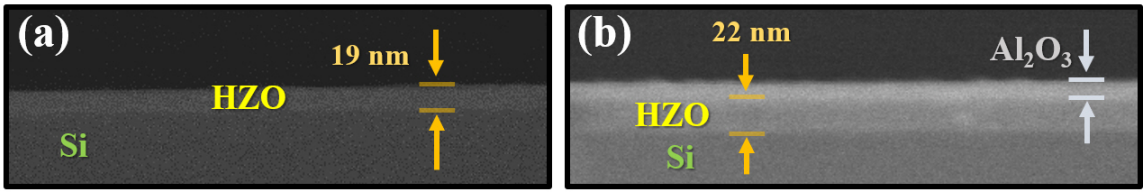

Fig. 2.2. (a) Deposited $Hf_xZr_{1-x}O_2$ at 250 °C. 120 cycles resulted in approximately 19 nm of HZO. (b) 156 cycles result in 22 nm which shares the same deposition rate.

2.2.1 ALD-deposited HZO

Integration of Zr into HfO_2 can be done by depositing alternating layer-by-layer deposition of HfO_2 and ZrO_2 during ALD deposition. Tetrakis(dimethylamino) hafnium (TDMAHf) and Tetrakis(dimethylamino) Zirconium (TDMAZ) were used as Hf and Zr precursors. H_2O (DI water) was used as oxidant. With chamber temperature set to 250 °C, 1 pulse of Hf precursor followed by a H_2O pulse deposited 1 layer of HfO_2 and then subsequent 1 layer of ZrO_2 was deposited. When HfO_2 was deposited separately, the rate was found to be 0.06 nm/cycle and ZrO_2 deposition rate was 0.08 nm/cycle. By alternating HfO_2 and ZrO_2 layers, deposition rate was confirmed to be 0.14 nm/cycle with SEM.

After depositing the HZO layer, a thin (1 nm) Al_2O_3 layer was capped to prevent the HZO from being exposed to atmosphere before transferring into the RTA chamber. More importantly, due to strained nature of the capping layer, capping the HZO helps promote ferroelectricity (orthorhombic) by preventing the crystallographic transformation from tetragonal (pure ZrO_2) to monoclinic (pure HfO_2) during cooling [41]. Increasing the ZrO_2 (tetragonal) content within the HZO film further induces antiferroelectricity as the mol% exceeds 50 and becomes tetragonal structure as the film reaches pure ZrO_2. The reported work also observed maximized remnant polarization (P_r) at Zr content of 50 mol% [41]. Controlling the Zr content within HZO

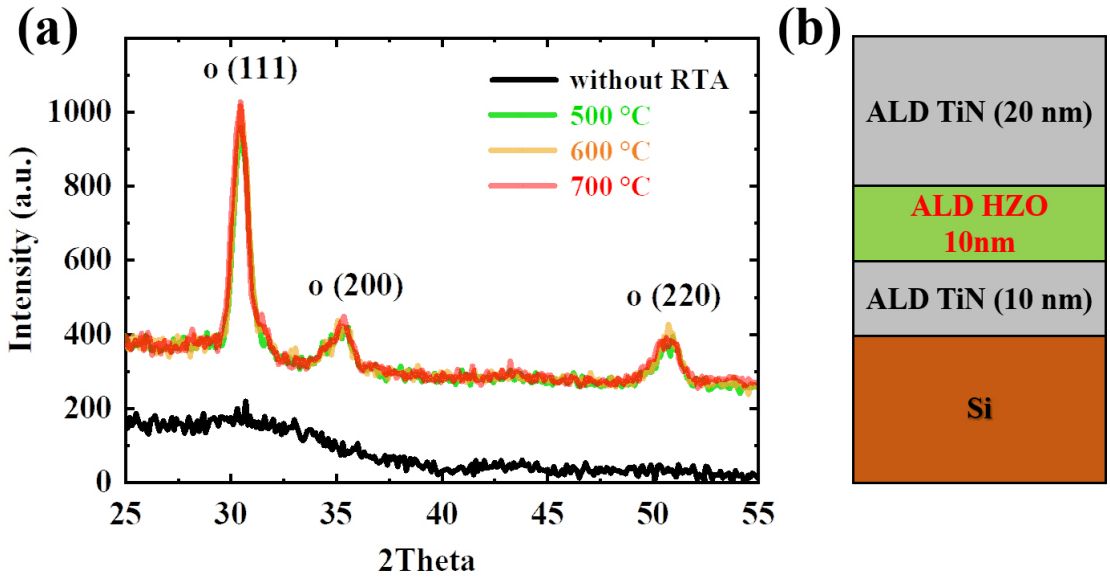

Fig. 2.3. (a) XRD peaks showing distinct difference in crystallographic structure in annealed HZO. Black curve shows as-dep HZO before RTA crystallization. (b) Oxide stack analyzed in (a).

to achieve anti-ferroelectricity was reported from our group recently [78]. However, in this thesis, only Hf pulse:Zr pulse = 1:1 was tested.

From Fig. 2.3 (b) structure, XRD analysis was taken place to probe the crystal structure before and after the RTA crystallization of 10 nm HZO film capped by TiN. Fig. 2.3 (a) shows that although as-dep HZO film (deposited at 250 °C) shows no distinct XRD peaks, annealed HZO layers show clear orthorhombic peaks as reported by various works [41, 44, 76, 77, 79, 80].

Another important physical/chemical analysis left is X-ray photoelectron spectroscopy (XPS) analysis. An ordinary XPS studies the atomic composition of the sample by irradiating X-ray and analyzing the emitted electron's kinetic energy. Also, number of electrons at each energy (eV) level are tracked as well for compositional ratio analysis. Usually the X-ray approximately penetrates the top 10 nm into the sample from the surface and averages the signal. However, if angle-resolved XPS

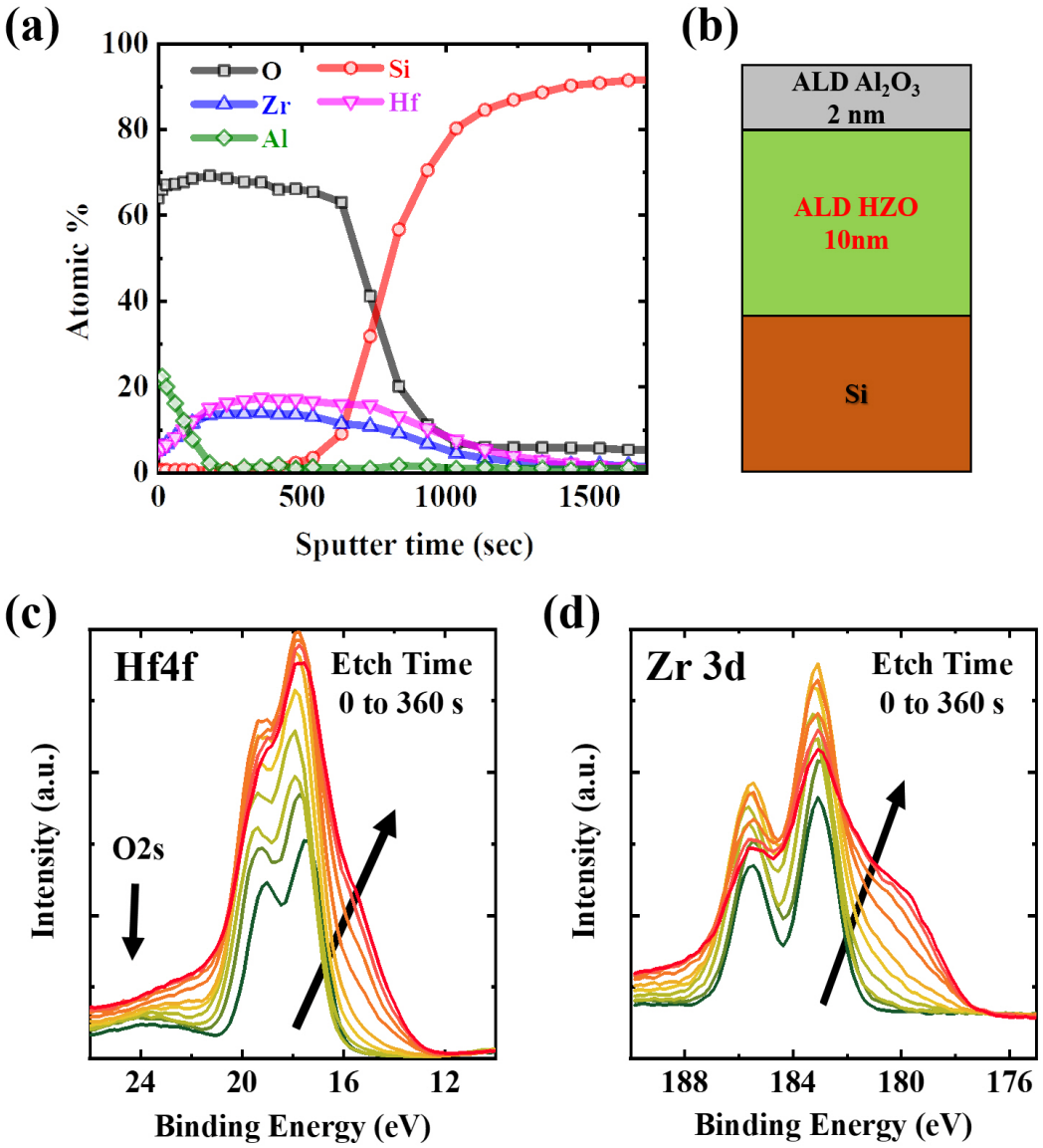

Fig. 2.4. (a) Atomic compositional ratio acquired by ion sputtering the sample (shown in (b)) for depth profiling using AR-XPS. (c) Hf4f and (d) Zr 3d XPS peaks as a function of etch time. It can be concluded that Hf:Zr=1:1 from (a) since during the first 120 seconds of sputtering, Hf:Zr=1:1 and slightly higher Hf % after 120 seconds could be due to increasing O2s peak in (c). Detailed % can be found in Table 2.1.

(AR-XPS) with ion etching capability is used, depth profiling at depths deeper than 10 nm or even specific depths shallower than 10 nm can be studied. To avoid the need to etch top 20 nm of TiN layer as seen from XRD sample (Fig. 2.3 (b)), only 2 nm of Al_2O_3 capping on top of 10 nm HZO was deposited. Fig. 2.4 (a) is the depth profiling of atomic % within the layer stack. Al peak decreases as the top capping Al_2O_3 layer is etched away but Hf and Zr peak increase simultaneously. After approximately 600 seconds of etching, Si peak rises implying the whole 12 nm of oxide stack has been etched away. Within the HZO layer, it seems as if the Hf % is higher than Zr. However, this is due to deconvolution error induced by the proximity of O2s signal near Hf 4f peak as shown in Fig. 2.4 (b). Due to this unwanted O2s peak interfering with Hf4f peak, Hf atomic % could have been over-estimated. With increasing etch time, both metallic Hf and Zr peaks at lower binding energy levels can be found (noted with black arrows) in Fig. 2.4 (c) and (d). Table 2.1 shows the detailed atomic % of the elements acquired within the first 120 seconds of etching from the surface. It can be seen from the first $0 \sim 120$ seconds that Hf:Zr ratio is indeed 1:1 within the region where Al_2O_3 layer still exists and O2s peak is weak. Therefore, in this thesis

Table 2.1.
Atomic % of O, C, Si, Zr, Hf and Al with increasing etch time as shown in Fig. 2.4 (a).

Sputter Time (s)	**O (%)**	**C (%)**	**Si (%)**	**Hf (%)**	**Zr (%)**	**Al (%)**	**Hf/Zr**
0	63.7	5.0	0.3	4.7	4.7	21.5	0.99
15	65.8	0.8	0.2	5.6	5.5	22.1	1.01
30	66.9	0.6	0.3	6.3	6.3	19.6	0.99
60	67.1	0.9	0.3	7.9	8.0	15.9	0.98
90	67.6	1.1	0.3	9.7	9.6	11.8	1.01
120	68.4	1.2	0.2	11.6	11.2	7.4	1.04

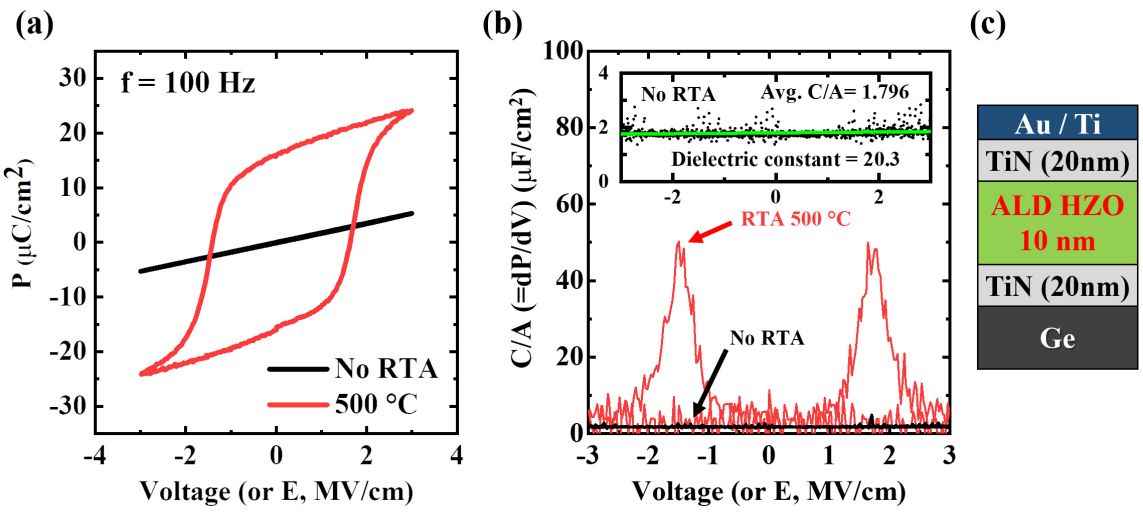

Fig. 2.5. Polarization - Electric field curve measured with ferroelectric tester. (a) Polarization before and after RTA reveals clear transition from dielectric HZO to ferroelectric HZO. (b) When the P is differentiated with V (dP/dV), capacitance density (μF/cm^2) can be acquired. Inset shows the capacitance density of the sample before RTA. (c) Structure of the ferroelectric sample measured in this figure.

unless otherwise specified, HZO is deposited with Hf:Zr ratio of 1:1 and HZO means $Hf_{0.5}Zr_{0.5}O_2$.

Ferroelectricity can be further confirmed electrically using polarization as a function of electric field graph (P-E). P-E curve can be acquired by either applying a triangular voltage [81] or using a commercially available ferroelectric tester. Polarization curve extracted with the ferroelectric tester (Model: RT66C) from Radiant technologies is presented in Fig. 2.5 (a). The P-E curve before RTA crystallization shows a constant linear line (Fig. 2.5 (a), black line). Taking the derivative of polarization with respect to voltage, Fig. 2.5 (b) can be acquired which is the ferroelectric capacitance (μF/cm^2). Without RTA, the capacitance was linear-fitted to be 1.796 μF/cm^2 which corresponds to dielectric constant of 20.3 (inset of Fig. 2.5 (b)). Coercive field (E_C) of 1.8 MV/cm and remnant polarization (P_r) of 22 μF/cm^2 were

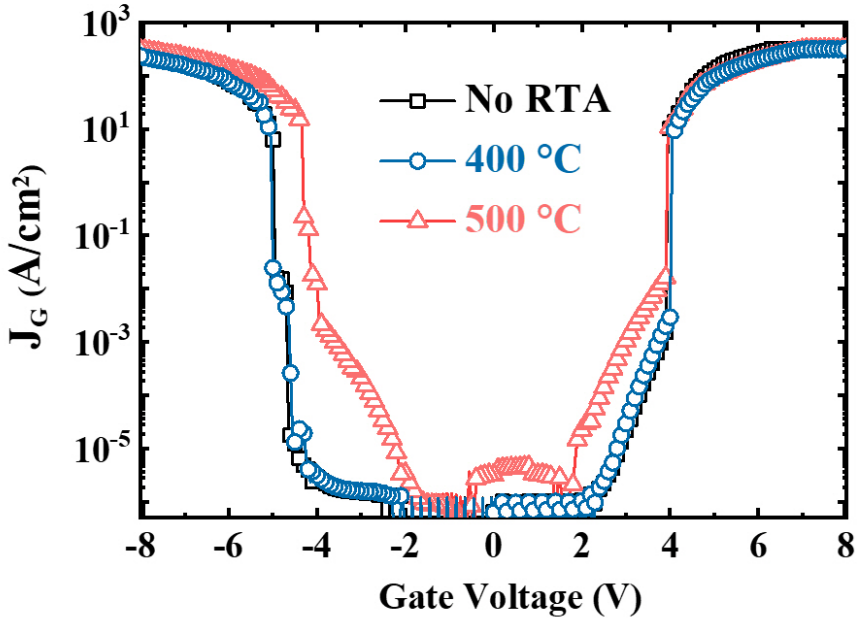

Fig. 2.6. Leakage current of the gate stack seen in Fig. 2.5 (c). RTA with higher temperature increases the leakage current. Breakdown voltage of HZO (10 nm) is extracted to be approximately ± 5 V.

extracted from the P-E curve when the voltage was swept in the range of ± 4 V (figure not shown) [43]. Two large spikes visible in Fig. 2.5 (b) is due to ferroelectric switching near the coercive field. This shows the strong ferroelectricity within the HZO film and when stabilized with positive dielectrics, the unstable negative capacitance behavior can be stabilized to result in capacitance boost and SS reduction. Without such stabilization, NC effect is very difficult to be directly probed [82].

Leakage current of the HZO film was also measured (Fig. 2.6) using the same structure shown in Fig. 2.5 (c). Increasing the annealing temperature increases the leakage current as HZO film crystallizes further. Later in the chapter, when fabricating germanium FeFETs and NCFETs, additional dielectric layers were deposited in series with HZO. Therefore, the breakdown voltages of these FeFET utilizing 10 nm of HZO is much higher than the breakdown voltage seen in Fig. 2.6.

2.2.2 Dry etching of HZO

With stabilized ALD deposition recipe for HZO, integration set up of HZO into the germanium platform is needed. One important fabrication step is the etching of HZO film. Since HZO is basically the mixture of HfO_2 and ZrO_2, dry etch recipe which was used for Al_2O_3 and germanium etching was first tested.

As shown in Fig. 1.3, recessed S/D strategy was employed in the Ge MOSFETs. To etch the S/D region of Ge, oxide stack (HZO, Al_2O_3, GeO_x) should first be etched. However, for possible applications towards gate-all-around (GAA) FETs using ALD deposited metals such as WN or TiN, 2 step etching of ALD metal and oxide is needed. For our group's reported works on germanium FinFETs [15] and nanowires [13], a single etch recipe based on BCl_3 was used. However, if only one recipe is used to etch various kinds of oxides and ALD-metals, the etch time should be very precisely calculated for each and every layer in the stack taking into account respective etch-rates. If ALD metal could be selectively etched without etching the underlying oxides,

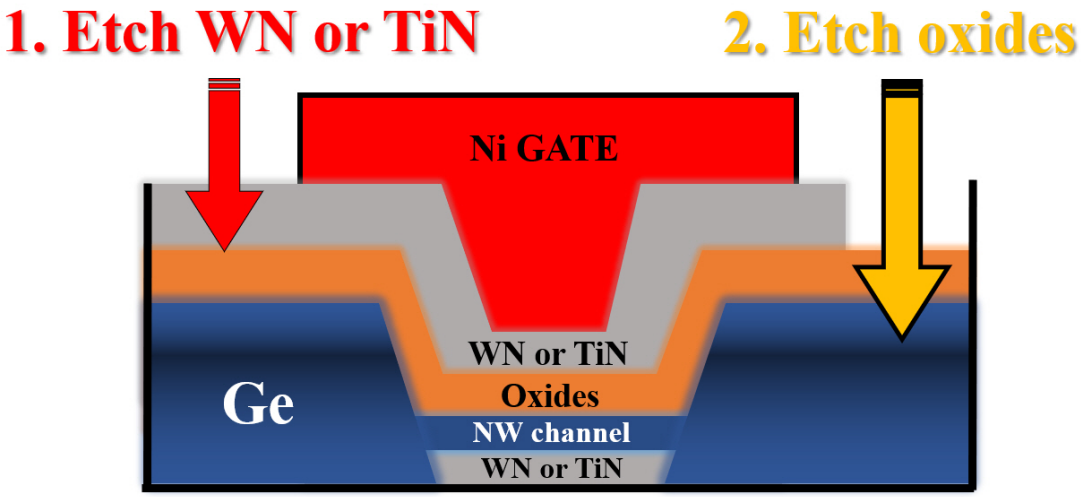

Fig. 2.7. Etching recipe needed for fabrication of ALD-deposited Metal/HZO/Al_2O_3/GeO_x/Ge gate stack. If step 1 can be highly selective, oxides can be used as an etch-stop layer.

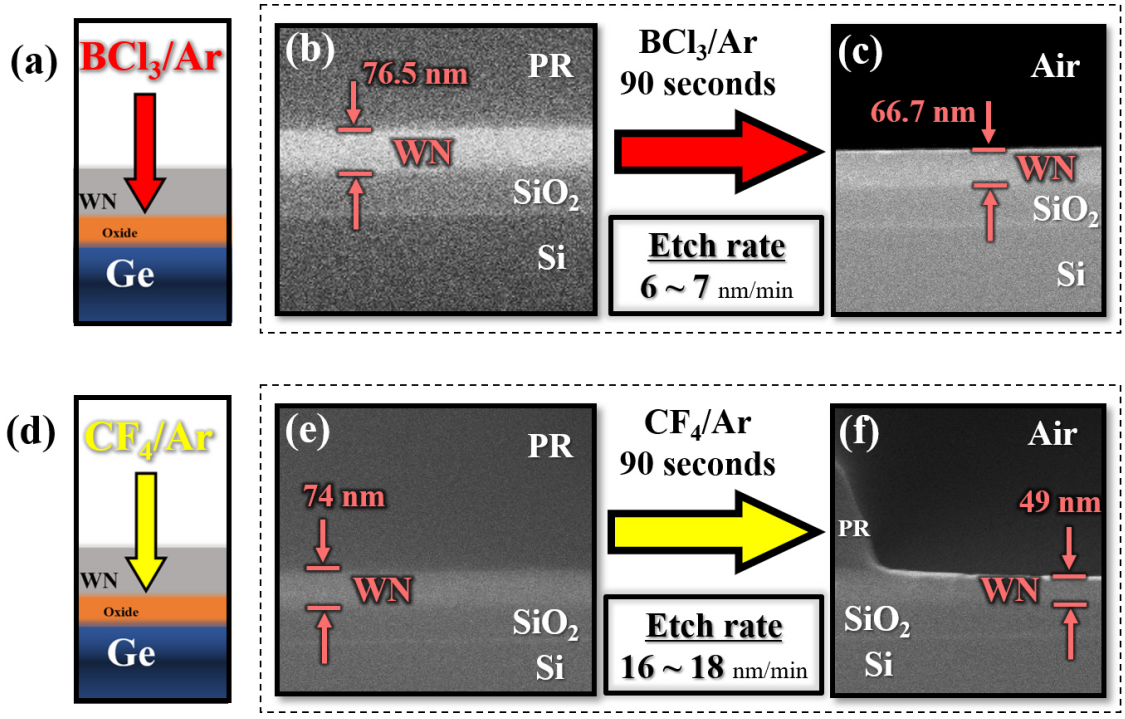

Fig. 2.8. (a)-(c) show the structure of the WN/oxide/Ge stack tested with BCl_3/Ar recipe. (d)-(f) are tested with CF_4/Ar recipe. Both gases etch WN film.

then the first recipe could be used a little bit longer to over etch and use the oxides as the etch stop. Then, the second etch recipe for the oxides could be employed to continue etching down into germanium substrate where the actual metal contacts are made.

First, the BCl_3/Ar-based etch recipe was tested to etch the ALD deposited WN, TiN and HZO. Fig. 2.8 (a)-(f) show the test structure (WN/Oxide/Ge) and its etch profile. Both gases were found to etch WN but CF_4/Ar recipe etched much faster than BCl_3/Ar. TiN (images not shown) were also tested using the similar sets of tests and the etch rate of TiN using BCl_3/Ar and CF_4/Ar were found to be approximately $8 \sim 9$ nm/min and 10 nm/min, respectively.

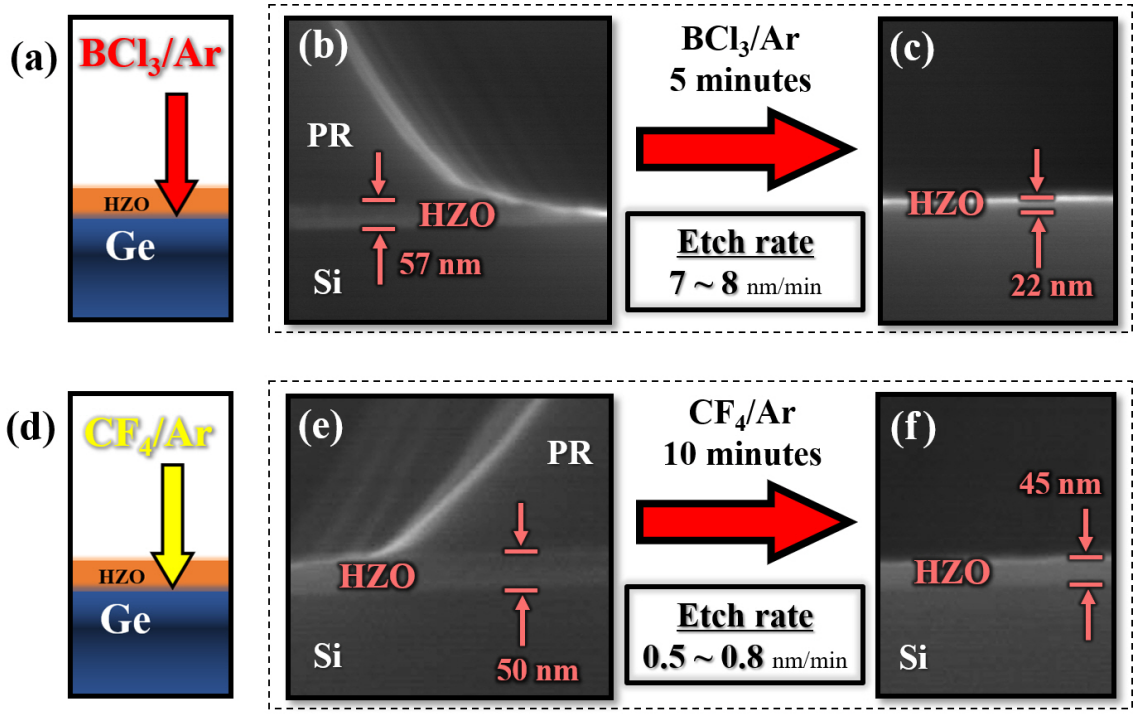

Fig. 2.9. (a)-(c) show the structure of the HZO/Ge stack tested with BCl_3/Ar recipe. (d)-(f) are tested with CF_4/Ar recipe. CF_4/Ar recipe has significantly slower HZO etch rate.

HZO was also tested with these 2 different recipes to see if there exists a significant etching selectivity between ALD nitride metals. It was found that BCl_3/Ar etches HZO at moderate etch rate like etching ALD nitride metals. However as observed in Fig. 2.9 (f), CF_4/Ar etches HZO very slowly suggesting high etch selectivity compared to ALD nitride metals. For GAA fabrication using ALD nitride metal and HZO, slight over-etching of nitride metal using CF_4/Ar can be done first and subsequent etching of HZO and Ge can complete the 2-step etching process.

2.3 Germanium FeFET

Using the ALD HZO and dry etch recipes optimized in the previous section, germanium FeFETs were fabricated. HZO with Hf:Zr ratio of 1:1 was deposited after

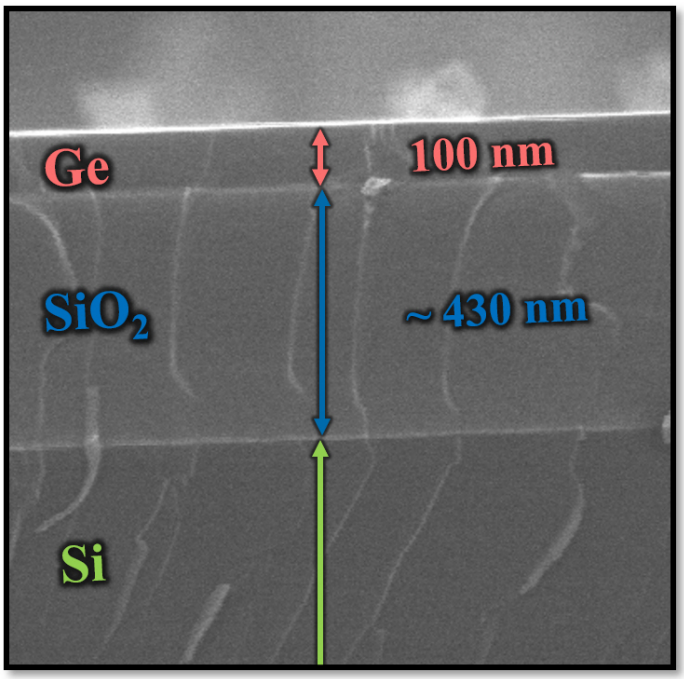

Fig. 2.10. GeOI wafer used for fabrication of germanium FeFETs. Top germanium layer thickness is 100 nm and the underlying SiO_2 has thickness of $\sim$ 430 nm.

defining germanium fin structures. Germanium-on-insulator (GeOI) wafer purchased from IQE was used. Cross-sectional SEM image of the used GeOI wafer is shown in Fig. 2.10. Under the thin germanium layer (100 nm), buried oxide (BOX, SiO_2) is visible and the thickness was measured to be approximately 430 nm.

Solvent and acid cleaning were done first which was followed by the first e-beam lithography of mesa isolation and alignment marks. The alignment marks for the e-beam were defined using SF_6-based dry etching of germanium layer. Before the ion implantation, 10 nm Al_2O_3 was deposited with ALD. This Al_2O_3 serves as a protection layer that prevents damage to the crystalline germanium layer due to ion implantation. Also, it helps control the projected range (R_p) of the implanted ions. P-type implantation using BF_2^+ with dose of 4×10^{15} cm^{-2} at power of 15 keV was done. The sacrificial Al_2O_3 was then removed and the sample was patterned with e-beam for definition of channel lengths. As mentioned earlier in chapter 2,

Table 2.2.
Fabrication process of germanium ferroelectric FinFET in detail.

Step	**Remarks**
1. Wafer cleaning, solvent and acid	GeOI ($Ge/SiO_2/Si$)
2. Mesa isolation definition	Dry Etching (SF_6)
3. P-type ion implantation	BF_2, 4×10^{15} cm^{-2}, 15 keV
4. Channel recess for fin height definition	Dry Etching (SF_6)
5. Fin patterning	Dry Etching (SF_6)
6. Gate oxide deposition (ALD)	
a) Al_2O_3	1 nm, 250 °C
b) Post Oxidation	RTA, O_2, 500 °C, 30 seconds
c) HZO deposition	10 nm, 250 °C
d) Al_2O_3 capping	1 nm, 250 °C
7. HZO crystallization (PDA)	RTA, N_2, 500 °C, 60 seconds
8. Source, drain recess	Dry Etching (BCl_3/Ar)
9. Ni contact deposition	Evaporation
10. Ohmic annealing	RTA, N_2, 250 °C, 30 seconds
11. Gate, source, drain pad deposition (Ni)	Evaporation

recessed channel scheme was employed for all the devices mentioned throughout this thesis. The SF_6-based dry etching of germanium mentioned in section 2.4 was used for channel recess and fin definition. By precisely controlling the etch time, channel height (fin thickness) was thinned down to approximately 22 nm as found in Fig. 2.11 (a). Fins were connected in parallel to form a single device (Fig. 2.11 (b)-(e)).

After definition of the fin structure, 1 nm of ALD Al_2O_3 was deposited and post oxidation in RTA chamber (O_2, 1 atm) at 500 °C for 30 seconds was done. Nanometer-thin GeO_x formed under the Al_2O_3 improves the interface quality between the germanium channel and the high-k oxides [12, 30, 83]. Then, 10 nm of HZO was deposited

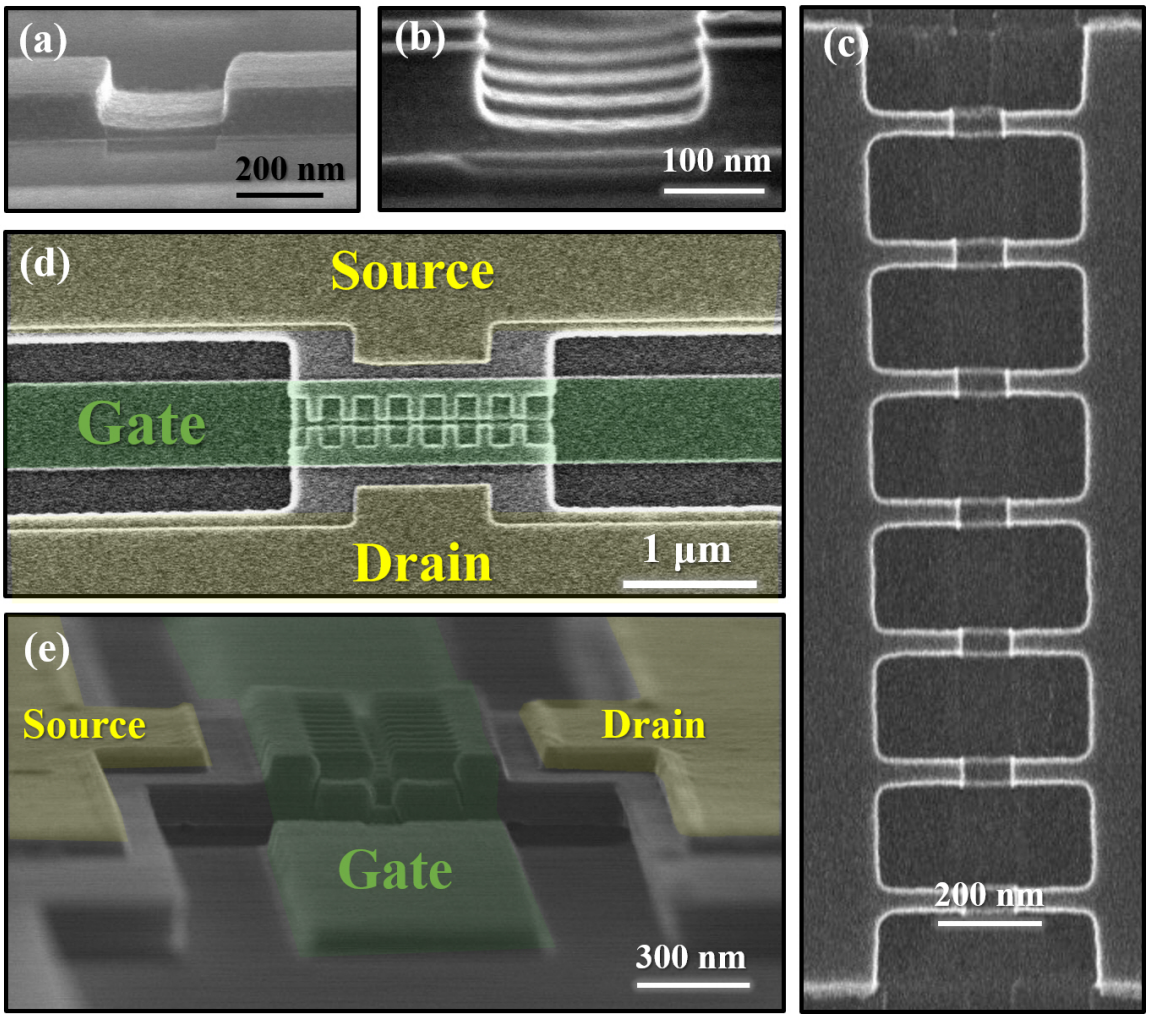

Fig. 2.11. (a) Recessed channel with fin height of approximately 22 nm. (b) Multiple parallel fins defined by SF_6-based dry etching that was used for the channel recess. (c) Top-view of fabricated parallel fin structures shown in (b). (d) False-colored SEM image showing multiple parallel fins seen from top. Gate, source and drain metallization was done. (e) Side view of (d) after all fabrication process

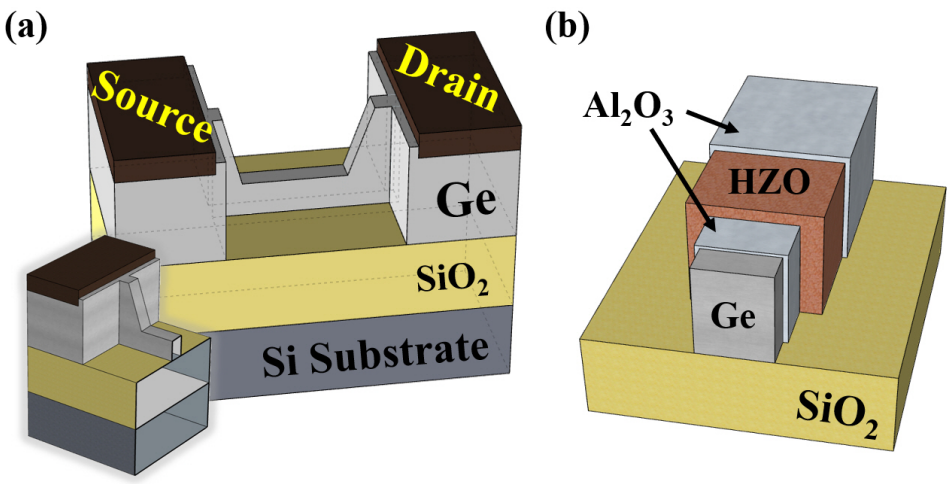

Fig. 2.12. (a) Recessed channel with fin height of approximately 22 nm. (b) Multiple parallel fins defined by SF_6-based dry etching that was used for the channel recess. (c) Top-view of fabricated parallel fin structures shown in (b). (d) False-colored SEM image showing multiple parallel fins seen from top. Gate, source and drain metallization was done. (e) Side view of (d) after all fabrication process.

at 250 °C as described in subsection 3.2.1. In-situ Al_2O_3 (1 nm) capping layer was deposited on HZO to prevent the exposure of HZO film to the atmosphere throughout rest of the fabrication processes and to promote the orthorhombic crystallization of HZO. The oxide gate stack was annealed in RTA chamber at 500 °C for 60 seconds with only N_2. As discussed earlier, HZO film becomes ferroelectric due to this step. HZO/Al_2O_3/GeO_x/Ge was etched with BCl_3/Ar dry etch recipe to make the optimum contact between the germanium and Ni [13]. Ohmic annealing (RTA chamber, 250 °C, N_2, 30 seconds) was done followed by deposition of gate, S/D metal pads. Final device SEM images after metallization can be found in Fig. 2.11 (d) and (e). 3D structures of fabricated FinFET structure is visible in Fig. 2.12 (a) and (b). Al_2O_3 layers are cladding the HZO layer in the middle of the gate oxide stack. Key processes for the fabrication are summarized in Table 2.2.

Ferroelectric material intrinsically possesses the voltage hysteresis as shown in Fig. 1.7 (a) and Fig. 2.13. The energy barrier that exists between the local minima in

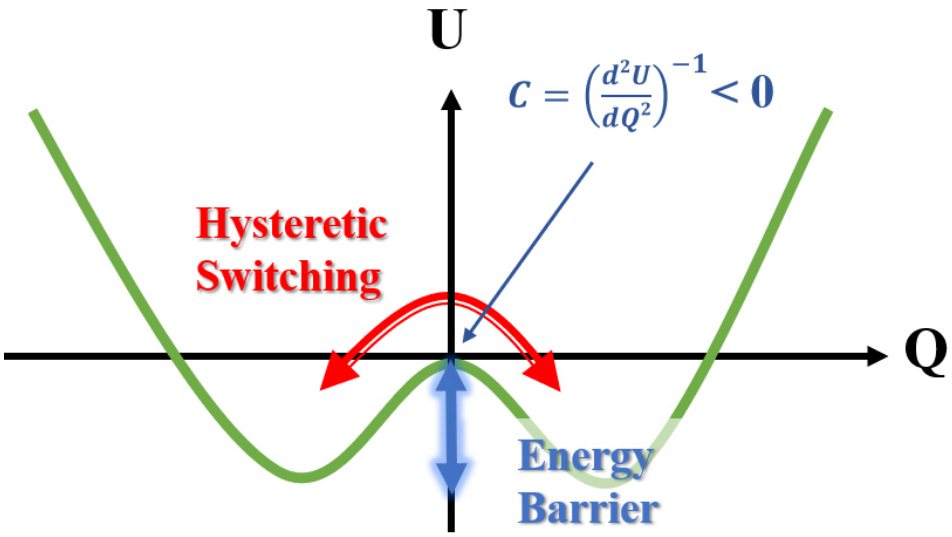

Fig. 2.13. Origin of voltage hysteresis in a ferroelectric material. Energy barrier is where the unstable negative capacitance ($(d^2U/dQ^2)^{-1} < 0$) region exists.

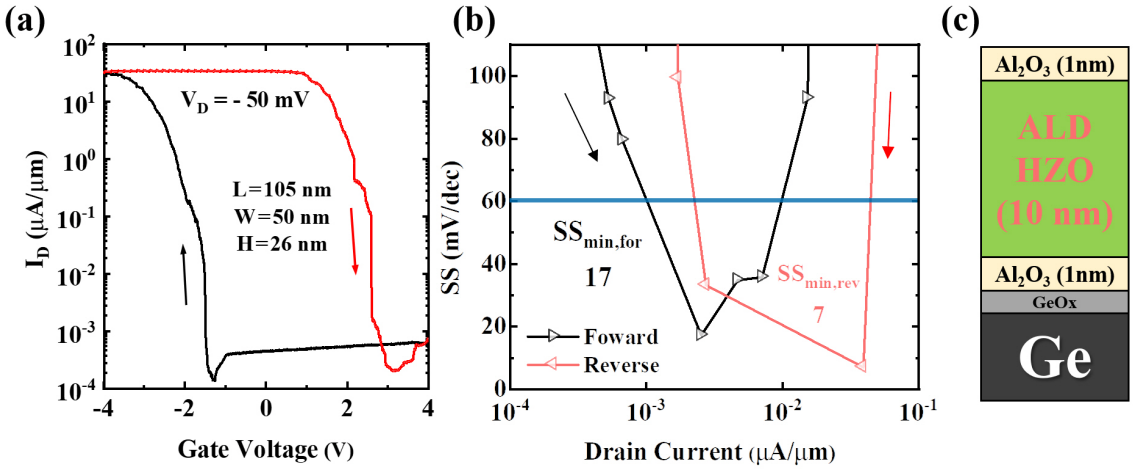

Fig. 2.14. (a) Transfer curve (I_D-V_G) of a typical Ge FeFET at low V_D = -50 mV. Ferroelectric hysteresis of approximately -4 V (clockwise for PMOS) can be seen. (b) SS as a function of drain current.

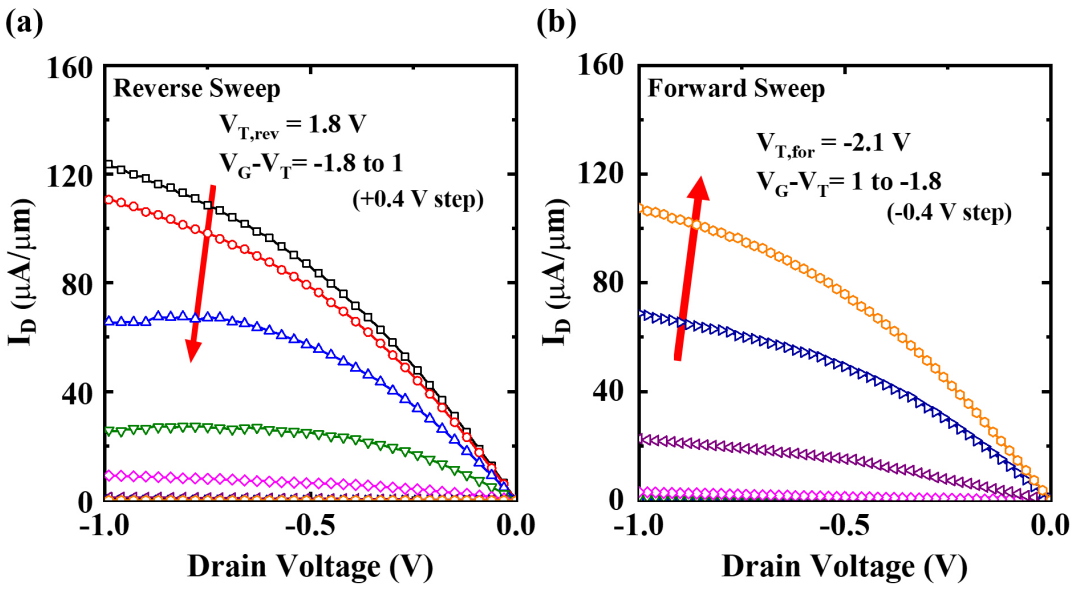

Fig. 2.15. V_G-V_T was swept from -1.8 to 1 V for the reverse sweep and 1 to -1.8 V for the forward sweep. Note that due to large voltage hysteresis, $V_{T,for}$ and $V_{T,rev}$ is apart from each other by $\sim$ 4 V.

the energy (U) landscape. If this energy barrier can be effectively stabilized and thus the negative capacitance region can be utilized, hysteresis-free operation (NCFET) is possible. This will be discussed in the following chapter.

Transfer characteristics of a germanium FeFET is shown in Fig. 2.14 (a). Large voltage hysteresis typically found from a ferroelectric oxide is visible which corresponds to hysteresis found in P-E curve Fig. 2.5 (a). SS was extracted from the transfer curve and was plotted as a function of drain current (Fig. 2.14 (b)). Output curves were measured in both reverse and forward sweep directions as seen in Fig. 2.15 (a) and (b), respectively. It can be seen that the turn on voltage is asymmetrical in reverse and forward sweep consistent with threshold voltages seen in Fig. 2.14 (a). This is not a favorable property for logic device application.

2.4 Time Response of Polarization

Another issue that is worth focusing is the ultrafast time response of polarization switching kinetics in ferroelectric materials [47, 49, 84–87]. Study of time response is not only helpful in the field of FeRAM but also could be valuable for insights into

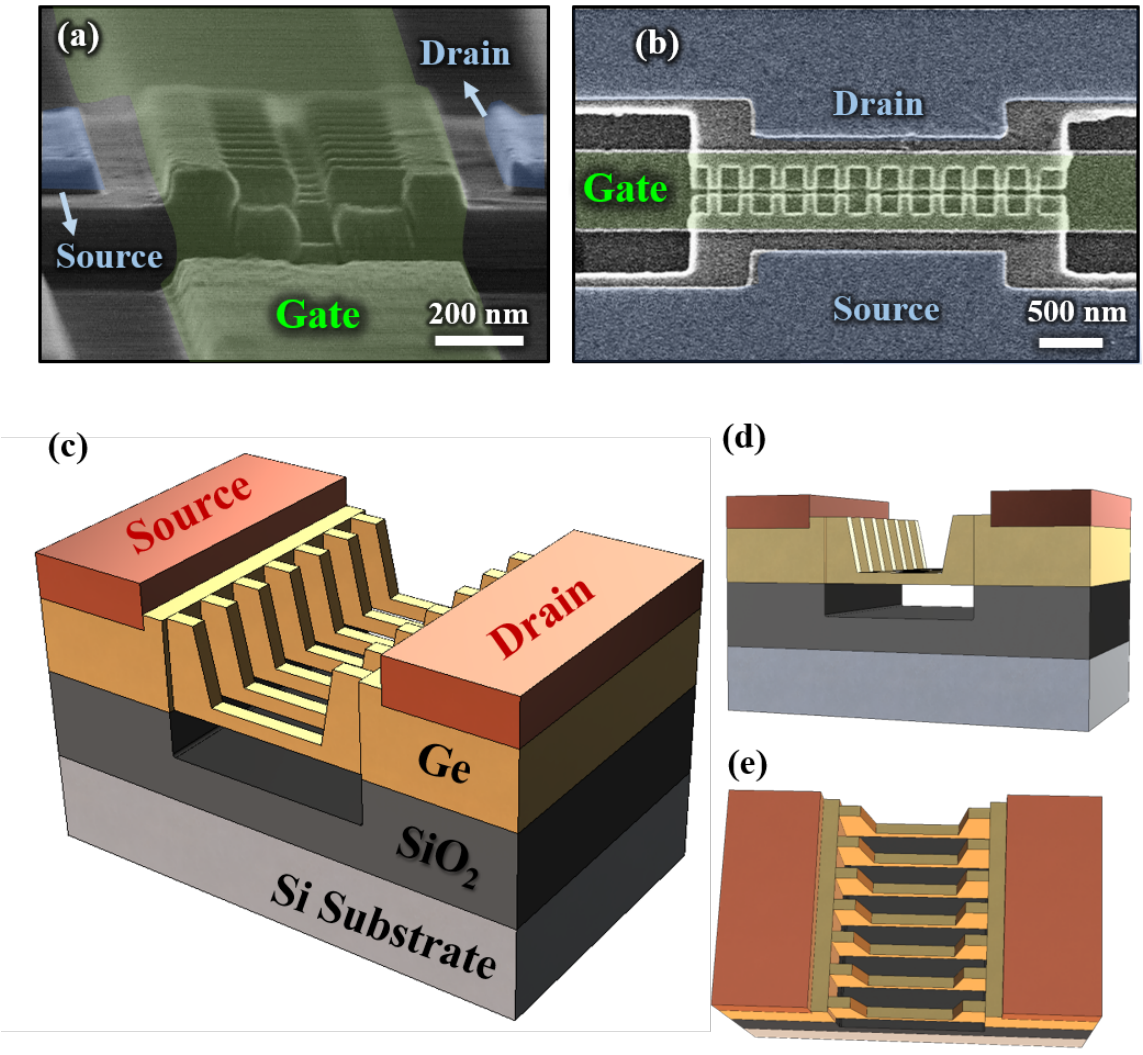

Fig. 2.16. False-colored SEM images of fabricated germanium FE NWFETs viewed from (a) side and (b) top. Parallel nanowires form a single device. (c), (d) and (e) show the 3D structure of the fabricated devices from various viewing angles.

the operation capability of NCFETs [88–92]. Furthermore, polarization switching properties can be used in application towards the neuromorphic synaptic devices [53, 59, 60]. To study the time response of the polarization switching, the germanium nanowire FeFETs were used. The fabrication of nanowires is the same as Table 2.2 except the etching of SiO_2 below the fins with HF before ALD oxide deposition. SEM images and 3D structure images of the fabricated nanowire device are found in Fig. 2.16 (a)-(e).

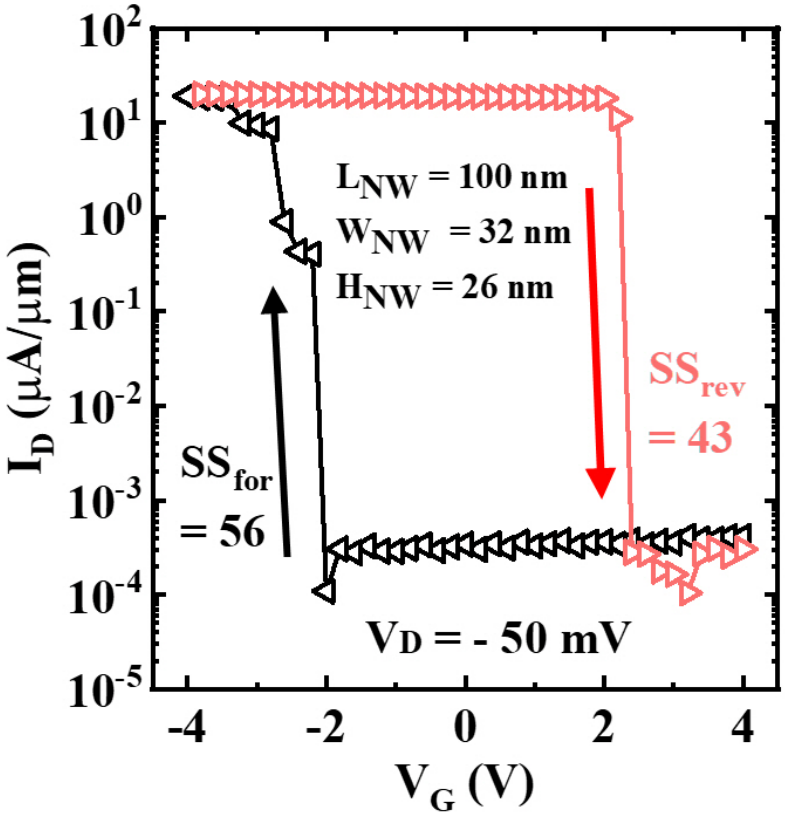

Fig. 2.17. Transfer curve (I_D-V_G) of a Ge FeFET at low V_D = -50 mV used for time response study. Ferroelectric hysteresis of approximately -4 V (clockwise for PMOS) can be seen.

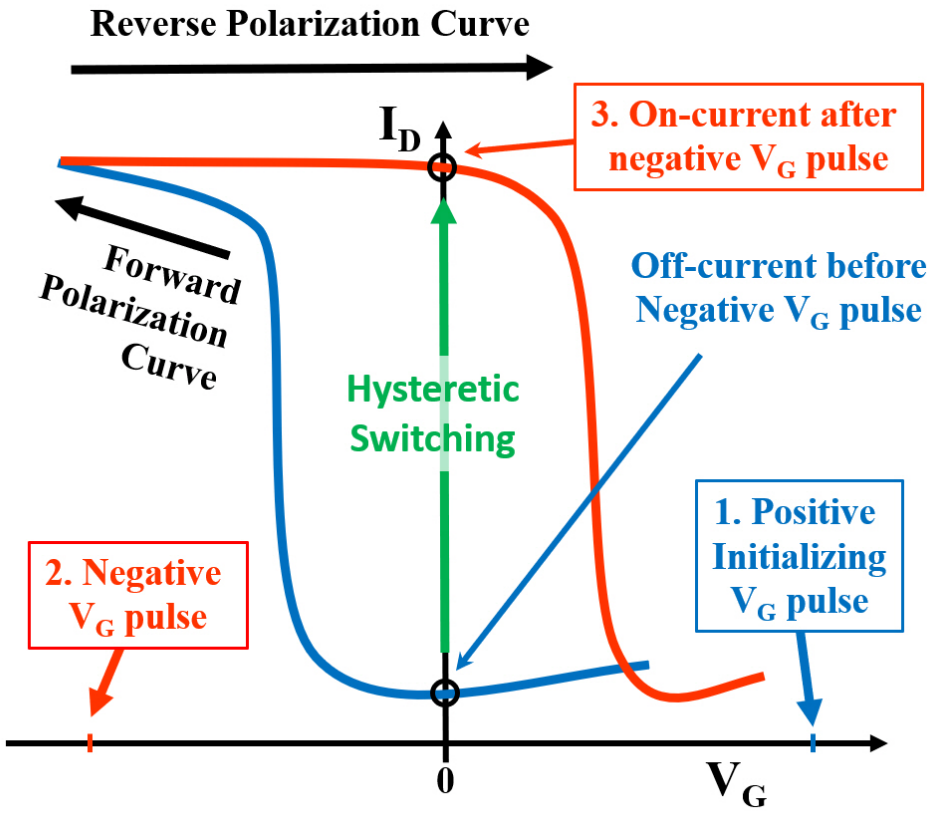

Fig. 2.18. Polarization switching in a ferroelectric oxide. Positive initialization assures the device to follow the forward polarization curve. Subsequent negative V_G pulses with various pulse widths and levels cause polarization switching.

Transfer curve (I_D-V_G) of the germanium ferroelectric nanowire devices (Ge FE NWFET) show abrupt switching both in forward and reverse directions. Large ferroelectric hysteresis can be seen in Fig. 2.17. The conceptual image describing the polarization switching in a ferroelectric oxide is depicted in Fig. 2.18. Initialization pulse (+5 V) first applied to the FeFET's gate ensures the polarization state to start from the same condition (following the forward polarization curve) before the negative pulses were supplied to the gates. When the negative gate voltage pulse is supplied, the FeFET undergoes polarization switching and this can be monitored in real-time through oscilloscope in the form of drain currents. When it is fully polarized in the

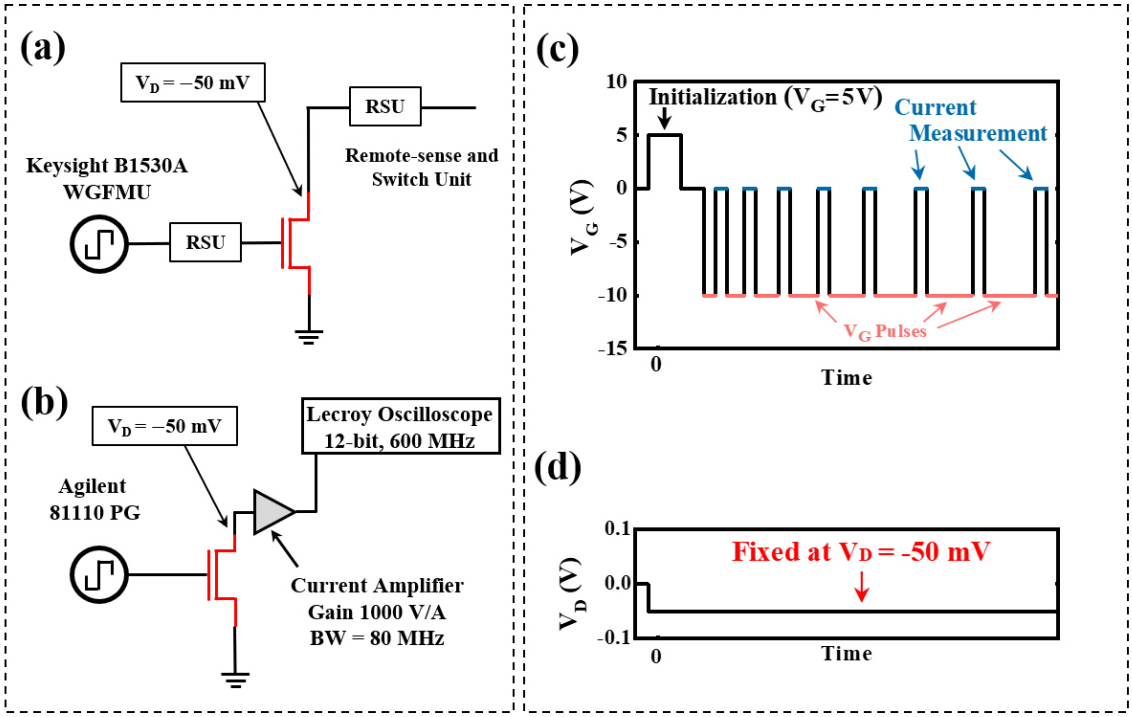

Fig. 2.19. (a) Measurement set-up used for pulse measurement on Ge FeFET. Waveform generator that generates pulses down to approximately 100 ns at maximum of -5 V was used for low voltage measurements. (b) Ultrafast measurement set-up for pulses as short as 3.6 ns and pulse level down to -10 V. (c) and (d) show the pulses that were delivered to the gate and drain of FeFETs, respectively.

opposite polarization state compared to the initial state, the device's drain current curve follows the reverse polarization curve.

To monitor the polarization switching in FeFETs, measurement set-up was prepared as shown in Fig. 2.19 (a) and (b). Low voltage pulse measurement (± 5 V) was done with minimum pulse width of 100 ns using the configuration of Fig. 2.19 (a). Keysight B1530A wave form generator and fast measurement unit (WGFMU) was used as a pulse generator and remote-sense and switch unit (RSU) were used to deliver and measure the signals. Measurement were taken place after each negative V_G pulses for 100 μs. For larger (± 10 V) and faster pulses (> 3.6 ns), Fig. 2.19 (b)

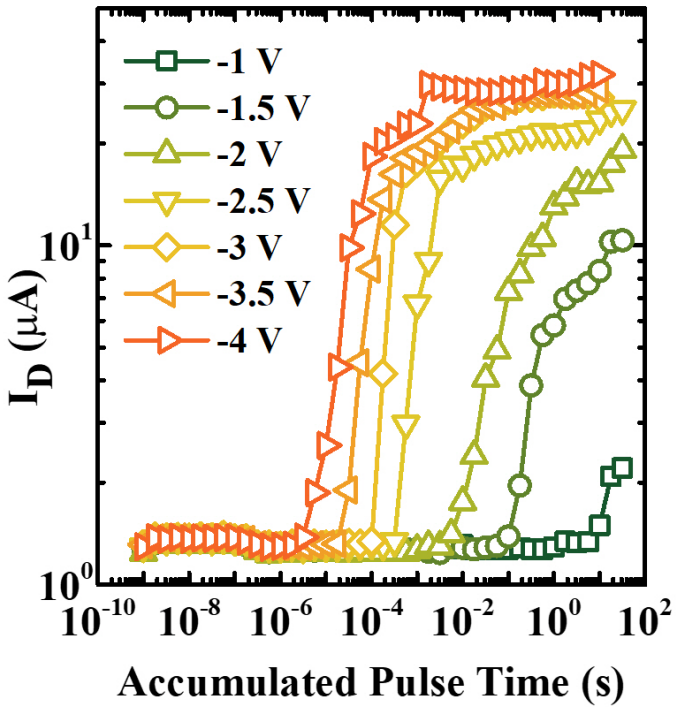

Fig. 2.20. Change in drain currents due to polarization switching using the low voltage set-up shown in Fig. 2.19 (a). Voltage level and pulse time was varied and drain current was monitored after each pulse.

was prepared in collaboration with National Institute of Standards and Technology (NIST). Agilent 81110 pulse generator (PG) was used and current amplifier connected in series with Lecroy oscilloscope monitored the change in drain current in real time. Fig. 2.19 (c) and (d) show the pulses that were applied to the gate and drain of a Ge FE pFinFET. With initialization pulse of 5 V, polarization state was first initialized. Then pulses with logarithmically increasing pulse width were applied to the gate of the FeFET. Pulse level was varied from -1 V to -5 V and the drain voltage was fixed to 50 mV. Change in drain current was monitored as in Fig. 2.20. It was observed that with larger pulse voltage level, faster polarization switching took place. -4 V

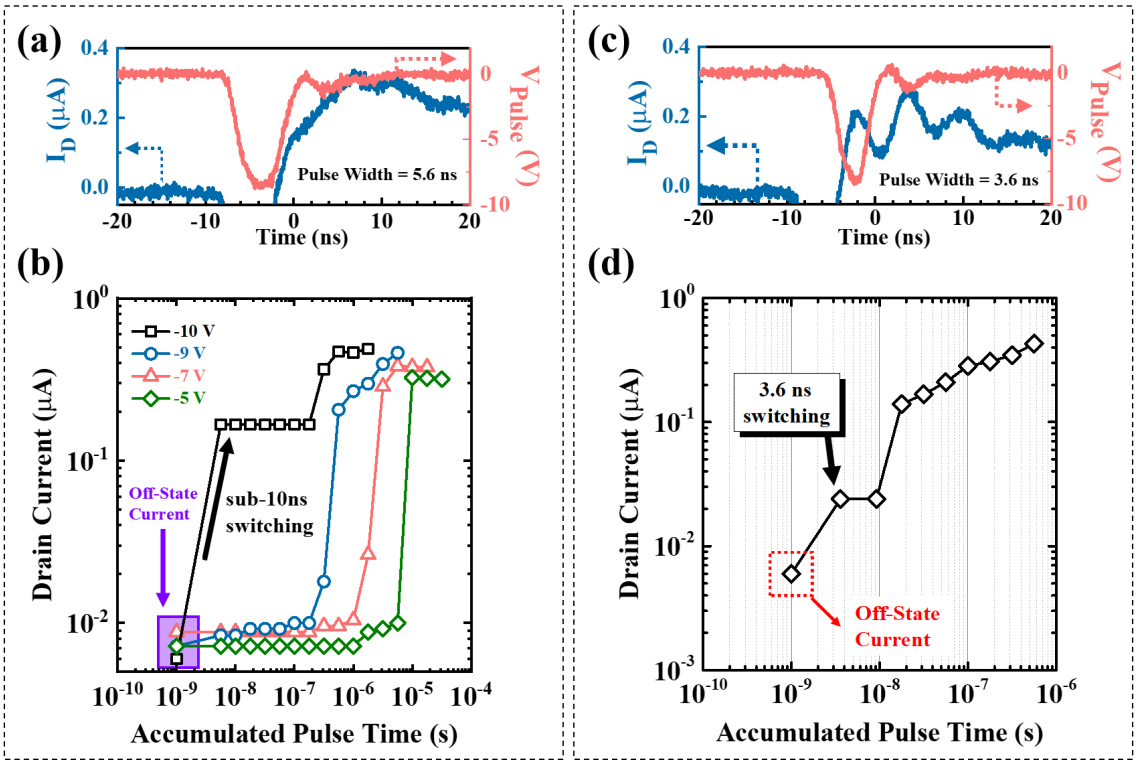

Fig. 2.21. (a) With a 5.6 ns gate pulse, drain current shows abrupt increase from the off-state. (b) As pulse time accumulates, the drain current continuously increases until it maximizes.

pulses showed the fastest polarization switching which started from approximately 1 μs.

To push the HZO's polarization switching capability (pulse width, voltage) beyond the limitations in low voltage set-up depicted in Fig. 2.19 (a), instruments that can generate and monitor higher voltage pulses with nanoseconds of pulse widths were configured as presented in Fig. 2.19 (b). Real-time, oscilloscope-monitored gate voltage and drain current signals is shown in Fig. 2.21 (a). It shows sub-10ns partial polarization switching of FeFET. Note that drain currents were measured with V_D = -50 mV and V_G = 0 V. As monitored, 5.6 ns pulse partially triggered a polarization switching and increased the current significantly from the off-state current. This off-state current is not the actual off-state current of the transistor but the default

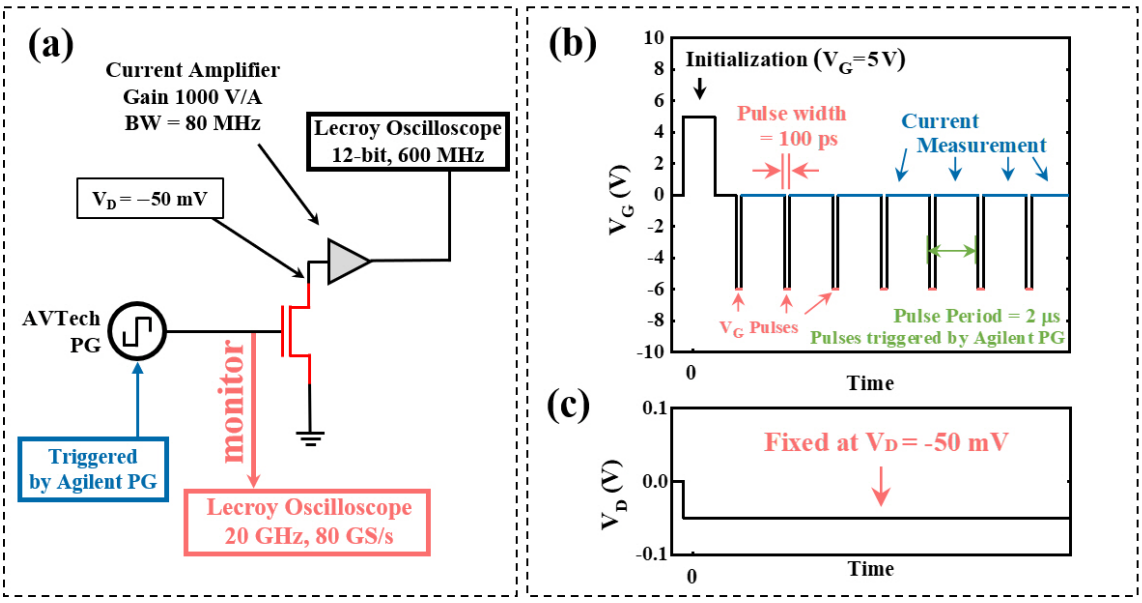

Fig. 2.22. (a) Measurement set-up used for generation and measurement of sub-nanosecond pulses. (b) and (c) show the V_G and V_D profiles during the measurement.

current level present due to the instrument set-up. Current levels smaller than this were considered as the off-state currents.

The fastest polarization switching was monitored to be at the minimum pulse width of the instrument which is 3.6 ns (Fig. 2.21 (c) and (d)). The minimum pulse width that Agilent 81110 PG could generate was 3.6 ns since the rise and fall time is 1.8 ns each. Even at this limit, detectable current increase due to polarization could be observed and this current level was maintained even after tens of seconds after the switching. The retention time of this current was not further studied but it did not fade away even after several tens of seconds from pulsing.

Although sub-10ns polarization switching was observed, faster pulses can be generated going well below 10 ns reaching 0.1 ns (or 100 ps). Special set-up (Fig. 2.22 (a)) that generates 100 ps pulses was configured using AVTech PG and a Lecroy oscilloscope in series with current amplifier. AVTech PG was triggered by another PG

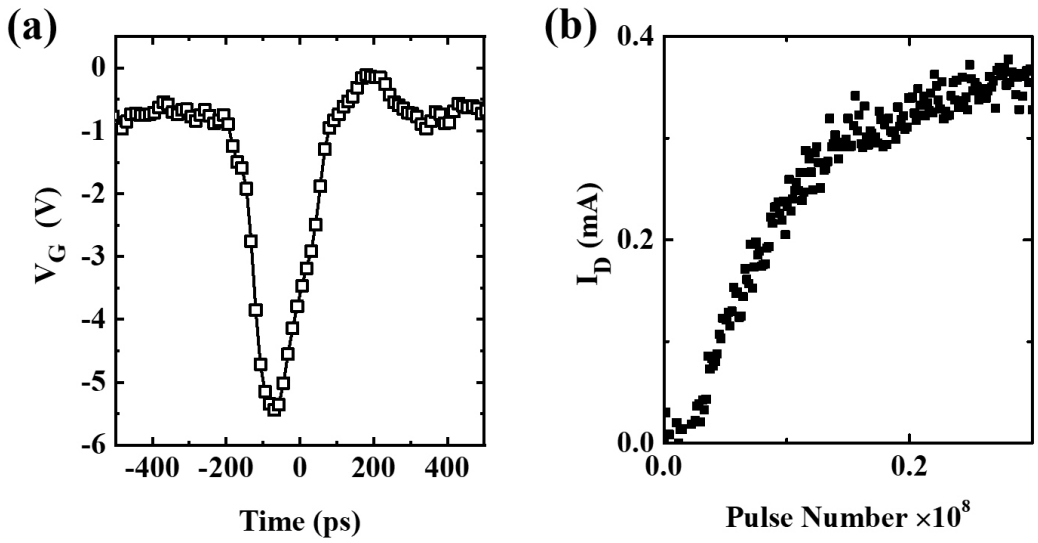

Fig. 2.23. (a) Measurement set-up used for generation and measurement of sub-nanosecond pulses. (b) and (c) show the V_G and V_D profiles during the measurement.

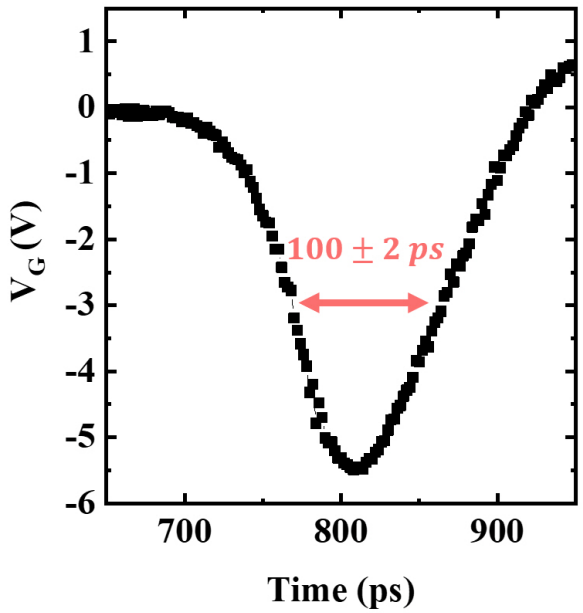

Fig. 2.24. More accurate measurement of generated 100 ps pulse with sampling scope.

that generates pulses every 2 μs (duty cycle = 0.005 %). Current was measured using V_G and V_D profiles shown in Fig. 2.22 (b) after every 100 ps pulse with pulse voltage of approximately -6 V. Fig. 2.23 (a) is the oscilloscope-measured real-time ultrafast pulse with pulse width of 100 ps. It may seem that the pulse width of this real-time measured signal is larger than 100 ps. However, the oscilloscope used for real-time monitoring operates at only 80 GS/s (12.5 ps interval) rate which is not capable of differentiating 100 ps and 120 ps. This real-time scope monitoring was used only to confirm that pulses were supplied without large distortions. To measure the 100 ps pulses more accurately, signal can be fed into sampling scope which has much larger sampling size. As presented in Fig. 2.24, actual signal generated and delivered to the device's gate is in fact 100 ps. Unfortunately, noticeable polarization switching was not observed with a single 100 ps pulse with pulse level of -6 V. However, if the device was delivered with pulse train of 100 ps pulses, gradual polarization switching was observed as seen in Fig. 2.23 (b).

2.5 Stress analysis in ALD HZO

Recently with systematic studies of scaled ferroelectric HZO and anti-aerroelectric (AFE), record high remnant polarization (P_r) in sub-10nm films were observed [93]. Further systematic studies on ultrafast polarization switching could reveal valuable insights and understandings related to HZO-based devices that could be applicable towards FeRAMs, neuromorphic synaptic devices and NCFETs.

Analysis on ferroelectric HZO's realiable switching capability is of great importance considering its possible application towards FeRAM or FeFET-based synaptic devices. To probe its polarization retention capability, Positive-up Negative-down (PUND) fatigue measurement was carried out to extract the remnant polarization (P_r) after continued stress on ALD HZO (Fig. 2.25). It was tested up to 10^9 cycles and P_r was approximately half the initial value. The slight increase in the value until 10^7 cycles may be related to wake-up effect of FE HZO [75, 94].

In addition, voltage hysteresis ($V_{T,forward}$-$V_{T,reverse}$) trend of ALD ferroelectric HZO with respect to negative stress time was measured using a typical negative bias temperature instability (NBTI) set-up as shown in Fig. 2.26 (a) and (b). Full bi-directional sweeps (forward and reverse) were done before applying any negative stress on the gate to record the initial ferroelectric condition of the FeFET as shown in Fig. 2.17. Then stress bias of V_G = -4.5 V was applied with V_D = 0 V. As defined in the inset of Fig. 2.26 (a), V_G step time interval during the bi-directional sweep measurement was approximately 30 ms and the V_D = - 50 mV was maintained throughout the bi-directional V_G sweep. During the recovery phase, V_G = 0 V was applied.

Fig. 2.27 (a) and (b) show the voltage hysteresis (memory window) trend over time acquired during 3 cycles of stress (V_G = -4.5 V) and recovery (V_G = 0 V) where

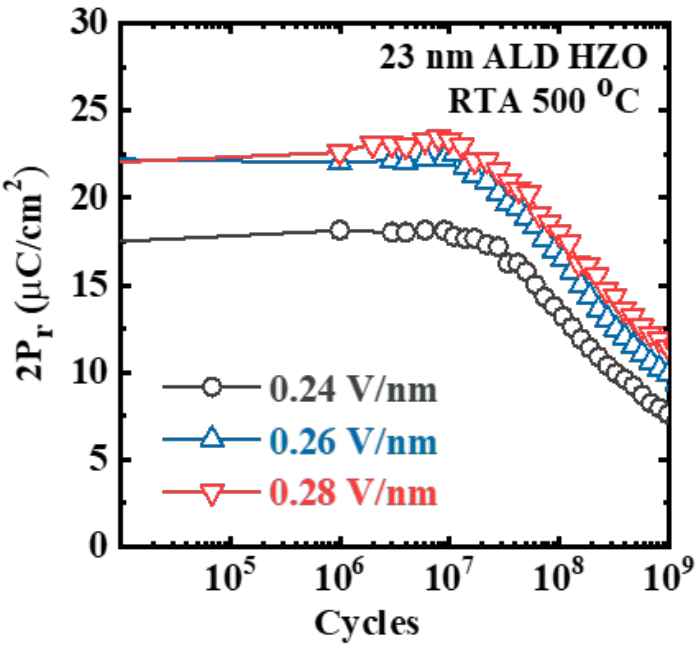

Fig. 2.25. Extracted remnant polarization (P_r) using the typical Positive-up Negative-down (PUND) measurement.

1 cycle consists of 10^4 s of stress and 10^4 s of recovery totalling approximately 17 hours of analysis. It can be seen that such negative stress did not affect the memory window and the hysteresis remained fairly constant at about -4 ∼ -5 V.

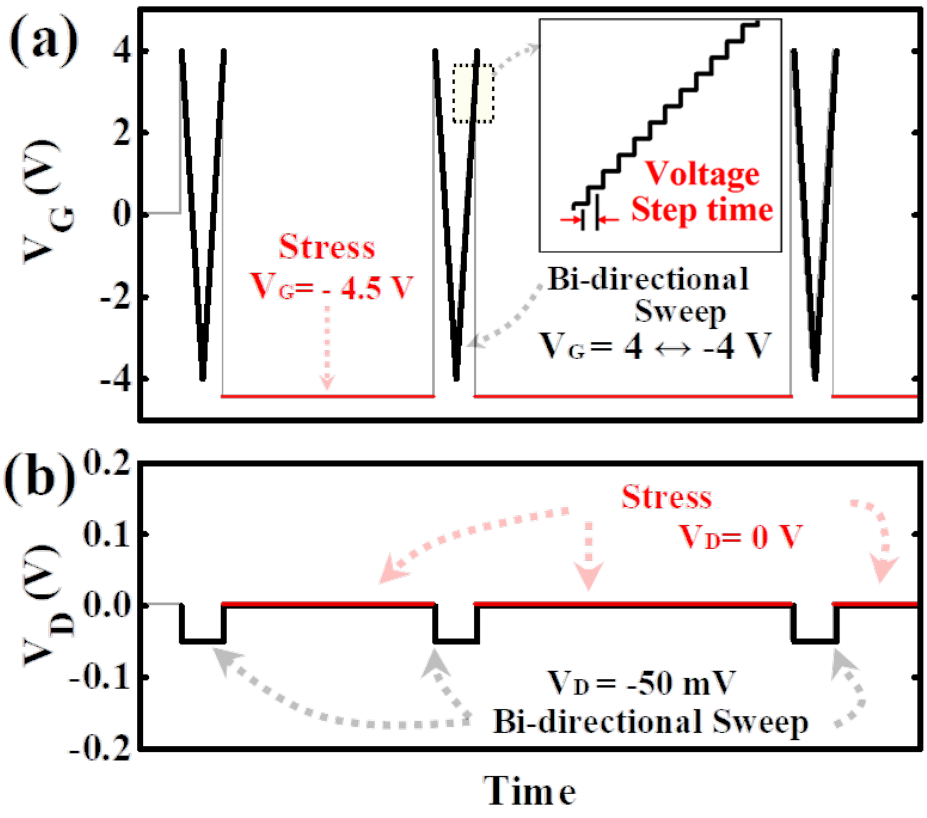

Fig. 2.26. Applied (a) V_G and (b) V_D versus time during the negative V_G stress cycles. V_G is kept at 0 V during recovery cycles.

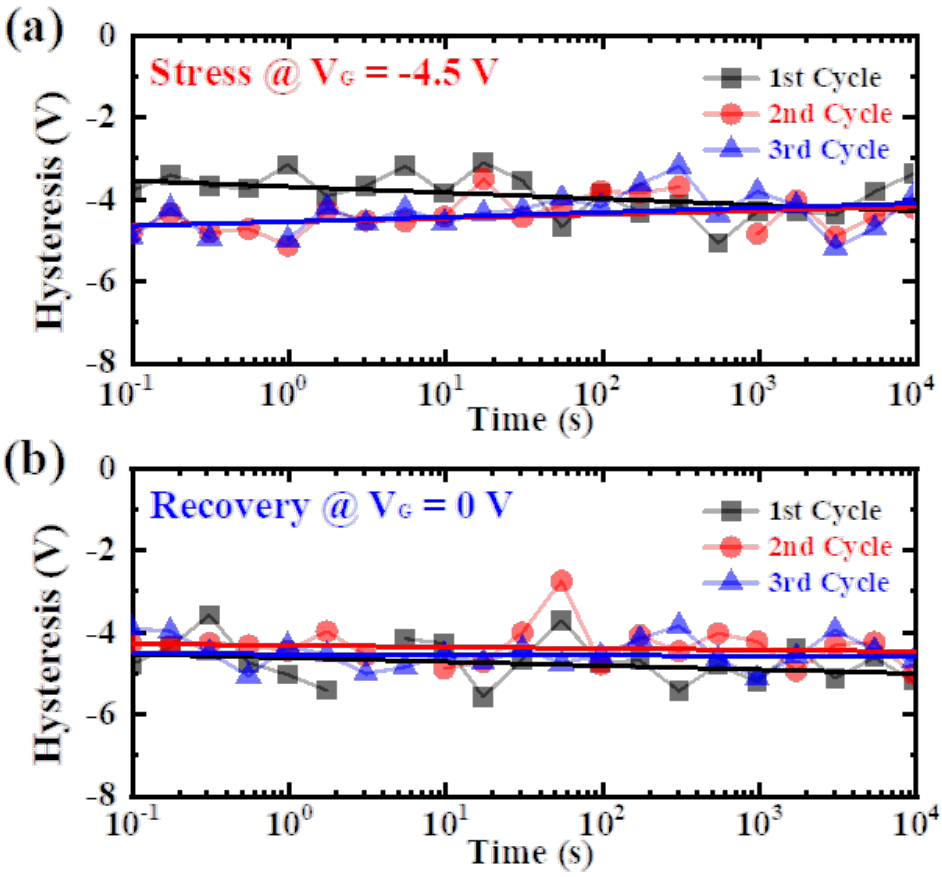

Fig. 2.27. Hysteresis ($V_{T,forward}$-$V_{T,reverse}$) trend during 3 cycles (10^4 seconds per cycle) of (a) negative stress and (b) recovery. V_T was extracted from constant I_D = 100 nA/μm.

3. GE NCFET TOWARDS STEEP-SLOPE LOGIC APPLICATION

3.1 Introduction

As discussed in the previous chapter, integration of ferroelectric materials has gained tremendous attention recently due to its possible application towards devices with steeper subthreshold slope (SS) [42–44, 55, 63, 72]. As mentioned briefly in previous chapters, the ferroelectric voltage hysteresis is not favorable in logic devices. Therefore, it is important that transistors operate with hysteresis-free and steep slope properties. To reduce the subthreshold slope (SS) by utilizing the negative capacitance effect of ferroelectric materials, it is important to stabilize the overall capacitance network so that hysteresis is negligible and . Fig. 3.1 depicts simplified capacitance network in a MOSFET already mentioned in Fig. 1.8 (a).

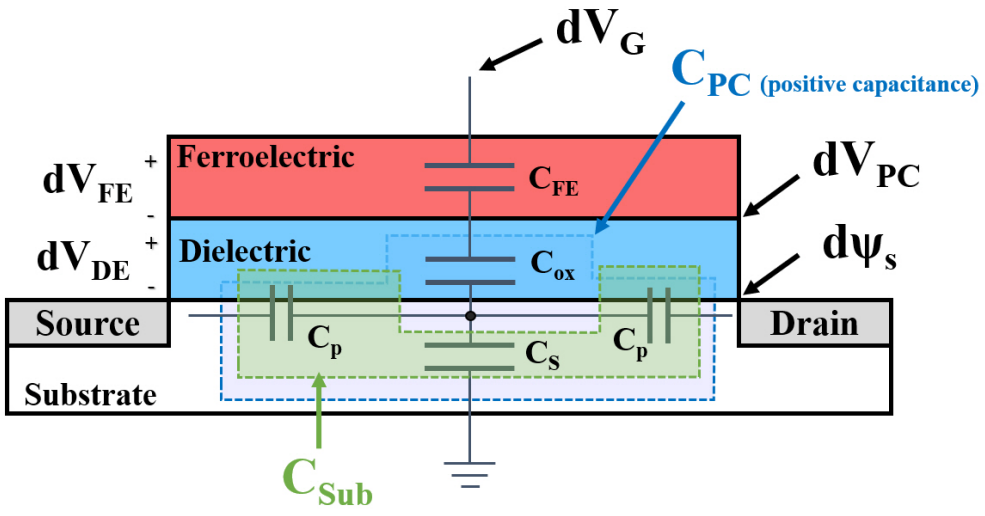

Fig. 3.1. Capacitance network in a NCFET.

C_{PC} is the series combination of positive capacitances (C_{ox} and C_{sub}) and C_{sub} includes substrate capacitance (C_S) and parasitic capacitance (C_p). From Fig. 4.1, eq. (4.1) (4.2) can be derived. C_S includes depletion capacitance and inversion (or accumulation) capacitances during the operation of the MOSFET, implying it is a variable capacitor. Assuming device operation under stabilized NC region, C_{FE} can be written as $-|C_{FE}|$.

$$\frac{dV_{PC}}{dV_G} = \frac{C_{FE}}{C_{FE}+C_{PC}} = \frac{|C_{FE}|}{|C_{FE}|-C_{PC}},\ where \frac{1}{C_{PC}} = \frac{1}{C_{sub}} + \frac{1}{C_{ox}} \tag{3.1}$$

$$\frac{d\psi_s}{dV_{PC}} = \frac{C_{ox}}{C_{ox}+C_{sub}} \tag{3.2}$$

$$\begin{aligned} SS = n \times m &= \left(\frac{d\log_{10} I_D}{d\psi_s}\right)^{-1} \times \left(\frac{d\psi_s}{dV_G}\right)^{-1} = 60\left(\frac{d\psi_s}{dV_{PC}} \times \frac{dV_{PC}}{dV_G}\right)^{-1} \\ &= 60\left(\frac{C_{ox}+C_{sub}}{C_{ox}}\right)\left(\frac{|C_{FE}| - \frac{C_{sub}C_{ox}}{C_{sub}+C_{ox}}}{|C_{FE}|}\right) = 60\left(1 + \frac{C_{sub}}{C_{ox}} - \frac{C_{sub}}{|C_{FE}|}\right) \end{aligned} \tag{3.3}$$

$$\frac{1}{C_{TOTAL}} = \frac{1}{C_{FE}} + \frac{1}{C_{PC}} = \frac{|C_{FE}| - C_{PC}}{|C_{FE}|C_{PC}} \tag{3.4}$$

From the definition of SS as presented earlier in (1.3), SS in a gate stack with both negative capacitance and conventional positive capacitances can be modified as (3.3). Total capacitance of the gate stack C_{TOTAL} should be positive. From (3.4), for hysteresis-free operation, $|C_{FE}| > C_{PC}$ is needed. From SS point-of-view, (3.3) shows that for SS < 60 mV/dec, $|C_{FE}| < C_{ox}$ is needed. It implies that if ferroelectric oxide becomes too thick (C_{FE} becoming smaller), hysteresis would be observed but on the other hand, if thinned down too excessively (C_{FE} becoming larger), SS would not be reduced. More complicated issue in capacitance matching is related with the variable capacitances present within the MOSFET such as C_S which is dependent on the channel charge. Other parasitic capacitances such as source/drain to VPC node were not included in Fig. 3.1. It can be roughly expected that by thinning down the ferroelectric HZO layer from the previous chapter with large ferroelectric hysteresis

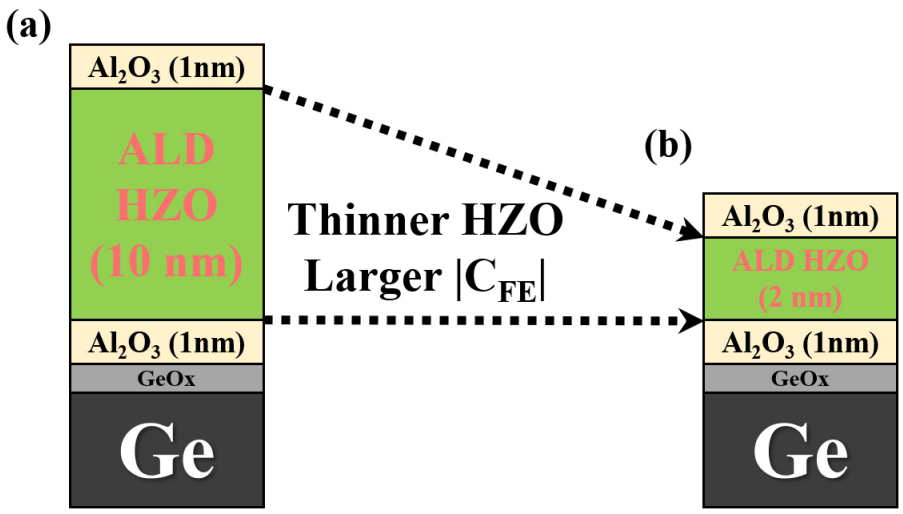

Fig. 3.2. (a) Germanium FeFET with large voltage hysteresis fabricated in the previous section. (b) HZO can be thinned down to obtain the stabilized condition for hysteresis-free and sub-60mV/dec operation by accessing the benefits of NCFET.

could result in hysteresis-free, stabilized negative capacitance FETs in germanium 3D structure platform. In this chapter, demonstration of germanium NC FinFETs both in NMOS and PMOS will be discussed.

3.2 Germanium NCFET

The fabrication step is the same as elaborated in Table 2.2 except the HZO's thickness was thinned down to 2 nm. In addition to p-type ion implantation shown in Table 2.2, n-type P ion implantation was done with dose of 5×10^{15} cm^{-2} at 15 keV. Both nFinFET and pFinFET are operating as accumulation mode (AM) transistors. Fabricated device structures are presented in Fig. 3.2 (b) which has thinner HZO (2 nm) than the ferroelectric FET fabricated in the previous section (Fig. 3.2 (a)).

As discussed in (3.1)-(3.4), thinning down the ferroelectric oxide layer weakens the effect of C_{FE} within the gate stack by increasing the C_{FE}. It was expected to reduce the voltage hysteresis in the current curves but at the same time at the cost

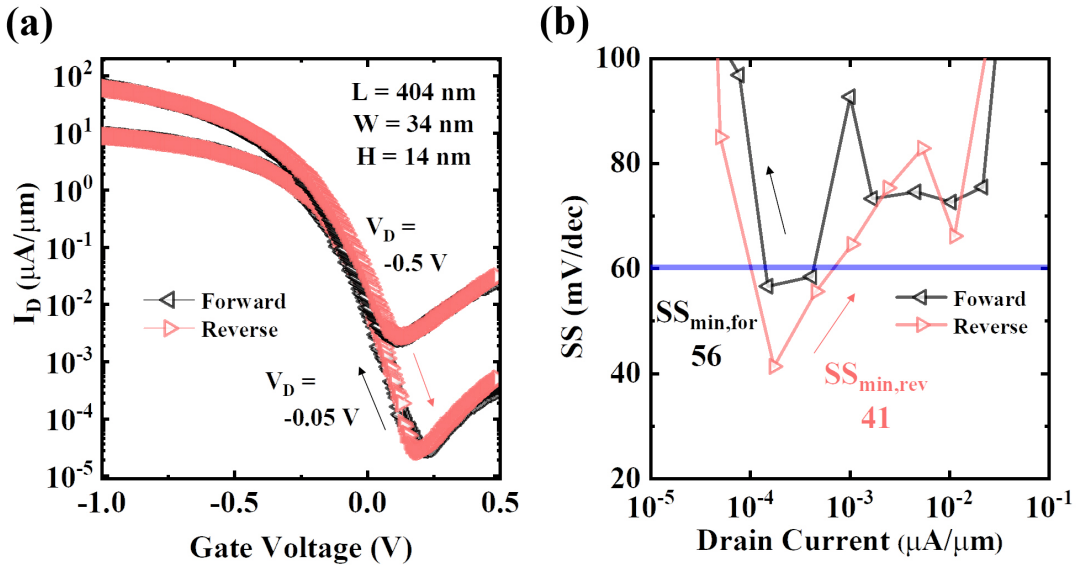

Fig. 3.3. (a) Transfer curve of a germanium NC pFinFET. Forward and reverse sweep are both shown at two different V_D values. (b) Extracted SS as a function of drain current.

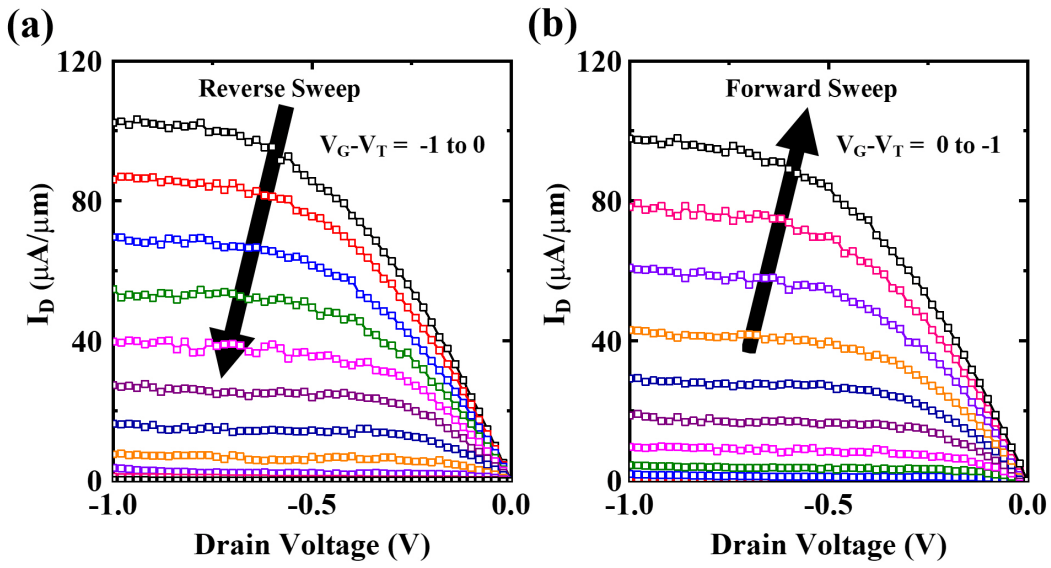

Fig. 3.4. Output curves (I_D-V_D) swept in the (a) reverse and (b) forward direction. V_G-V_T was swept from -1 to 0 V for the reverse sweep and 0 to -1 for the forward sweep.

of larger SS. Fig. 3.3 (a) shows the transfer curve of a germanium NC pFinFET. Hysteresis (defined as $\Delta V_T = V_{T,for} - V_{T,rev}$ in PMOS) was found to be negligible (approximately $\Delta V_T = 17$ mV). V_T was extracted using constant current method at 100 nA/μm. SS below 60 mV/dec was observed both from forward and reverse sweep directions. Fig. 3.3 (b) depicts the SS as a function of drain current. Minimum SS in the forward and reverse direction sweep were extracted to be 56 and 41 mV/dec, respectively. SS was extracted not from point-wise differentiation of the transfer curve since point-SS method intrinsically suffers from large noise. To prevent large spikes from point-SS method, transfer curves were measured every 5 mV or 10 mV steps so that large number of data points could be acquired. Then, every 3 data points were grouped and linear-fitted so that spikes can be effectively suppressed. Due to conservative nature of the SS-extraction method, actual SS could be lower than the displayed figures.

Output characteristic curves (I_D-V_D) were extracted in reverse and forward sweep directions as presented in Fig. 3.4 (a) and (b) respectively. Since there is no voltage hysteresis in this NCFET, currents exhibit similar levels when swept in both sweep directions unlike the asymmetric turn-on voltages in Fig. 2.15 (a) and (b).

Germanium NC nFinFETs were fabricated together with the pFinFETs. Negligible hysteresis (defined as $\Delta V_T = V_{T,rev}$ $V_{T,for}$ in NMOS) of approximately -4 mV was observed the transfer curves shown in Fig. 3.5 (a). The minimum SS calculated from the transfer curves in both directions are 43 and 49 mV/dec for forward and reverse sweep directions, respectively. SS with respect to the drain current is presented in Fig. 3.5 (b).

From the extracted SS curves as a function of drain current in Fig. 3.4 (b) and Fig. 3.5 (b), the Sub-60mV/dec regions are only visible from narrow ranges of drain currents. This could be due to variation in C_{PC} while channel charges were modulated along with V_G. As seen in Fig. 3.6, accessing the negative capacitance regime ($C_{FE} < 0$) and stabilizing it so that the device can benefit from NC is dependent not only on the operating voltage (V_G) but also on C_{PC}. Capacitance is defined as C≡dQ/dV.

Table 3.1.
Benchmark of device parameters extracted from various reported experimental NCFETs at room temperature. Hysteresis is defined as $\Delta V_{T,NMOS} = V_{T,rev} - V_{T,for}$ and $\Delta V_{T,PMOS} = V_{T,for} - V_{T,rev}$.

	This Work		**[45]**		**[44]**		**[72]**
Material	GeOI		Ge Bulk	GeSn	GeSOI		Si
Gate Stack (nm)	Al_2O_3/HZO(2)/Al_2O_3/GeO_x		HZO(6.5)/TaN/HfO_2		HZO(7)/GeO_x		HZO(1.5)/SiO_2
Structure	pFinFET	nFinFET	Planar pFET	Planar pFET	pFinFET	nFinFET	Planar nFET
W/L (nm)	34/404	41/302	L = 2,000	L = 3,000	20/100	20/60	136,000/20,000
Minimum SS (mV/dec)	56 (for) 41 (rev)	43 (for) 49 (rev)	100 (for) 56 (rev)	100 (for) 100 (rev)	86 (1 way) at 300 K	75 (1 way) at 300 K	52 (for) 52 (rev)
Hysteresis (mV)	-4	17	-40	-60	N/A	N/A	-0.8

The intercept between the load line of C_{PC} and the C_{FE} is the operating point for the NCFET. Fig. 3.6 (a) shows the modulation in Q with respect to V_G. If V_G is raised beyond certain condition which causes Q to exit the NC regime, C_{FE} becomes positive. Similarly, Fig. 3.6 (b) explains the effect of C_{PC} which is represented by the slope of the load lines. Even at the same V_G, inappropriate value of C_{PC} can remove the NC effect of ferroelectric material. Therefore, optimization of both operating voltage range and its respective Q-points are crucial for stable operation of NCFET. If devices can be precisely optimized to yield wide enough NC regime with Q-point in it throughout the whole operating voltage of the MOSFET, it will be able to fully benefit from the NC effect. For the optimization, numerous aspects should be considered such as design of parasitic (fringing) capacitance (Cp, C_{fr}), remnant polarization (P_r), coercive voltage (E_C), thickness of FE oxides, positive oxide (C_{ox}),

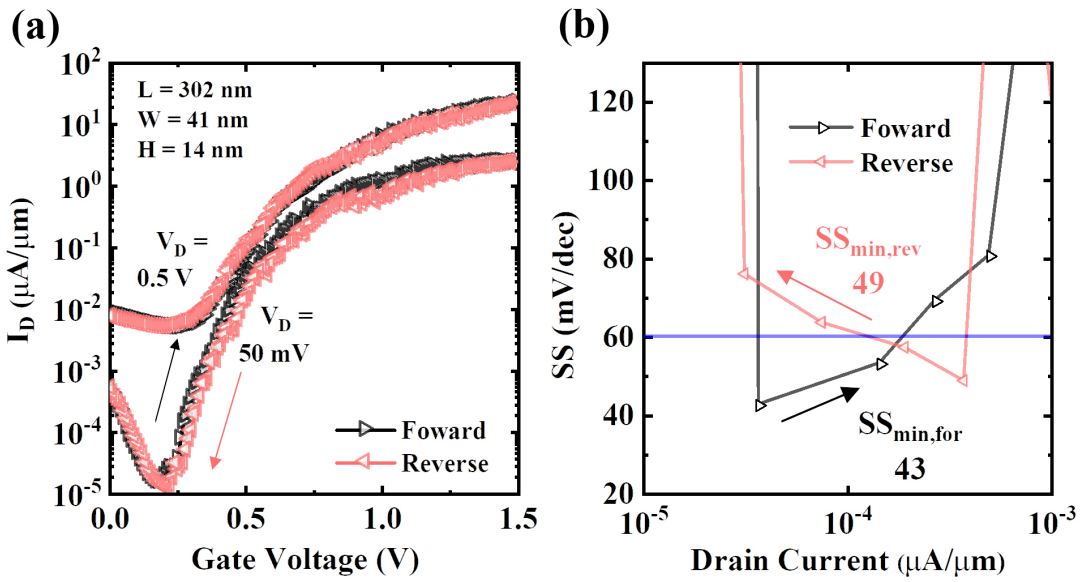

Fig. 3.5. (a) Hysteresis-free transfer curve of a germanium NC nFinFET swept in both forward and reverse direction at two different drain voltages. (b) Extracted SS as a function of drain current.

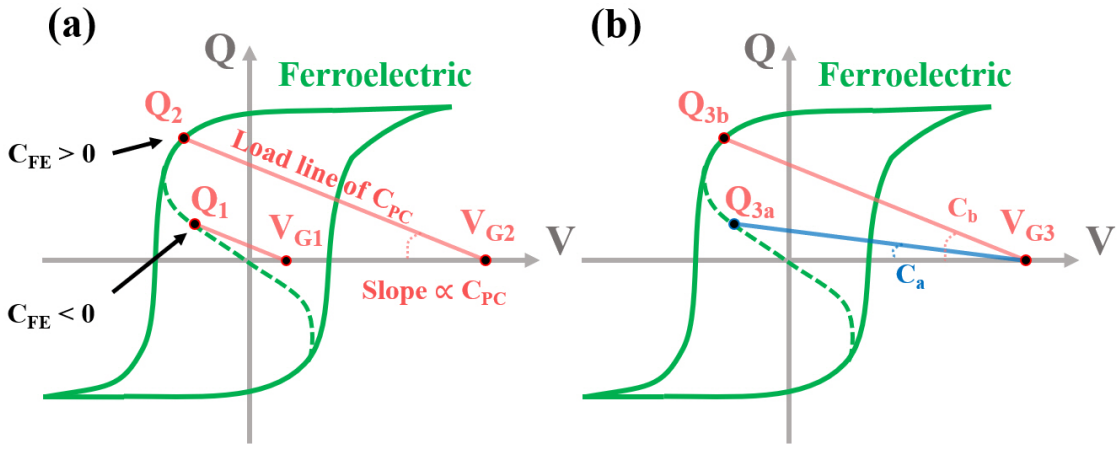

Fig. 3.6. Stabilization of NC within the gate stack can be realized with a series-connected positive capacitance (C_{PC}) represented as load lines. (a) Larger V_G ($V_{G2} > V_{G1}$) will push the Q-point out of $C_{FE} < 0$ region. (b) Larger C_{PC} will also push the Q-point out of NC regime.

annealing condition (temperature or time) of FE oxides, compositional ratio of Hf and Zr within HZO and so on.

Table 3.1 is the benchmark of reported NCFETs based on germanium, GeSn and Si channel. Gate stacks and device structures used for the integration of ferroelectricity including the thickness of the ferroelectric oxide are stated. Device dimensions (Width/Length), minimum extracted SS at room temperature are summarized. Voltage hysteresis values extracted from reverse and forward sweep direction are included.

3.3 Short channel effect in Ge NCFETs

Both germanium NC nFinFETs and pFinFETs were studied statistically to compare the effect of NC upon typical parameters studied in short channel devices, such as DIBL, V_T roll-off and SS. DIBL and SS are well-known to increase with channel length scaling with weakening gate oxide controllability over channel. V_T roll-off is also a typically observed phenomenon related with DIBL. However in NCFETs, it

is reported to be more robust towards these unwanted effects accompanied by the channel length scaling due to its nature of NC [52, 54, 55, 95]. As shown in Fig. 3.7 (a) and (b), increasing V_D with fixed V_G reduces the internal voltage at the node (V_{int}) between the C_{ox} and C_{FE} because the charge decrease translates to V_{FE} increase (since $C_{FE} < 0$). Increased VFE reduces the voltage on C_{ox} and consequently channel charge decreases [51]. When the device scales down, it was found that due to increasing dominance of fringing capacitance (C_{fr}) within the capacitance network

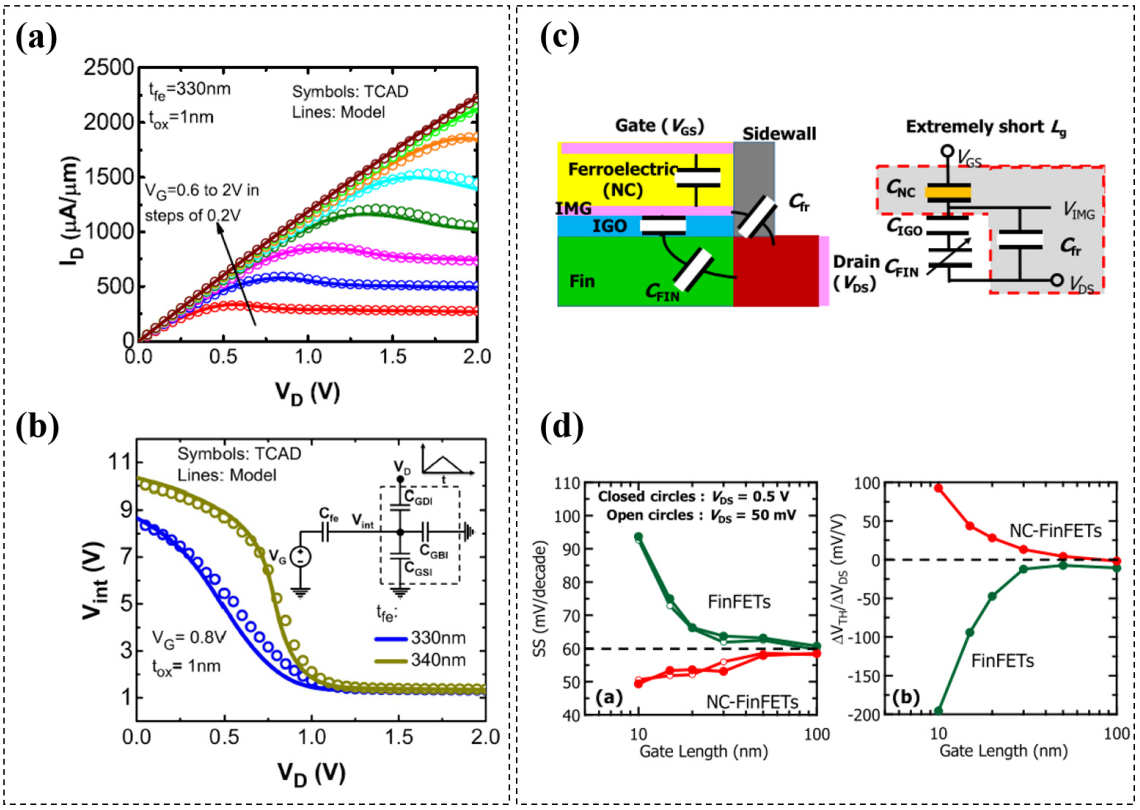

Fig. 3.7. Reported studies discussing the negative DIBL stemming from the nature of NC in ferroelectric oxide. (a) and (b) show negative DIBL due to increase voltage drop across ferroelectric oxide [51]. (c) and (d) show the effect of fringing capacitance with channel length scaling in a NCFET. Shorter channel length increases the dominance of C_{fr} within the gate stack and the drain's coupling through C_{fr} to the NC increases [52].

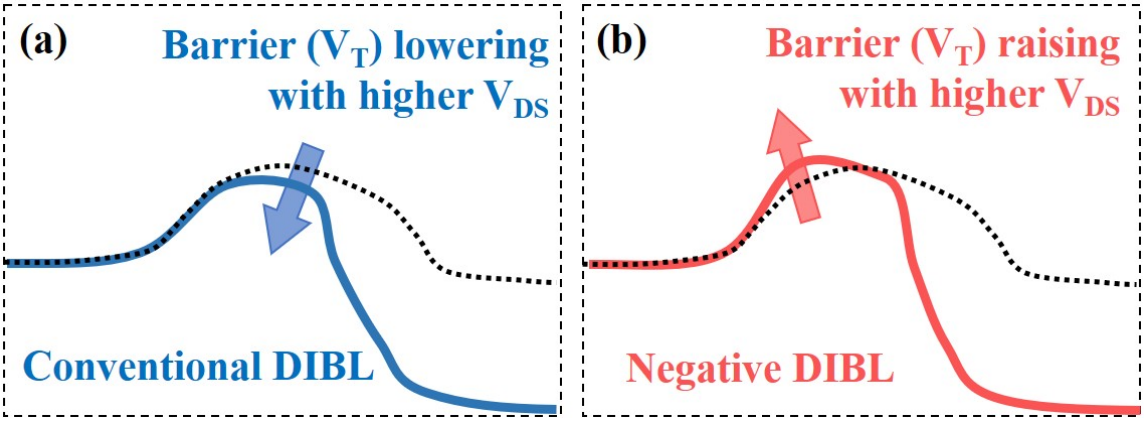

Fig. 3.8. Potential distribution from source via channel to drain in a (a) conventional FET and (b) NCFET. In NCFET, with an increase in V_D, negative (reverse) DIBL can be observed [42], [51].

(Fig. 3.7 (c)) results in stronger drain to VIMG coupling. This results in opposite trends in SS and V_T roll-off as presented in Fig. 3.7 (d) [52]. Fig. 3.8 (a) and (b) compare the DIBL in a conventional MOSFET and a NCFET, respectively. Due to drain to channel (and to NC oxide) coupling, increase in drain voltage can increase the barrier in the source-end of the channel, increasing the V_T instead of lowering it (DIBL, V_T roll-off) [51, 52].

Germanium FinFET devices (both nFinFET and pFinFET) fabricated and reported using the same process steps (recessed source and drain, recessed channel using SF_6-based dry etching, ALD-deposited Al_2O_3, formation of GeO_x using post oxidation process and same metal layers) and equipment were taken as reference devices [15].

As seen in Fig. 3.9 (a) and (b), fabricated NCFETs have thicker gate oxides than the reference group with only 1 nm of Al_2O_3 and same thickness of ultrathin GeO_x layer underneath it. With additional 2 nm of HZO and 1 nm of Al_2O_3 capping layer, devices in Fig. 3.9 (a) should show worse gate controllability and suffer from more severe short channel effects than Fig. 3.9 (b). To statistically study the NCFET's, 3

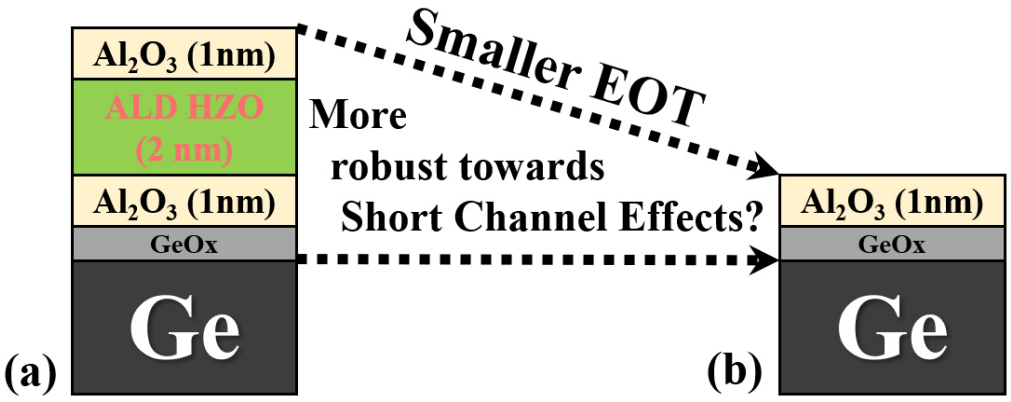

Fig. 3.9. Gate stacks of (a) germanium NC FinFETs and (b) reported germanium FinFETs using the same fabrication process and equipment [15].

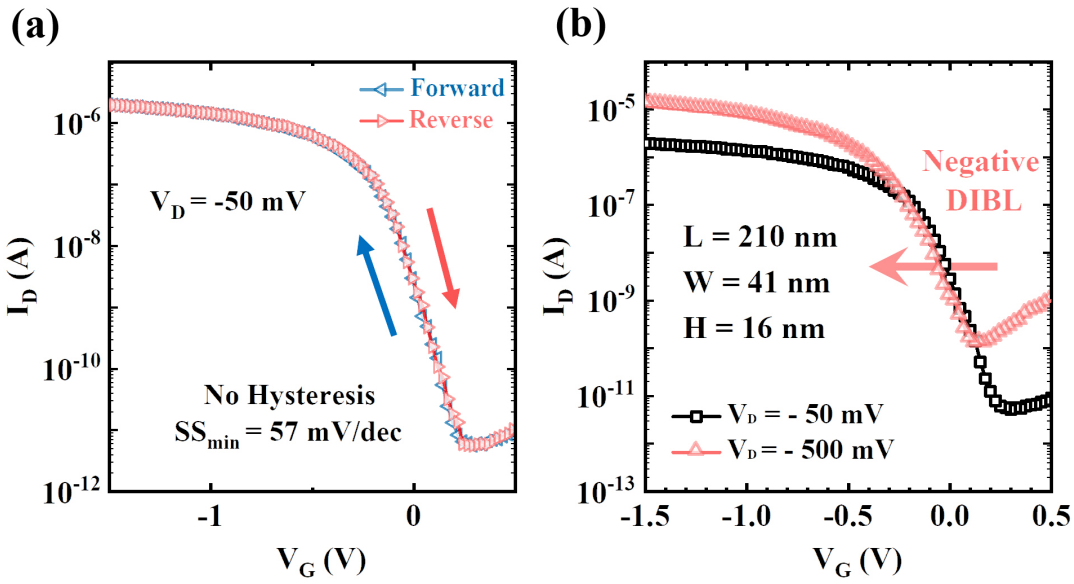

Fig. 3.10. (a) Transfer curves showing negligible hysteresis and sub-60mV/dec SS measured from one of the germanium NC pFinFETs. (b) Negative DIBL can also be seen where higher drain voltage increased the V_T instead of reducing it as in typical DIBL.

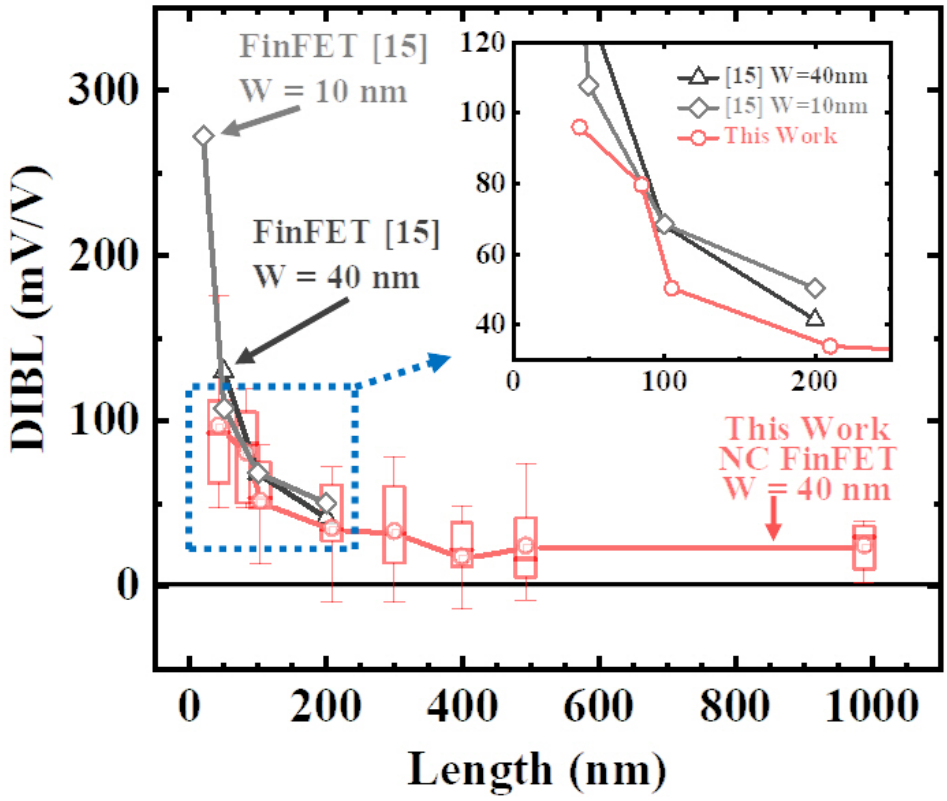

Fig. 3.11. DIBL as a function of channel length for both NCFETs and reference devices [15] show increasing DIBL with length scaling. However, inset graph which enlarges the blue-boxed region shows that NCFETs have smaller DIBL than reference devices.

parameters (SS, V_T and DIBL) were extracted and averaged over approximately 10 $\sim$ 20 devices per dimension.

From the measured transfer curves (I_D-V_G) swept in forward and reverse directions, hysteresis-free operation of germanium NC FinFET was once again confirmed as in Fig. 3.10 (a). Minimum SS of 57 mV/dec could be extracted from the curve. In addition, negative DIBL was also observed where $|V_T|$ measured with larger $|V_D|$ was than the $|V_T|$ from smaller $|V_D|$. DIBL was extracted from NCFETs and the ref-

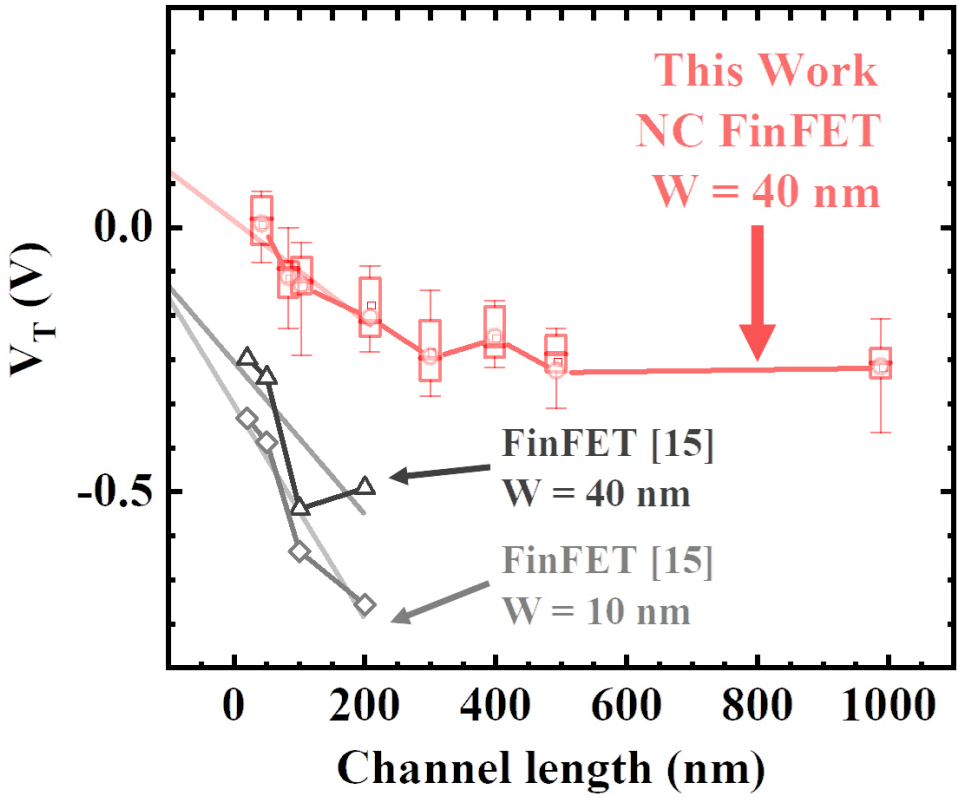

Fig. 3.12. Extracted V_T monitored with scaling channel lengths of NC FinFETs and reported conventional FinFETs [15]. V_T roll-off is less severe as seen from linear-fitted lines under L = 200 nm regime.

erence devices (Fig. 3.11). Inset graph of Fig. 3.11 shows the enlarged portion of the graph marked with blue-dotted box. Although both devices (NC and conventional FinFET) show increasing DIBL as the channel length scales down, NCFETs always show smaller DIBL than reported germanium FinFETs [15]. Moreover, DIBL < 0 could be observed within the statistical range of NCFETs' DIBL. The box represents $25 \sim 75$ percentile range and whiskers extends to $10 \sim 90$ percentile range. Mean and median values are denoted as a round symbol a bar within the box, respectively.

Fig. 3.12 is the V_T roll-off trend extracted from both device types. In V_T's case, when fitted with linear lines below L = 200 nm, slope of the V_T in conventional FinFETs are found to be steeper than the NC FinFETs. This also can be co-related with negative (reverse) DIBL effect in NCFETs. Fig. 3.13 shows the extracted SS as a function of channel length. Significant reduction in SS could be seen in NC FinFETs when compared to our reported FinFETs. These robustness in short channel effects of germanium NC FinFETs could be due to more stabilized process steps since the fabrication of the reported works back in 2015. However as seen from

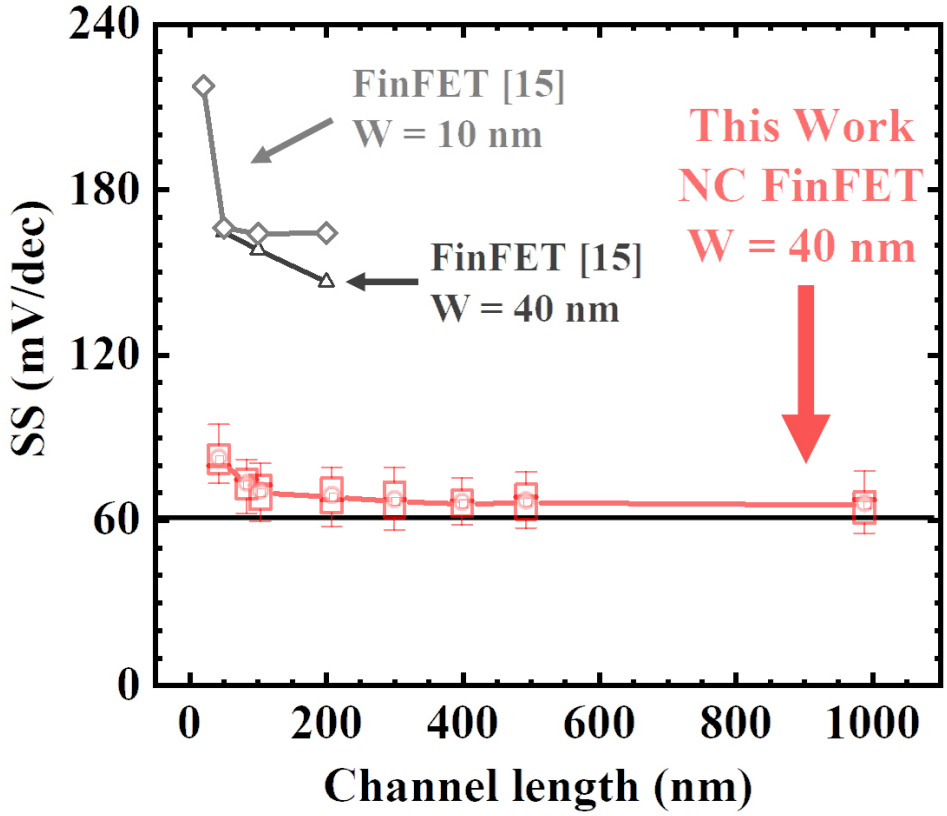

Fig. 3.13. SS as a function of channel length in NCFETs and reference devices [15]. SS was reduced significantly in NCFETs. SS levels that go sub-60 mV/dec limit in NC FinFETs can be visible.

Fig. 3.10, Fig. 3.11 and Fig. 3.13, although stabilization in fabrication process steps could alleviate the short channel effects but still cannot completely explain the negative values of DIBL and sub-60mV/dec SS. The acquired data did not coincide with dramatic results presented in Fig. 3.7 (d) but was found that integration of NC effects into conventional germanium FinFET platform slowed down the deterioration of short channel effects with scaling channel lengths. Similar results were reported in silicon platform recently as well [54, 95–97].

3.4 Digital etching technique for smaller devices

Fabricating smaller 3D devices can be challenging if the device dimensions approach the critical dimension of the lithography tools. Obviously, the smallest feature size that an electron-beam lithography tool can fabricate is much smaller than a typical photo-lithography tool. Using Vistec VB6 tool in Birck nanotechnology center

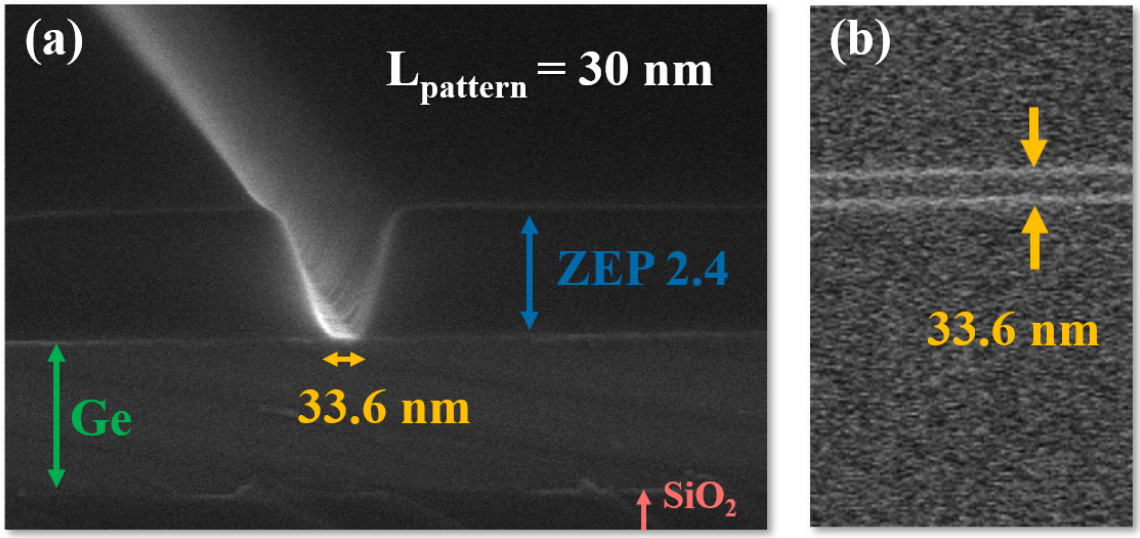

Fig. 3.14. (a) Minimum developed trench from direct e-beam lithography (VISTEC VB6) using ZEP 2.4 e-beam resist. (b) Top view of the trench.

(Purdue University, West Lafayette), the smallest e-beam pattern of approximately 30 nm on germanium-on-insulator wafer could be achieved as seen in Fig. 3.14. Further optimization may be possible to achieve even more extreme feature sizes but following condition was used for this study: ZEP 2.4 e-beam resist, 2500 RPM & 50 seconds spin coating, baking at 180 °C for 90 s, beam current = 0.5 nA, dose = 250 $\mu c/cm^2$). With this condition, the minimum feature size is limited to approximately 30 nm using similar fabrication recipes on GeOI wafers.

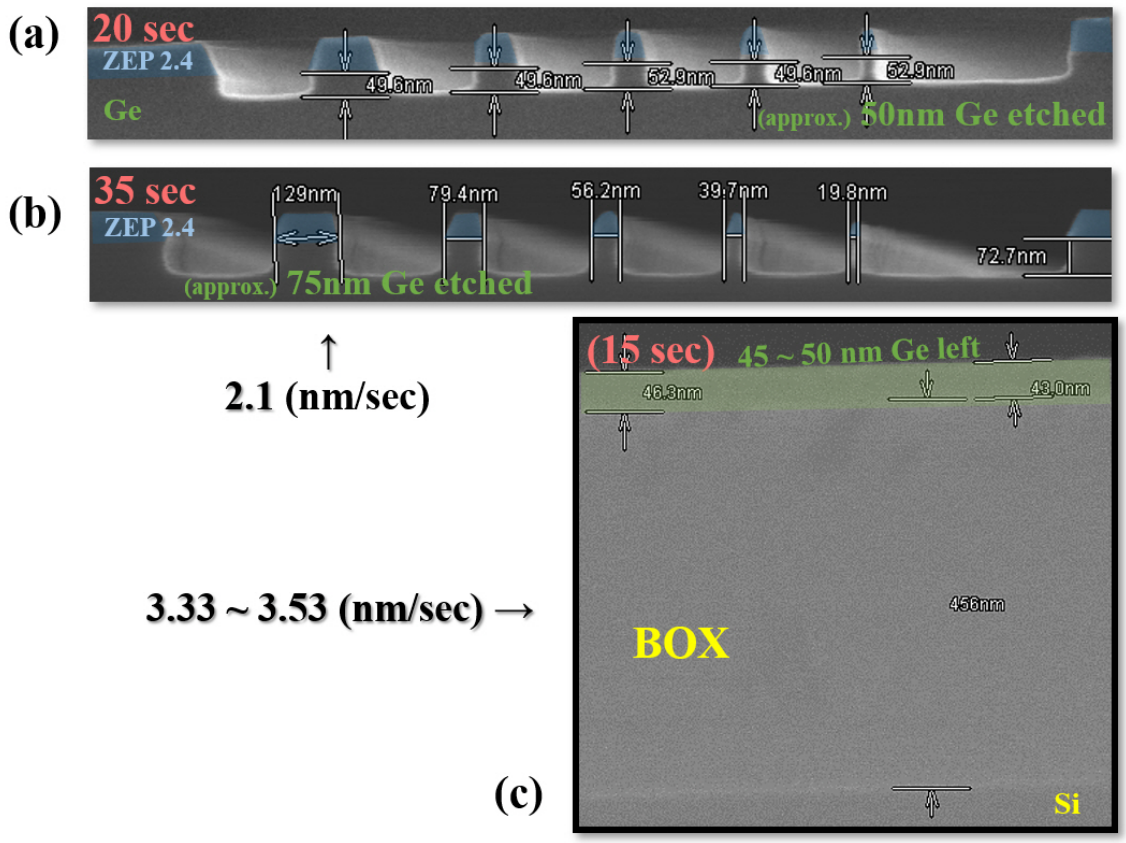

Fig. 3.15. Germanium dry etch profile with identical SF_6 recipe. Etch test on patterned trench window for (a) 20 seconds and (b) 35 seconds. (c) Etch test on GeOI wafer without forming etch window. Etch rate without etch window shows significantly higher rate.

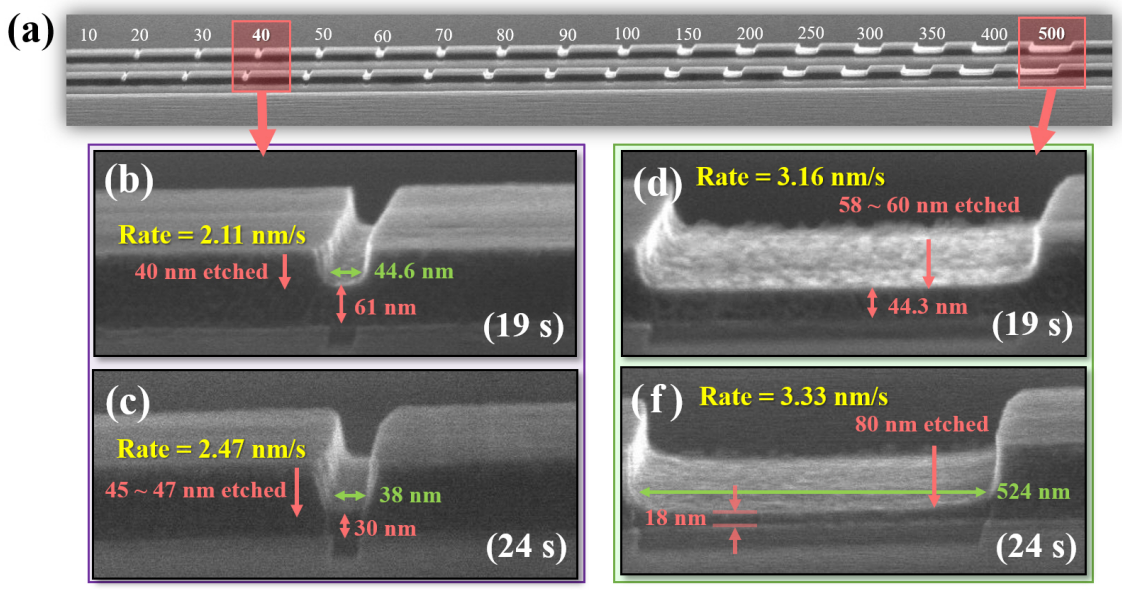

Fig. 3.16. (a) Etched Ge trench with different etch window ranging from 20 to 500 nm. (b) and (c) show etched profile of 40 nm long trench after 19 seconds and 24 seconds of etching, respectively. (d) and (f) are the etched profile of 500 nm long trench. Note that larger etch windows have higher etch rate.

To further push the feature size below this limit, digital etching can be implemented where cyclic oxidation of germanium surface and etching of the resulting GeO_x take place. If etch rate of $1 \sim 2$ nm/cycle can be achieved, device sizes can be shrunk gradually to achieve smaller dimensions beyond lithographic limit.

As frequently used on SOITEC GeOI wafer in our group [13,15,98,99], germanium dry etching using SF_6-based recipe was tested to accurately characterize the etching characteristics on newly acquired IQE GeOI wafers. Source RF power and bias RF power of 200 and 100 W was used with SF_6 flow rate of 40 cm^3/min was used at pressure of 0.3 Pa. As seen from Fig. 3.15, etch rate of bulk Ge without trench pattern (etch window) was significantly faster. It may be because for larger etching window, more SF_6 plasma can reach the Ge surface and etch the Ge. Etched byproducts can also be effectively transported away from the Ge surface accelerating the etch

process. Fig. 3.16 shows the relationship between the etch rate and the etch window. The results are summarized in Table 3.2. It can be confirmed again that with larger etch window, the etch rate becomes faster. To conclude, germanium etch rates are approximately 3.1 $\sim$ 3.3 nm/s if the gap is larger than 200 nm and 2.4 $\sim$ 2.8 nm/s if the gap is below 200 nm.

With the acquired etch results, digital etch recipe can be optimized. Germanium nanowire devices were fabricated as seen in Fig. 3.17 (a)-(e). Channel lengths were first defined (Fig. 3.17 (a), (b)) with SF_6 dry etch recipe optimized previously. Then fin widths were defined using the same dry etch recipe. Fin widths can be controlled

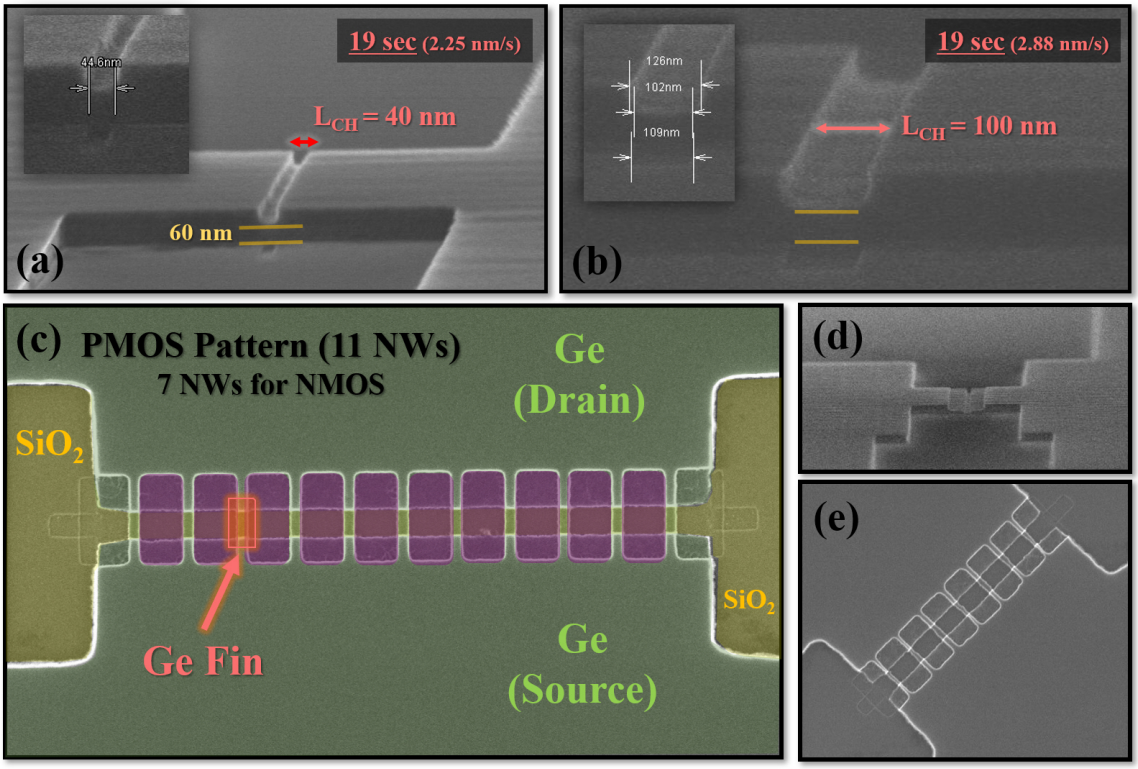

Fig. 3.17. SEM images after channel length of (a) 40 nm and (b) 100 nm were defined. Etch rate is consistent with values from Table 3.2. (c) Top-view of false-colored SEM image after the fin definition with the same SF_6 dry etching. (d) and (e) show views from different angles.

Table 3.2.
Etched Ge (nm) and etch rate (nm/s) as a function of etch window (nm).

Etch window (nm) →	**40**	**50**	**60**	**70**	**80**	**90**	**100**	**250**	**500**
Etch time, 19 s Etched Ge(nm)	45	46	51	51	51	51	54	59	60
Etch rate (nm/s)	2.37	2.42	2.68	2.68	2.68	2.68	2.84	3.11	3.16
Etch time, 24 s Etched Ge(nm)	70	71	77	75	72	74	72	78	82
Etch rate (nm/s)	2.92	2.96	3.21	3.13	3	3.08	3	3.25	3.42

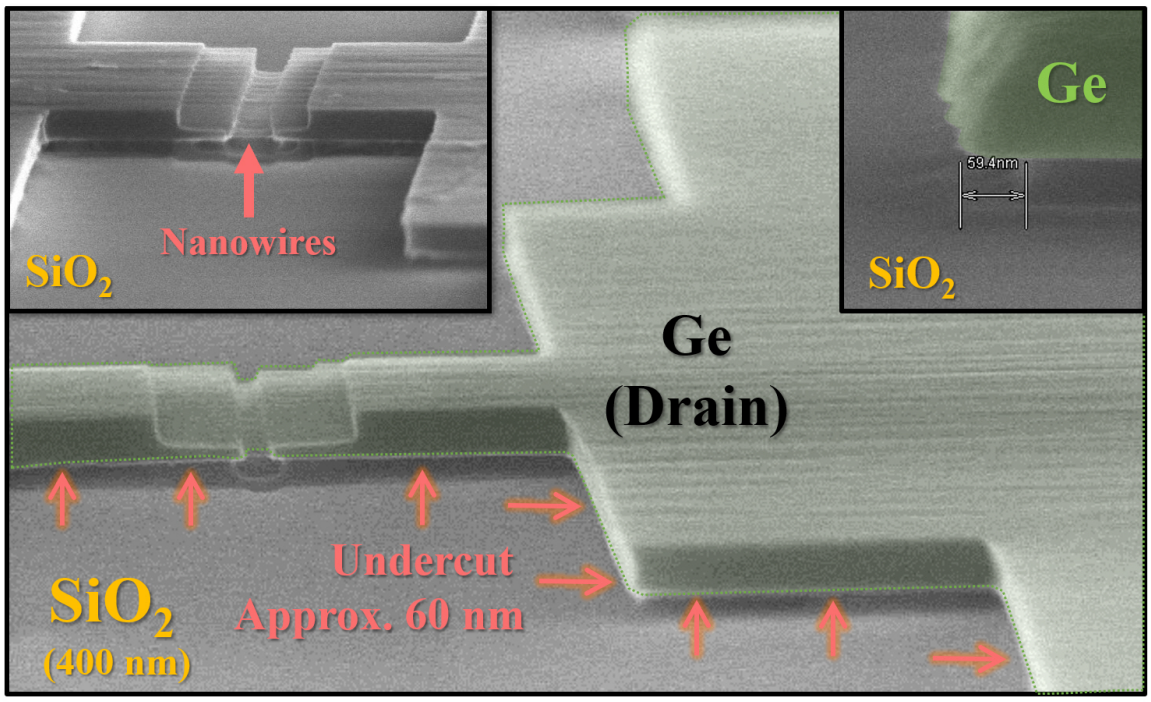

Fig. 3.18. False-colored SEM images after nanowire release with HF (4 %) cyclic etching. Undercut of approximately 60 nm is visible.

with e-beam lithography as seen in Fig. 3.17 (c). Then, nanowires were released with cyclic HF wet etching (4 %), etching away the SiO_2 underneath the Ge fins. Fig. 3.18 shows the SEM images that show approximately 60 nm undercut of SiO_2 formed after the nanowire release process.

After the nanowire structure was defined, two different oxidation equipment that are readily available in Birck nanotechnology center were used. The first equipment used for the digital etching is the Jipelec rapid thermal annealing machine (Fig. 3.19 (a)). Pyrometer is used to control the temperature above 500 °C and various process gasses (N_2, O_2, Ar and forming gas) are available. Within the chamber, the temperature of the sample was raised up to 500 °C within ramp time of 10 seconds. The pressure was kept at 1 atm. During the annealing time, O_2 gas was supplied for the oxidation. The sample was kept at 500 °C for 30 seconds until the temperature is brought back down to the room temperature. Immediately after each oxidation, oxidized germanium surface (GeO_x) was etched with H_2O (DI water) for 30 seconds since as mentioned in chapter 1, GeO_x is hygroscopic. 3 cyclic oxidation/etching

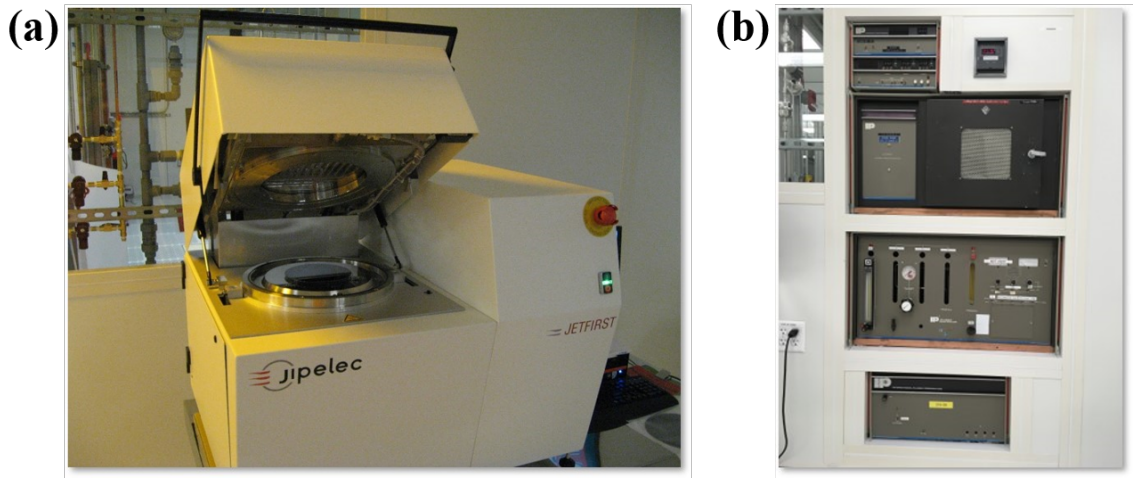

Fig. 3.19. (a) Jipelec rapid thermal annealing machine. (b) Branson plasma etching system (Ar/O_2).

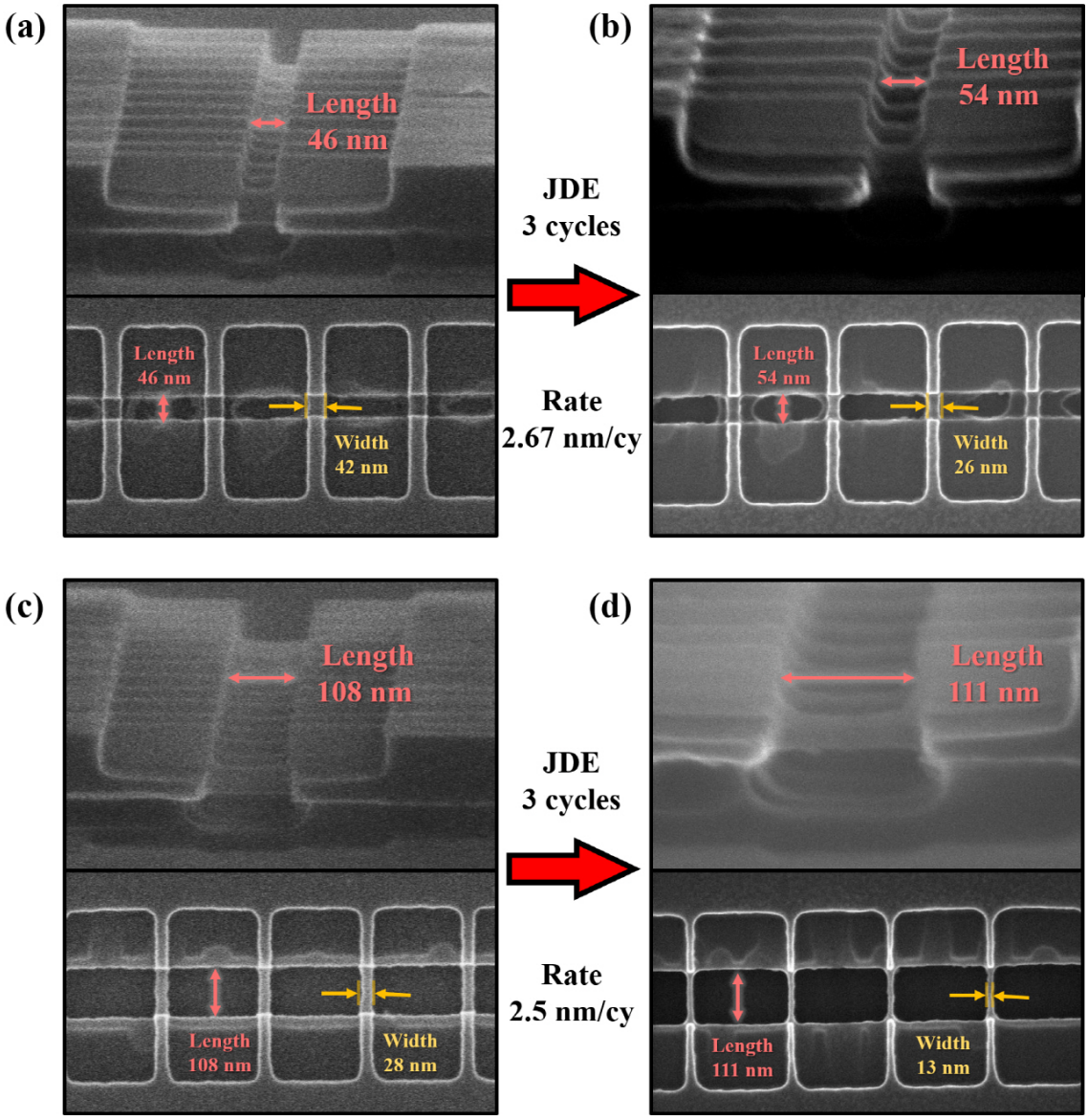

Fig. 3.20. SEM images of germanium nanowires (L = 46 nm, W = 42 nm) (a) before and (b) after 3 cycles of Jipelec digital etching (JDE). Another nanowire (L = 108 nm, W = 28 nm) is shown (c) before and (d) after the same JDE process.

were done with Jipelec (JDE , Jipelec digital etching) and the nanowire profiles were observed with SEM.

Resulting nanowire dimension change can be seen in Fig. 3.20 (a)-(d). Although various channel lengths and widths were all treated with JDE simultaneously, only 2 different channel lengths and widths are presented here. The etch rate of JDE was found to be in the range of 2.5 $\sim$ 3.0 nm/cycle. However, the etch rate is too fast to control the device dimensions within 1 nm precision.

The second equipment that can oxidize the surface of germanium nanowires is Branson plasma etcher (Fig. 3.19 (b)). This plasma system provides process gasses such as Ar and O_2. RF generator is used to generate the plasma. Both O_2 and Ar was supplied for the Branson digital etching (BDE) process and the pressure was supplied with 12:125 ratio. Pressure within the chamber was maintained at 1.05 torr during the 60 seconds of oxidation. Subsequent GeO_x was etched with the same process as JDE using DI water for 30 seconds. Fig. 3.21 (a)-(b) show the results from BDE. It

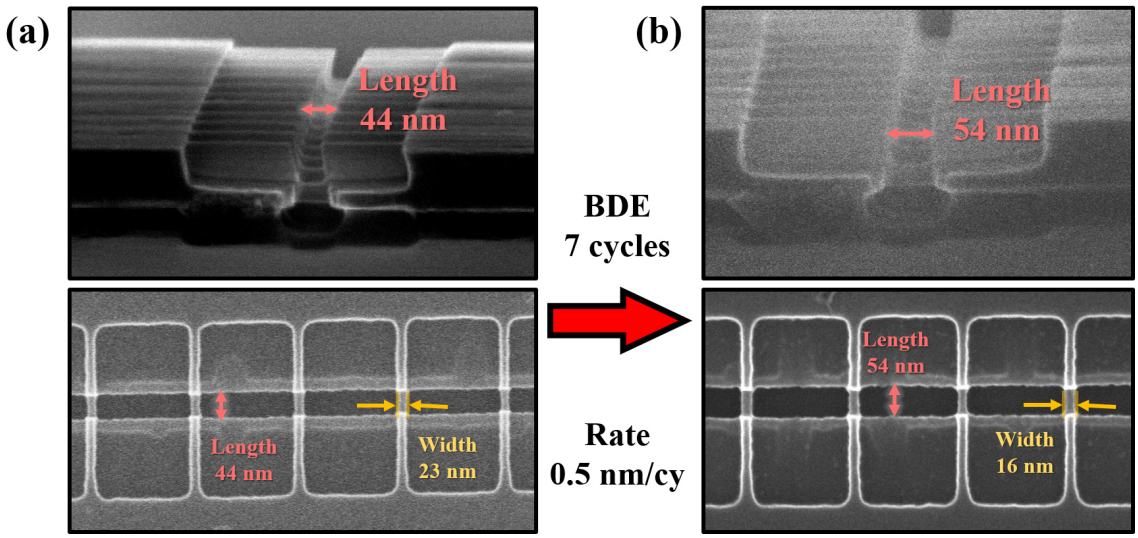

Fig. 3.21. SEM images of germanium nanowires (L = 44 nm, W = 23 nm) (a) before and (b) after 3 cycles of Branson digital etching (BDE). The etch rate for BDE is more precise than JDE in Fig. 3.20.

was found to have much slower etch rate of approximately 0.5 $\sim$ 1 nm/cycle. The range of the etch rate may stem from different aspect ratios or dimensions of the Ge nanowires. With BDE, nanowires with widths smaller than 9 nm were fabricated but they were too thin and long (height $>$ 35 nm, length $>$ 50 nm) to sustain its shape and got distorted easily. If the aspect ratios are designed to withstand such thin nanowire (note that there is an air gap below the nanowires), it would be feasible to fabricate extreme widths $<$ 10 nm using precisely controlled BDE.

4. GE FEFET TOWARDS NEUROMORPHIC COMPUTING

4.1 Introduction

Continued improvement in processor performances led to faster parallel computing capabilities. Such trend ignited the realization of brain-inspired computing and synaptic devices [101–107]. It is known that a human brain operates in a highly ef-

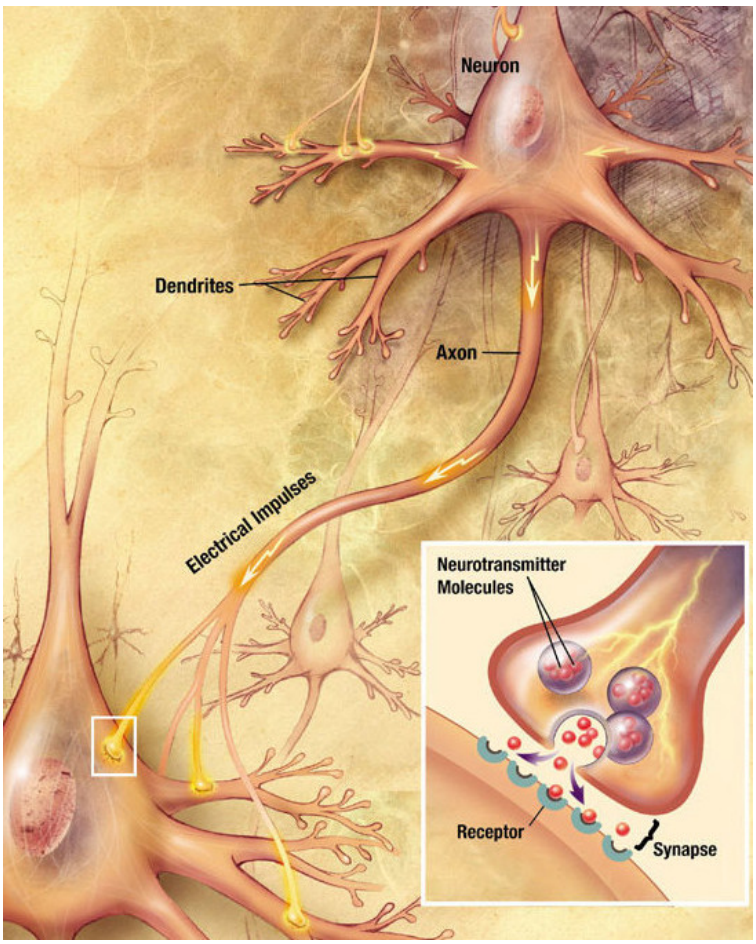

Fig. 4.1. An artistic interpretation of synapses and neurons in human brain [100].

ficient way even with approximately 10^{11} neurons and 10^{15} synapses when compared to conventional electronic circuitry [108].

As depicted in Fig. 4.1, a brain perceives biological sensory data in parallel and processes them instantaneously with very low power (∼10 W). In order to mimic human brain's operation, electronic neuromorphic circuits employ the parallel computing which executes multi-layers of multiplication and addition. Each layer's output is fed to the input of the following layer as shown in Fig. 4.2 which briefly shows the simplified schematic of a deep neural network (DNN) used in machine learning. In this schematic, input neurons receive 20 by 20 pixels (cropped) image data of hand-written numbers from Modified National Institute of Standards and Technology (MNIST) database which are then processed through 2 hidden layers. The weight data saved in synaptic devices are processed (multiplication and addition) and forward propagated towards the next layer through a specific non-linear function such as sigmoid, hyperbolic tangent or ReLU (rectified linear unit) function. Therefore simply put, a neuron can be considered as a simple computing element and a synapse

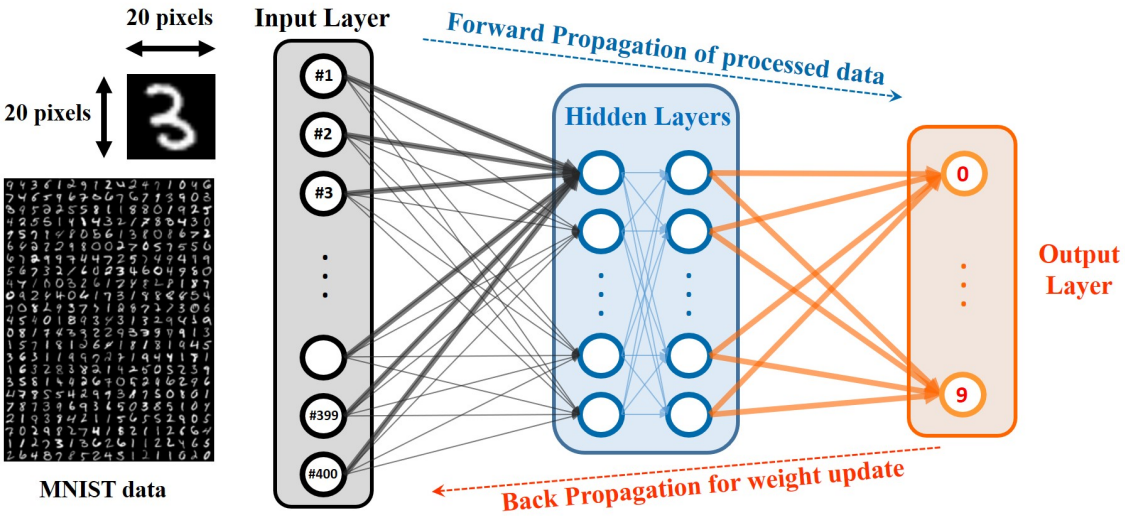

Fig. 4.2. A brief network schematic of a deep neural network (DNN) with 400 input neurons, 10 output neurons and 2 hidden layers.

can be viewed as a local weight storage memory [109, 110]. Output layer represents a single digit number from 0 to 9. If the output is incorrect, the network is re-trained through back propagation by adjusting the weight values throughout the whole network. This iterative correction of weight values accumulates over multiple epochs and the accuracy of the system gradually improves.

In conventional von-Neumann-based DNN, programmable weights are propagated through a complex and dense network where such weights are saved elsewhere (external memory devices). In this architecture, data processing and data saving happen at separate locations which require additional saving and accessing time. Also when static random access memory (SRAM) is used, the device density is restricted due to larger area of SRAM when compared to emerging devices [110]. If such bottleneck can be removed by using pairs of emerging non-volatile memory (e-NVM) and a selector configured into highly dense crossbar array structure, lower energy consumption, reduction in processing time and high density processing for neuromorphic circuits could be achievable.

There are several e-NVM that can be utilized as the synaptic device in DNN such as resistive [57, 58, 104, 111], phase change [56, 107, 112] and ferroelectric [59–61] memory. Among these candidates, ferroelectric FET (FeFET) is promising due to its partial polarization capabilities, low energy consumption and high compatibility with CMOS platform. Since the introduction of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO), it has been studied extensively not only in negative capacitance (NC) devices but also its application towards FE memory devices. Neuromorphic application of HZO is of interest and reported work [59, 61] shows its possibility as highly efficient synaptic device.

Aforementioned e-NVMs operate under different mechanisms but share common non-ideal characteristics when considered as candidates for synaptic device in neuromorphic computing which were elaborated in Chapter 1, section 1.4. These non-idealities shown in Fig. 1.11 are listed below.

- Randomness in conductance (G) values and device to device variation..

- Low G_{max}/G_{min} value.
- Non-linear and asymmetric conductance update (potentiation and depression).

Suffering from such non-ideal conductance update profiles, reported works on e-NVM neural networks try to alleviate the accuracy loss by introducing various pulse schemes [59, 61]. As depicted in Fig. 4.3, pulses with different bias or pulse width are possible. However, it is most preferable if all the pulses are identical

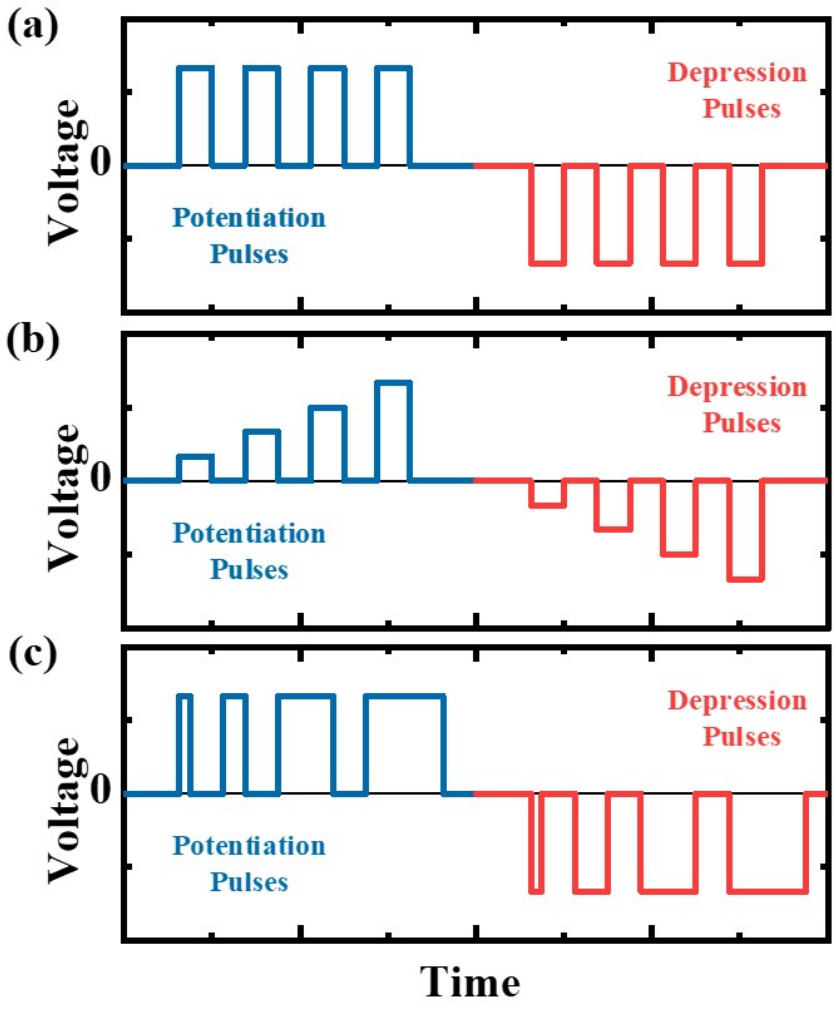

Fig. 4.3. Various possible update pulses for e-NVM synaptic devices. (a) Identical pulses, (b) Variable pulse levels and (c) variable pulse widths

during potentiation or depression. If the pulses are like Fig. 4.3 (b) or (c), an additional step (and thus time and energy) is needed to sense the current weight value to figure out the correct pulse to use as the update pulse at that specific status. This will compromise the proposed efficiency of using e-NVM-based non-von-Neumann architecture as neural network. Therefore it is important to optimize the pulsing schemes for improved linearity and symmetry.

Table 4.1.
Fabrication process of germanium ferroelectric nanowire FET in detail.

Step	**Remarks**
1. Wafer cleaning, solvent and acid	GeOI ($Ge/SiO_2/Si$)
2. Mesa isolation definition	Dry Etching (SF_6)
3. P-type ion implantation	BF_2, 4×10^{15} cm^{-2}, 15 keV
4. Channel recess for Fin height definition	Dry Etching (SF_6)
5. Fin patterning	Dry Etching (SF_6)
6. Nanowire release	HF cyclic wet etching
7. Gate oxide deposition (ALD)	
a) Al_2O_3	1 nm, 250 °C
b) Post Oxidation	RTA, O_2, 500 °C, 30 seconds
c) HZO deposition	10 nm, 250 °C
d) Al_2O_3 capping	1 nm, 250 °C
8. HZO crystallization (PDA)	RTA, N_2, 500 °C, 60 seconds
9. Source, drain recess	Dry Etching (BCl_3/Ar)
10. Ni contact deposition	Evaporation
11. Ohmic annealing	RTA, N_2, 250 °C, 30 seconds
12. Gate, source, drain pad deposition (Ni)	Evaporation

4.2 Ge NW FeFET synaptic device

Table 4.1 elaborates the fabrication process of Ge nanowire (NW) FeFET synaptic device studied in this chapter. Fabrication of NWFET is identical to the process flow of Ge FinFET device shown in Table 2.2 except the nanowire release procedure directly following the fin etching step. Etching the underlying SiO_2 selectively with HF releases the nanowire structure with air gap underneath it. As found in Fig. 4.4 (a) and 4.5 (a), multiple nanowires were formed in parallel by dry etching and the underlying SiO_2 was selectively etched to form the air gap under the nanowires.

After the physical nanowire structure was formed, gate oxides were deposited in 2 steps (Al_2O_3 followed by HZO) including the post oxidation step in RTA chamber immediately after the first Al_2O_3 deposition step. After the HZO deposition, post deposition annealing (PDA) was carried out to induce ferroelectricity in HZO as elaborated in step # 8 in Table 4.1.

Fig. 4.6 shows the strong ferroelectricity in the fabricated Ge NWFET. The memory window (voltage hysteresis) was measured to be approximately -5 V. The

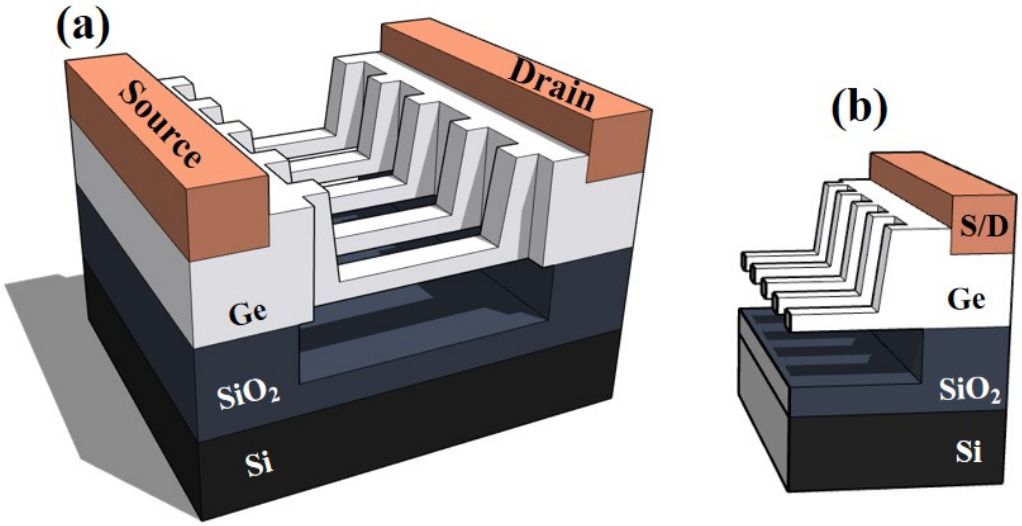

Fig. 4.4. (a) 3D structure of the Ge synaptic nanowire device. (b) Cross-sectional view of nanowires before step # 7 in Table 4.1

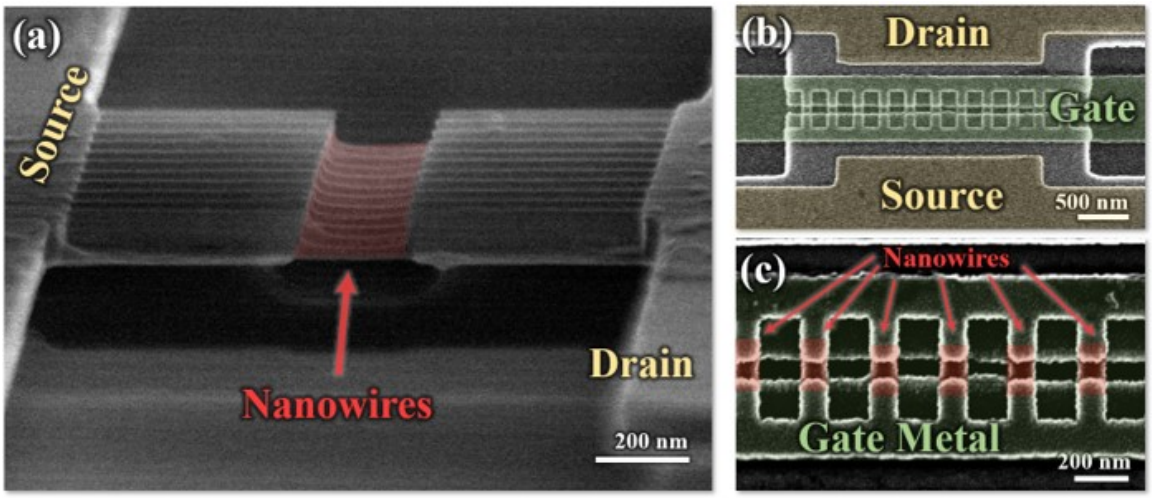

Fig. 4.5. False-colored SEM images of Ge NWFET viewed from (a) the side before step # 7 in Table 4.1. Top view SEM images after step # 12 in Table 4.1 is shown in (b) and (c). In the zoomed-in image of (c), multiple parallel nanowires can be seen.

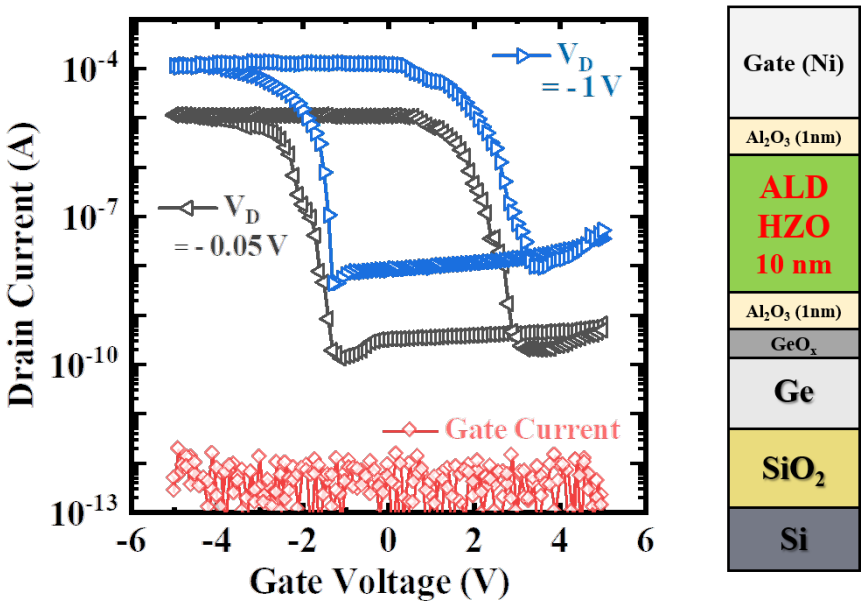

Fig. 4.6. Transfer curve (I_D-V_G) of the Ge NW pFET and its negligible gate leakage current. Cross-sectional gate oxide stack is shown on the right.

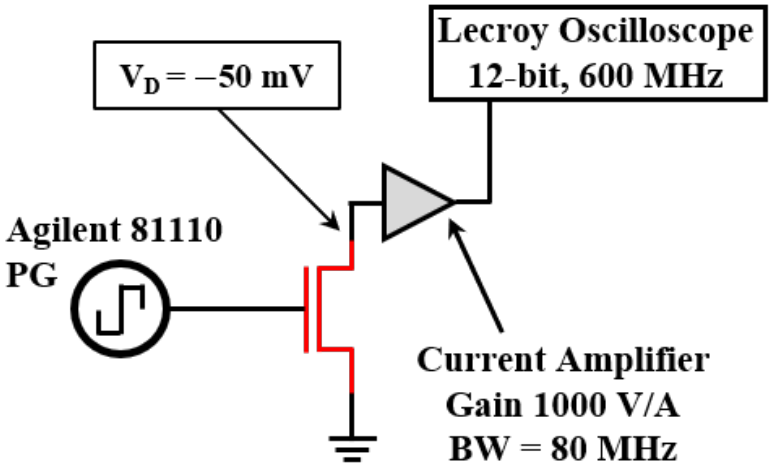

Fig. 4.7. Measurement set-up for real time conductance update probing.

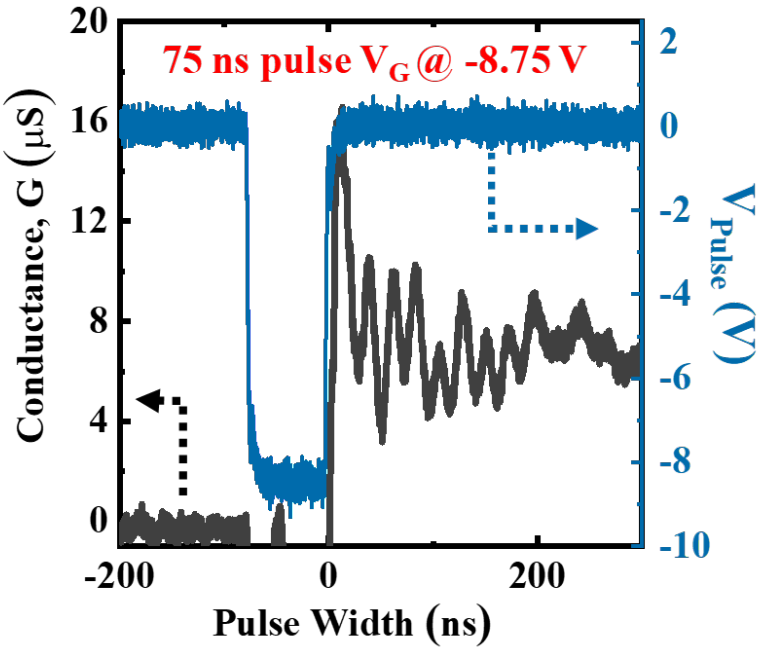

Fig. 4.8. Real-time potentiation with 75 ns negative pulse (V_G) using set-up shown in Fig. 4.7.

physical dimension of FeFET (L_{NW}= 105 nm, W_{NW}= 50 nm, H_{NW}= 26 nm) reveals FeFET's promising scalability. In addition, gate leakage current was observed to be negligible (Fig. 4.6) within the operation voltage range (± 5 V).

To observe the conductance programming into FeFET in real-time, measurement set-up shown in Fig. 4.7 was prepared in collaboration with laboratory stationed in National Institute of Standards and Technology (NIST). Current amplifier was connected to the drain of the FeFET under test in series with 600 MHz oscilloscope while keeping the drain voltage stable at -50 mV. With Agilent 81110 pulse generator supplying the negative V_G pulse of -8.75 V (pulse width 75 ns), drain current fluctuation was monitored in real-time as presented in Fig. 4.8. The drain current was then translated into channel conductance (G, μS).

After probing the real-time conductance potentiation, pulse optimization was done using the measurement set up depicted in Fig. 4.9. The whole process was similar to the procedure shown in Fig. 2.18 except that the applied negative V_G pulse level and its pulse width had to be optimized precisely in order to keep the linear and symmetric conductance profile during weight update process. First, the positive ini-

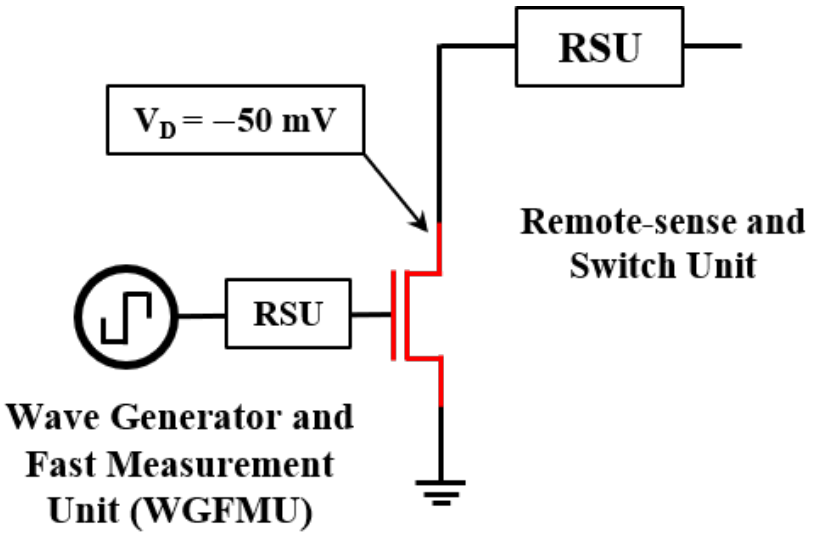

Fig. 4.9. Measurement set-up for optimization of consecutive potentiation and depression using fast measurement unit.

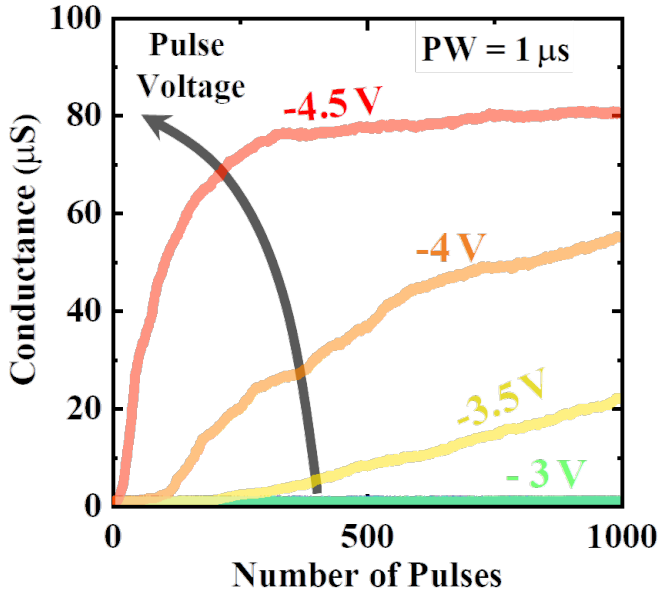

Fig. 4.10. Potentiation profile with varying pulse levels (V_G = -1 V to -4.5 V) at fixed pulse width (1 μs).

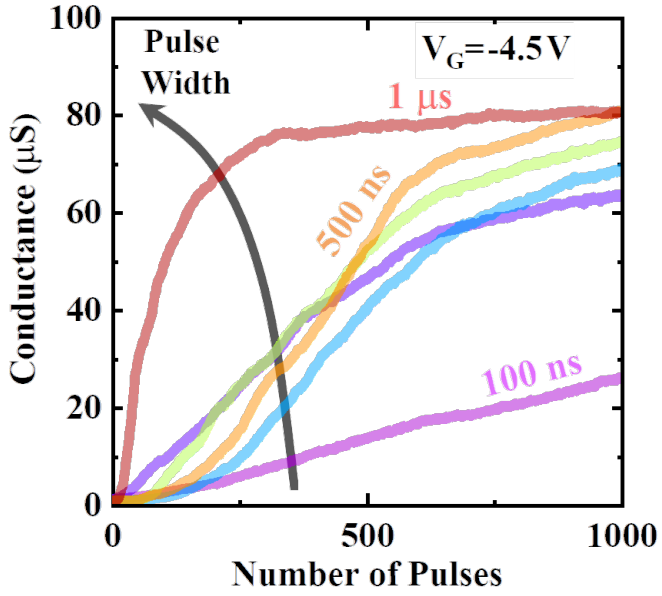

Fig. 4.11. Potentiation profile with fixed V_G= -4.5 V but varying pulse widths.

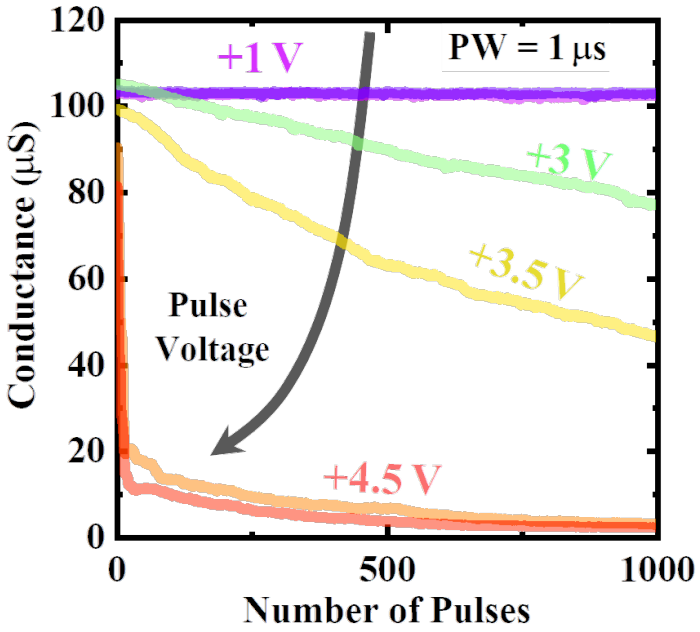

Fig. 4.12. Depression profiles with fixed pulse width of 1 μs.

tializing V_G pulse was applied to ensure device operation via forward polarization curve. Then optimized negative V_G pulses were given to the gate of FeFET in order to partially polarize the HZO which will then translate to partially adjusted channel conductance. Drain current (I_D) is measured with V_G = 0 V to minimize the disturbance to the programmed conductance level. Drain voltage (V_D) is always kept at -50 mV throughout the whole process.

Fig. 4.10 and Fig. 4.11 show the potentiation conductance profiles resulting from unoptimized potentiation pulses. In Fig. 4.10, a relatively long pulse width of 1 μs was used while varying the pulse level from -1 V to -4.5 V. As the trend suggests, increasing the potentiation voltage up to -4.5 V reduces the number of pulses needed to reach the G_{max} of approximately 80 μS. This indicates that with such a long pulse width, pulse level should be reduced to prevent abrupt potentiation and secure good number of conductance states. Similarly with fixed pulse level of V_G = -4.5 V, longer

pulse widths (increased from 100 ns up to 1 μs) reduce the number of pulses to reach the G_{max} (Fig. 4.11). This trend is exactly the same in depression cases depicted in Fig. 4.12. Therefore as Fig. 4.13 suggests, if the pulses for potentiation and depression are not optimized respectively, the conductance profile will turn out to be highly non-linear and asymmetrical. This will definitely degrade the online learning accuracy of the DNN. One more issue observed from inset graph of Fig. 4.13 is that the depression is much more sensitive in this pulsing scheme than the potentiation case. The conductance dramatically decreases down to approximately 1/8 of G_{max} value after the initial 20 depression pulses. Therefore the depression pulses should be optimized appropriately relative to the potentiation counterpart.

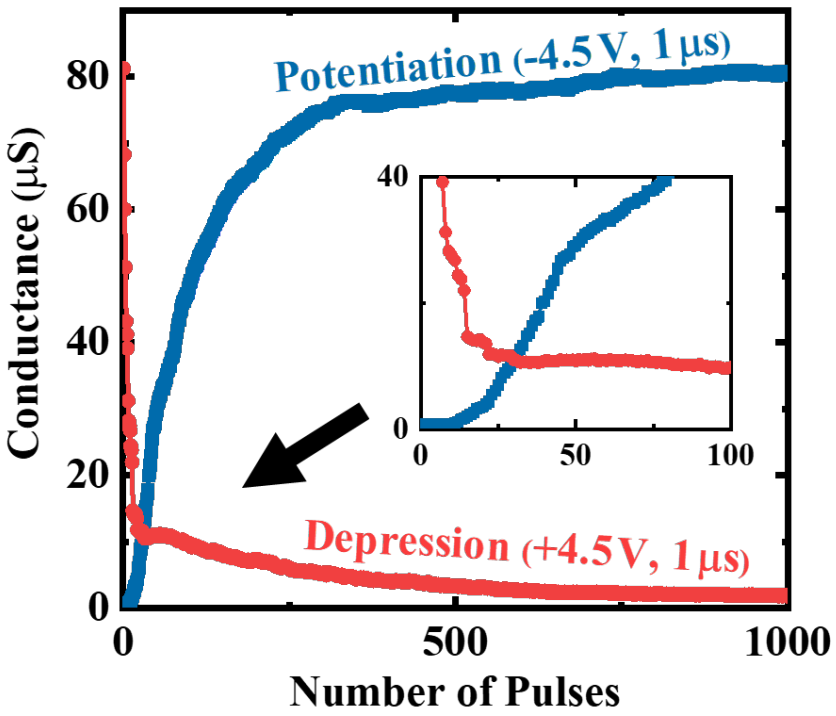

Fig. 4.13. Highly non-linear and asymmetric weight update profile due to unoptimized pulsing schemes for both potentiation and depression.

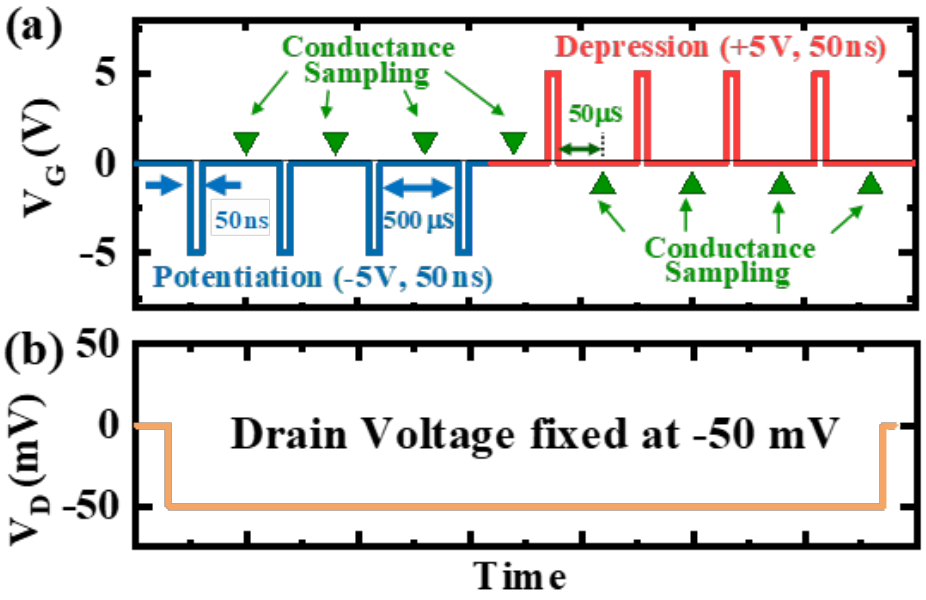

Fig. 4.14. (a) Optimized potentiation (-5 V, 50 ns) and depression (+5 V, 50 ns) pulses for the fabricated Ge FE pNWFET (L = 105 nm, W = 32 nm, H = 26 nm) (b) V_D is fixed at -50 mV.

While optimizing the pulses, freezing of a device was observed frequently when excessively strong pulses were applied. Excessively strong pulses not only represent pulses with long pulse widths or larger voltages but also include significantly larger number of pulses beyond reaching G_{max} or G_{min}. When such freezing happens, the Fe-FET does not respond to subsequent programming signals and requires initialization by applying large (± 5 V) voltage for relatively long time. Although such restoration is still possible in the worst case when the devices get stuck beyond the maximum value, it would be more efficient to use intermediate G range instead of exploiting the maximum range (G_{min} to G_{max}).

4.3 Optimization of update pulses

As mentioned in previous section, pulse optimization criteria should include pulse level (V_G), pulse width and appropriate number of pulses to prevent devices from becoming non-responsive while programming the subsequent conductance value. Fig. 4.14 (a) and (b) depict the optimized pulses for the fabricated Ge FE pNWFET. After testing various pulse widths, pulse levels and number of pulses, separate optimized pulsing conditions were found for both potentiation and depression. With pulse widths for potentiation and depression both fixed at 50 ns, optimum pulse levels for potentiation and depression were determined to be V_G = -5 V and V_G = +5 V, respectively. Time interval between two consecutive pulses was 500 μs and conductance values were sampled 50 μs after each pulse was delivered.

Another crucial factor which is the number of pulses to maximize and minimize the conductance value (G_{max} or G_{min}) were found to be 320 and 256, respectively in the cost of lower G_{max} and higher G_{min} value. Although more than 320 potentiation pulses could be applied for even higher G values, only 320 steps were used to prevent freezing the device. Lower number of pulses for depression (256) was used considering more sensitive nature of conductance profile during depression than potentiation as observed in the previous section (Fig. 4.13). When more than 320 and 256 pulses were used for potentiation and depression, conductance freezing could be observed. Since the number of conductance states were high in this case, multiple pulses may be applied consecutively to form a pulse train and reduce the number of states for various applications that require fewer bits or higher ΔG between states. For example, 10 consecutive pulses as 1 pulse train will result in lower 320/10 = 32 states (5 bits) but 10 times larger ΔG.

Fig. 4.15 (a) shows the accumulated conductance profile after 9 consecutive alternating cycles of potentiation and depression under the optimized pulsing conditions. It can be seen that throughout these consecutive cycles, conductance update was executed repetitively from cycle to cycle. Fig. 4.15 (b) is the overlapped data of

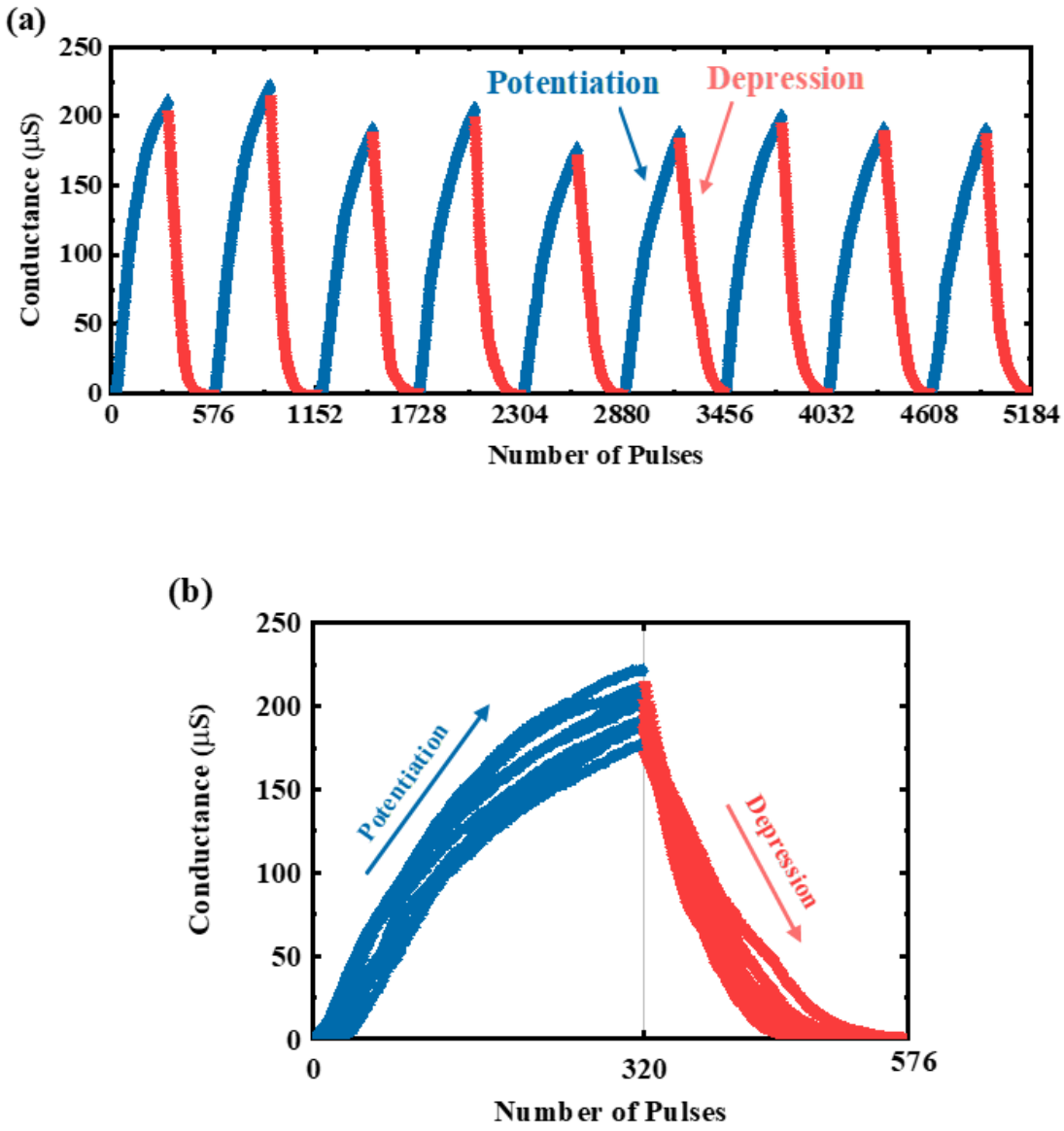

Fig. 4.15. (a) Conductance profile during 9 cycles of consecutive alternating potentiation (-5 V, 50 ns, 320 pulses) and depression (+5 V, 50 ns, 256 pulses). (b) Overlapped curves of (a).

Fig. 4.15 (a). It can be seen that the conductance profile acquired during the multiple cycles is highly reliable and repetitive. The G_{min} state was measured to be well below 1 μS while G_{max} went beyond 200 μS resulting in very high G_{max}/G_{min} ratio (few hundreds). This is also an important factor in improving the online learning accuracy [58, 62].

4.4 On-line learning simulation with Ge FeFET

After acquiring the preferred conductance profiles for potentiation and depression, device parameters can be extracted and simulated through multilyer perceptron (MLP) simulator (+NeuroSim) V2.0 [62]. It is a simulator that trains MNIST handwritten dataset to the MLP neural network. The strength of this simulator lies in its ability to use not only the conventional SRAM-based neural network but also e-NVM devices including the FeFET with non-ideal conductance profiles as synaptic devices. When an e-NVM device such as FeFET is used as a synaptic device, it retains the weight data in the form of conductance since it supports intermediate values (conductance states) within its operating memory range.

As described in Fig. 4.16, a FeFET can be paired with a selector to form a dense array of pseudo-crossbar. By selecting a row (WL, word line) a synaptic FeFET's gate terminal can be accessed through the selector MOSFET which delivers weight update pulses. Then input data (BL, bit line) is given in the form of voltage which then is translated to weighted current because conductance (G) multiplied by voltage (V) is current (I). This current is weighted proportionally with respect to pre-programmed channel conductance (G) of the FeFET. During the inference step, input data are supplied to multiple rows of FeFETs which yield corresponding weighted currents that add up via Kirchhoff's current law.

Since simple data processing (matrix multiplication and addition) and retention of programmable weight data within the synaptic device both happen locally within the dense pseudo-crossbar array, this network can be viewed as a basic non von-Neumann

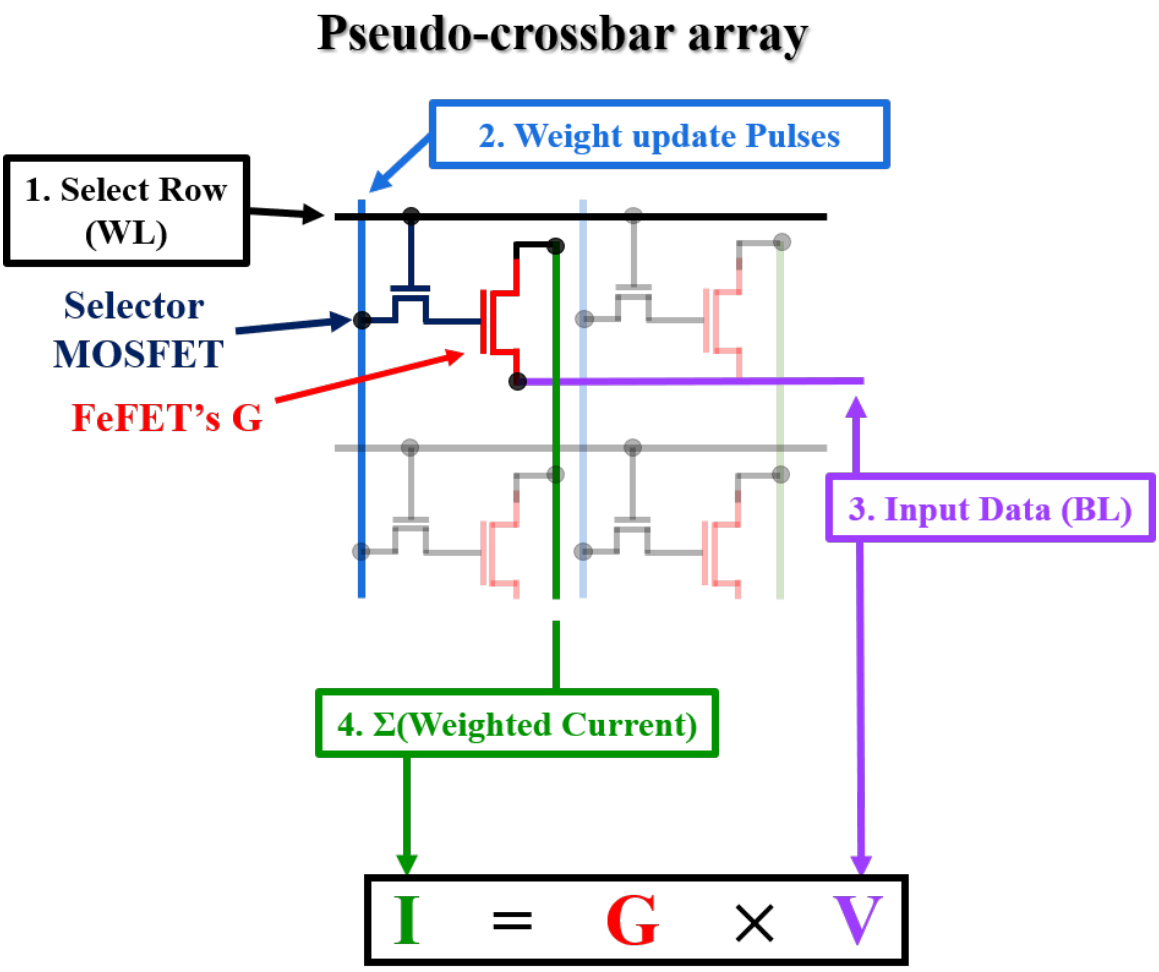

Fig. 4.16. Pseudo crossbar array in a DNN using FeFET as a synaptic device.

architecture that doesn't suffer from memory accessing bottleneck mentioned in the introduction (Section 4.1).

4.4.1 Linearity and asymmetry analysis

To assess the linearity and asymmetry of the conductance profile, curve-fitting model embedded in the simulator was used to extract various parameters. According

to the model, conductance value (G) can be expressed using the following equations (Eq. 4.1 $\sim$ 4.3) where P is the pulse number and A is the normalized fitting coefficient (either positive for potentiation or negative for depression). After loading the measured conductance profile to MATLAB, A_{LTP} and A_{LTD} were first roughly curve-fitted as in Fig. 4.17.

$$G_{LTP} = B(1 - e^{-\frac{P}{A}}) + G_{min} \tag{4.1}$$

$$G_{LTD} = B(1 - e^{-\frac{P - P_{max}}{A}}) + G_{max} \tag{4.2}$$

$$B = (G_{max} - G_{min})/(1 - e^{-\frac{-P_{max}}{A}}) \tag{4.3}$$

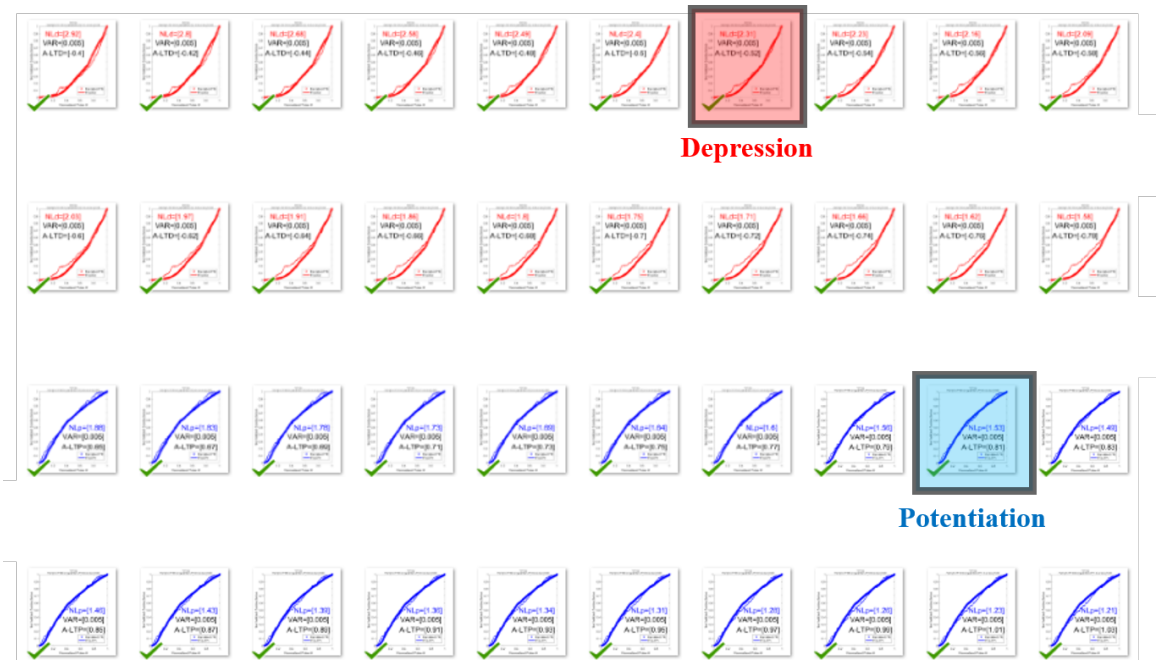

Fig. 4.17. Curve fitting procedure using MATLAB to extract A coefficients for potentiation (Blue, A_{LTP}) and depression (Red, A_{LTD}).

Then corresponding non-linearity coefficients α_p and α_d were found from table included in the simulator. With fixed A coefficients, other parameters such as cycle-to-cycle variation and pseudorandom seeds (parameter 'rng' in MATLAB code) were also taken into account to precisely acquire the most closely-fitted curves as presented in Fig. 4.18. Cycle to cycle variations for potentiation (ρ_p) and depression (ρ_d) from conductance profile of Fig. 4.18 are approximately 1.08 % and 0.31 %, respectively.

Fig. 4.19 compares the improvement in non-linearity coefficients (α_p, α_d) before and after optimizing the pulses. Ideally, both α_p and α_d should be 0 but they approach the desired targeted values of +1 and -1, respectively [62].

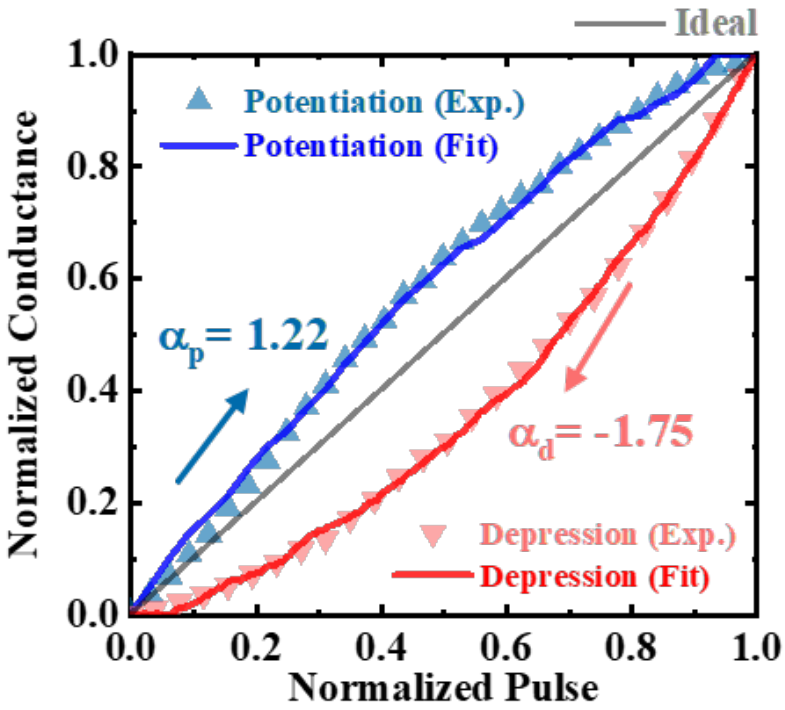

Fig. 4.18. Most closely-fitted curves after loading appropriate parameters and experimentally measured conductance profiles. α_p = 1.22 and α_d = -1.75 give asymmetry ($|\alpha_p - \alpha_d|$) of 2.97.

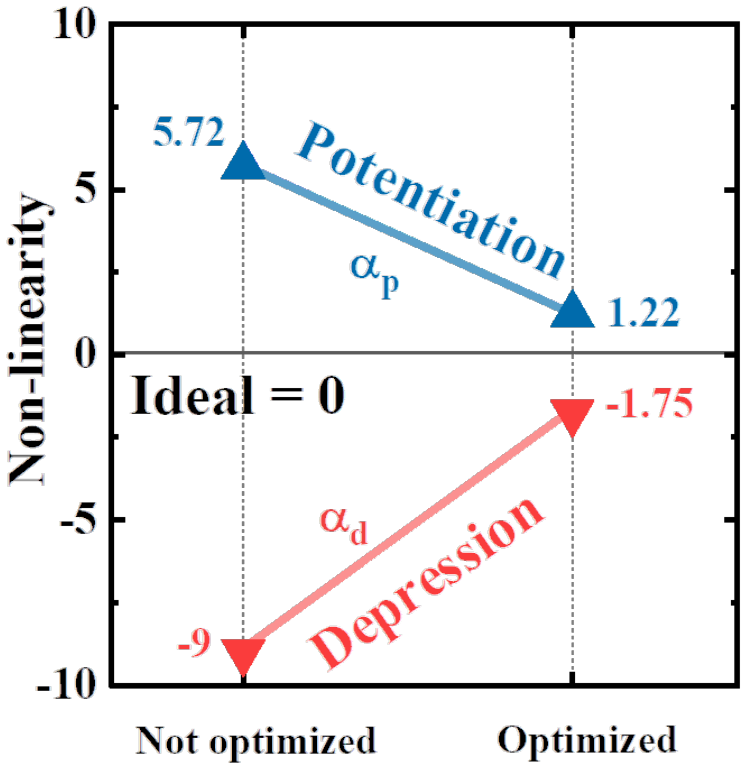

Fig. 4.19. Comparison of non-linearity coefficients (α_p, α_d) extracted from conductance profiles acquired using optimized (Fig. 4.18) and not optimized pulses (Fig. 4.13).

4.4.2 Online learning accuracy of Ge FeFET synaptic device

After extracting non-linearity coefficients (α_p, α_d) from potentiation and depression conductance profiles as described in the previous section 4.4.1, Linux-based simulation can be executed using various experimentally acquired parameters. Fig. 4.20 shows few major parameters that need to be input into the code. Firstly real device simulation mode was selected with FeFET based pseudo-crossbar array architecture. Number of potentiation and depression pulses were input respectively (320, 256) along with the corresponding pulse levels (-5 V, +5 V). 200 μS was used as the G_{max} and

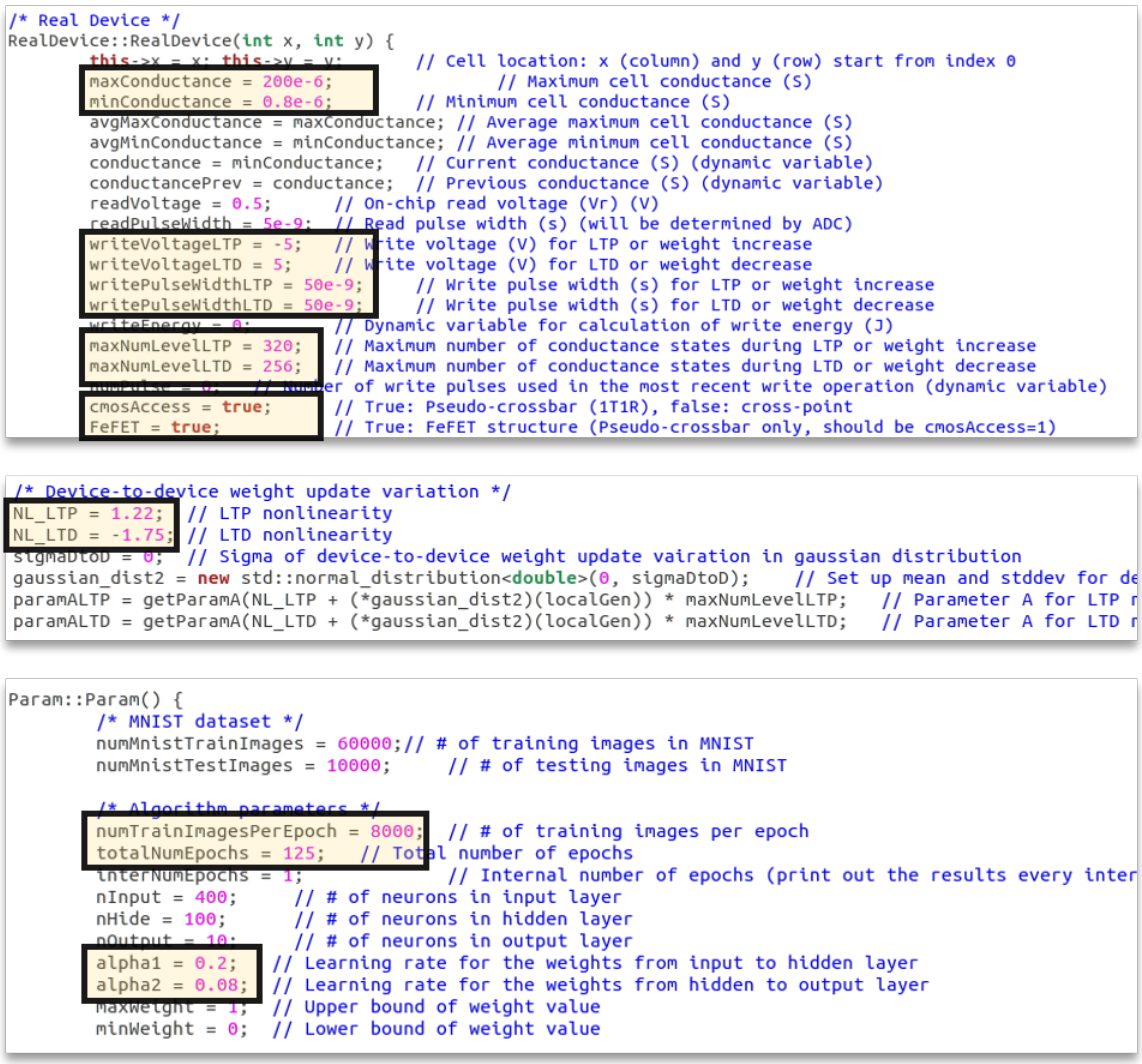

Fig. 4.20. Major parameters that needs to be updated in the simulation code.

0.8 μS as the G_{min}. Pulses width was fixed at 50 ns for both cases. Extracted α_p and α_d were used and number of training images per epoch was fixed at 8000. Total of 125 epochs were trained (1 million hand-written digits) with alpha1 and alpha2 (learning rates) of 0.2 and 0.08, respectively.

The resulting accuracy from the online learning simulation is shown in Fig. 4.22. Accuracy has been significantly improved from 36% up to approximately 88% (highest

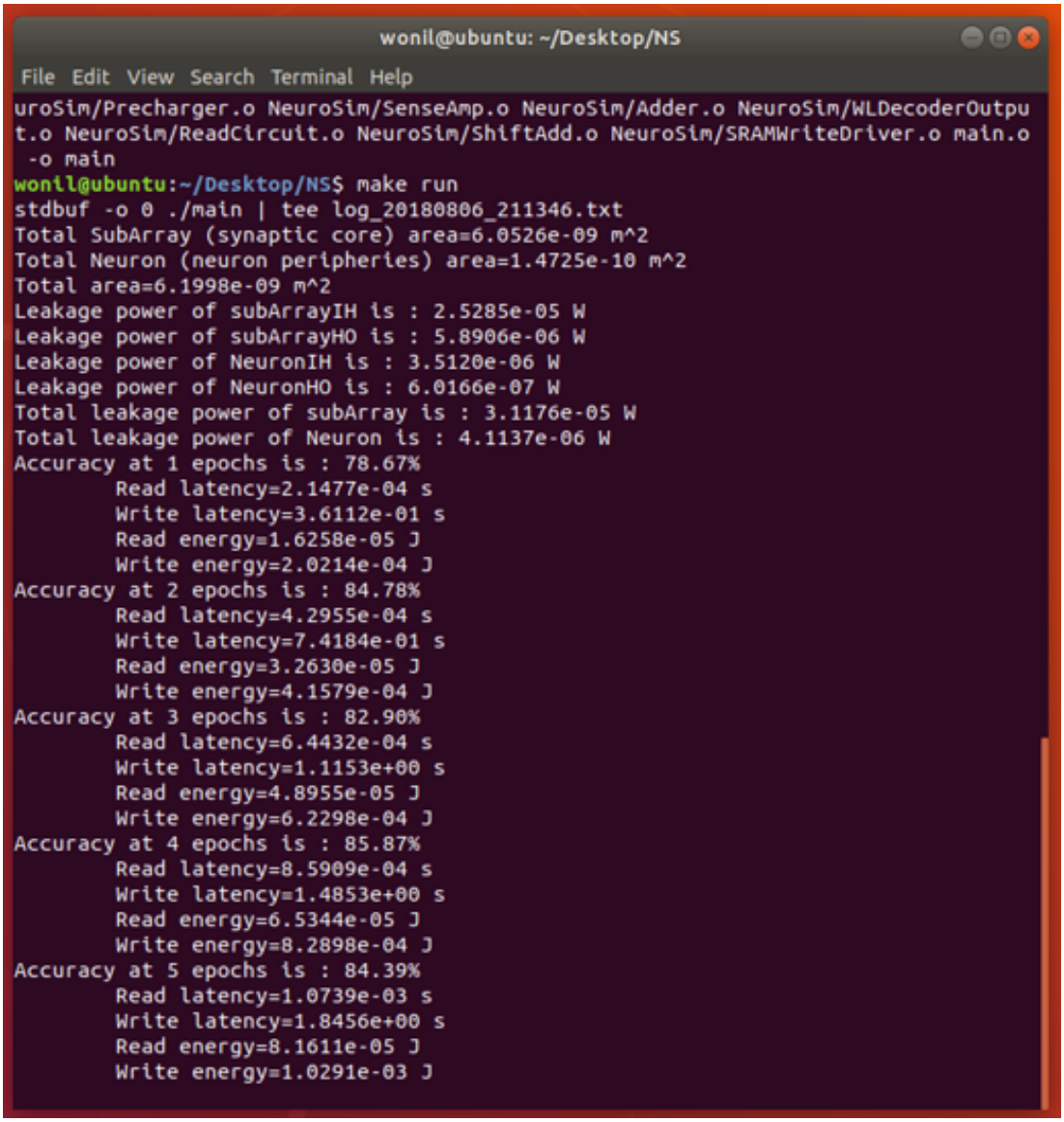

Fig. 4.21. Screenshot taken in the middle of running the online learning simulation.

of 88.7 %) and the asymmetry ($|\alpha_p - \alpha_d|$, ideally 0) was reduced from 14.72 to 2.97 when the pulses were properly optimized.

Fig. 4.23 shows the accuracy throughout the whole 125 epochs of training using the parameters acquired from optimized and un-optimized pulses. Only using the optimized pulse results, various combinations of learning rates (α_1, α_2) were tested. With $\alpha_1 = 0.3$ and $\alpha_2 = 0.08$, the maximum accuracy of 88.51 % was acquired. Even

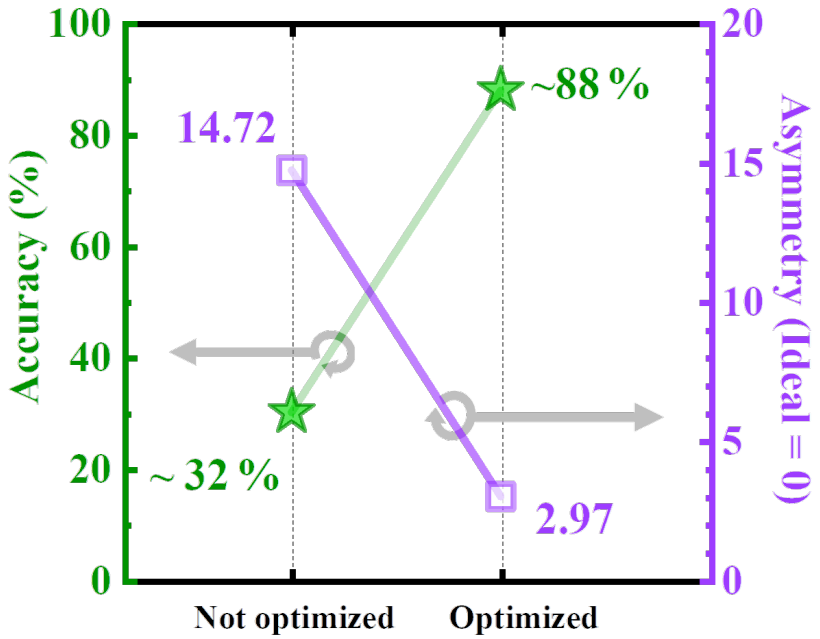

Fig. 4.22. Improvement in simulation accuracy after 125 epochs of training totalling 1 million MNIST images (cropped to 20 by 20 pixels).

without any learning rate tuning, default values of 0.2/0.1 gave 87.69 %. Although further optimization of learning rates, number of neurons and hidden layers may enhance the accuracy of the online learning, it was left as one of the future research topics since this is not the scope of this study.

Table 4.2 summarizes reported simulation accuracy of online learning employing MNIST dataset and respective HZO-based FeFET synaptic device performance metrics.

Table 4.2.
Benchmark of reported works based on FeFET syanptic devices for online learning.

	This Work	**[59]**		**[60]**
Device	Ge FE Nanowire pFET	Si FE Planar nFET		Si FE Junctionless nFinFET
Gate Stack (Thickness, nm)	GeO_x (∼1) + HZO (10) + Al_2O_3 (2)	HZO (10) + SiO_2 (0.8)		HZO (8.5) + SiO_2 (1.5)
Device Dimension	L = 105 nm, W = 32 nm	L = 600 nm, W = 20,000 nm		L = 120 nm, W = 50 nm
# of States (Pot./Dep.)	320 / 256	20	32	>32
Pot. Pulse (Type)	(Identical) 50 ns, 5 V	(Identical) 75 ns, 3.7 V	(Varying) 75 ns, 2.85 ∼ 4.45 V	(Identical) 100 μs, 3.7 V
Dep. Pulse (Type)	(Identical) 50 ns, -5 V	(Identical) 75 ns, -3.2 V	(Varying) 75 ns, -2.1 ∼ -3.8 V	(Identical) 100 μs, -3.2 V
Non-linearity (α_p/α_d)	1.22 / -1.75	5.54 / -8.08	1.75 / 1.46	1.58 / - 7.57
Asymmetry ($\lvert\alpha_p - \alpha_d\rvert$)	2.97	13.62	0.29	9.15
$\mathbf{G}_{max}/\mathbf{G}_{min}$	Few hundreds	∼8	45	4.98
Accuracy (# of trained images)	∼88 % (1 Million)	N/A	∼90% (1 Million)	∼80 % (3 Million)

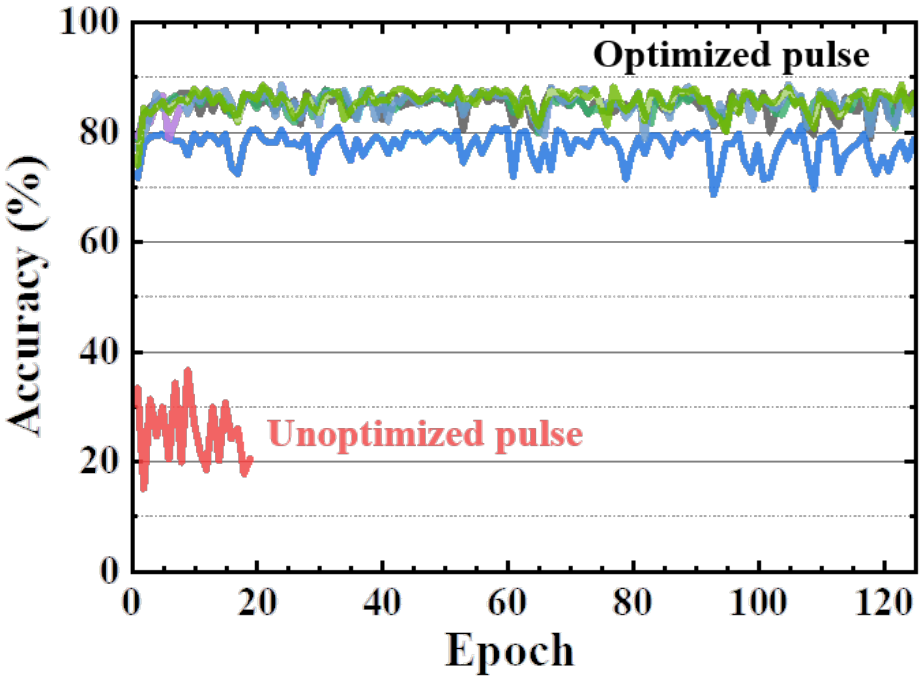

Fig. 4.23. Simulated online learning accuracy throughout 125 epochs of training 1 million MNIST dataset. Various combinations of learning rates α_1, α_2 were tested for conductance profile acquired using the optimized pulse. Un-optimized pulse (red) yields low accuracy.

5. SUMMARY AND OUTLOOK

5.1 Summary

In this dissertation, nanoscale CMOS devices based-on germanium 3D structures (FinFET and nanowire) were fabricated and studied. Integration of ferroelectric material was done into the conventional germanium MOS devices.

- Chapter 2 studied the integration and fabrication of ferroelectric ALD-deposited $Hf_{0.5}Zr_{0.5}O_2$ (HZO) oxide into the advanced germanium 3D platform. Large ferroelectric voltage hysteresis was seen with abrupt switching due to polarization of ferroelectric oxides. Time response of polarization switching within germanium nanowire FeFETs down to 100 ps was experimental observed in real-time with ultrafast pulse measurement set-up. The fastest switching of polarization within 10 nm of ALD-deposited HZO was found to be 3.6 ns. Sub-10ns polarization switching was observed in real time in collaboration with NIST. Picosecond pulse generator was configured with high performance oscilloscope to probe the polarization switching in sub-ns regime. Although a single 100 ps pulse at -6 V did not cause the switching, accumulated 100 ps pulses in the form of pulse train did gradually switched the FeFET and increased the current.

- Chapter 3 includes the first demonstration of hysteresis-free germanium CMOS NC FinFETs with sub-60mV/dec SS bi-directionally at room temperature. Minimum extracted SS (mV/dec) in forward/reverse direction were found to be 56/41 for the pFinFET and 43/49 for the nFinFET. Parameters that describe the short channel effects within conventional MOSFETs were studied statistically (measured and averaged from approximately 10 $\sim$ 20 devices per dimension) in fabricated germanium NC FinFETs. It was statistically observed

that DIBL and SS was reduced when compared to our reported germanium FinFETs with identical fabrication processes. V_T roll-off was less severe in NC FinFETs as well due to negative DIBL present in NCFETs.

- Chapter 4 shows the possible application of Ge FeFETs as synaptic devices for neuromorphic computing. Ferroelectric HZO was integrated into Ge nanowire structures and optimum potentiation/depression pulses were found to yield improved linearity and symmetry of conductance profiles with high number of states and G_{max}/G_{min}. Using MLP simulator and NeuroSim V2.0, online learning accuracy of approximately 88% was achieved from measured device parameters.

5.2 Outlook

More detailed works based on the studied results so far can be carried out in the near future as elaborated below.

- Study of reliability in ferroelectric material to study fatigue in ALD HZO for its application towards more robust memory device.

- Further study on the time response of polarization in ferroelectric (FE) and anti-ferroelectric (AFE) ALD-deposited HZO film considering switching speed difference in FE and AFE HZO.

- Integration of anti-ferroelectric material into germanium 3D structures for control of NC region within the operating voltage range.

- Application towards the neuromorphic synaptic devices using Ge FE and AFE Fin/nanowire FETs. Circuit simulation based on measured experimental data.

- Realization of neuromorphic circuitry including selectors and synaptic FE/AFE SOI/GeOI devices.

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VITA

Wonil Chung was born in January 1987 in Seoul, Republic of Korea. He entered Hanyang University in 2005 and received his B.S. in Department of Electronic Engineering in 2012, including 27 months of military service in power and generator operation division of Seoul Airbase, Republic of Korea Air Force. In 2012, he joined Professor Byung Jin Cho's group in Department of Electrical Engineering of Korea Advanced Institute of Science and Technology (KAIST) and received his M.S. degree in 2014. His research topic was on improvement of electrical properties in higher performance germanium MOS devices. With a novel process of vacuum annealing and in-situ ultrathin Hf and Zr capping layer on Ge, improvements in EOT and leakage current were achieved. In 2015, he joined the School of Electrical and Computer Engineering of Purdue University for his PhD study advised by Professor Peide Ye. His research topic covers integration of ferroelectric oxide into high performance nanoscale 3D germanium (GeOI) and silicon (SOI) devices for applications towards steep-slope devices, ferroelectric devices and neuromorphic synaptic devices.

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