HIGH TEMPERATURE SEMICONUCTING POLYMERS AND POLYMER BLENDS

by

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To my family.

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ABSTRACT

Organic semiconductors have witnessed a prolific boom for their potential in the manufacturing of lightweight, flexible, and even biocompatible electronics. One of the fields of research that has yet to benefit from organic semiconductors is high temperature electronics. The lightweight nature and robust processability is attractive for applications such as aerospace engineering, which require high temperature stability, but little has been reported on taking such a leap because charge transport is temperature dependent and commonly unstable at elevated temperatures in organics. Historically, mechanistic studies have been bound to low temperature regimes where structural disorders are minimal in most materials. Discussed here is a blending approach to render semiconducting polymer thin films thermally stable in unprecedented operation temperature ranges for organic materials. We found that by utilizing highly rigid host materials, semiconducting polymer domains could be confined, thus improving their molecular and microstructural ordering, and a thermally stable charge transport could be realized up to 220°C. With this blending approach, all-plastic high temperature electronics that are extremely stable could also be demonstrated. In efforts to establish a universal route towards forming thermally stable semiconducting blends, we found that the molecular weight of conjugated polymer plays a crucial role on the miscibility of the blends. Finally, we found that the choice of the host matrix ought to consider the charge trapping nature of the insulator.

CHAPTER 1. GENERAL INTRODUCTION

1.1 Charge transport in organic semiconductors

Since the demonstration of semiconducting and conducting properties in organic materials by Prof. Alan Heeger and colleagues,[1-3] this class of materials has gained tremendous attention for a multitude of applications.[4-6] Though these materials were not necessarily destined to rival the inorganics such as crystalline silicon, they offered other features that remain challenging to realize in inorganic systems including solution processability into thin films, flexibility, as well as biocompatibility.[7-15] Experimentally, the electronic performances of organic materials are commonly characterized in terms of their charge carrier mobility either in a diode configuration, a field-effect transistor, or using other setups such as time of flight and pulse radiolysis. Organic field-effect transistors (OFETs) became one of the most widely studied electronic configurations.[16-21] A FET is a three terminal electronic device consisting of a semiconducting layer deposited between two ohmic contacts (source and drain), separated by a thin dielectric layer from a third contact, the gate.[22-25] The gate can be positioned either on the top (top gate) or at the bottom (bottom gate). In some cases, the gate can also serve as the substrate, otherwise, the assembly can be patterned on a substrate (glass, plastic, or silicon).[26-30] A FET provides amplifying and/or switching of electronic signals passing through the semiconducting layer as a response to a certain voltage applied to the gate contact (V_G).[30, 31] The amount of current that is able to flow between the source and drain—through the active layer—subsequently marks the device's performance in terms of its ability to transport charge carriers. In a such simplistic device architecture, OFETs have then been used as one of the robust ways to extract and benchmark the semiconducting properties of organic materials. These electronic devices have thus been widely

studied to the extent of improving the primitive charge carrier mobilities from $\sim 10^{-5}$ to higher than tens of cm^2/Vs.[32-34]

Ordinarily, the transistor performance is tested by analyzing the channel layer's transductance as a response to an applied bias at the gate (V_G). By applying another voltage (V_{DS}) between source and drain contacts, the performance of the channel layer can be monitored from the current flow through the organic material. Extrapolating transfer and output curves, a few key parameters are usually reported to characterize OFET performance. First, charge carrier mobility (μ), ON/OFF current ratio, as well as the threshold voltage (V_{TH}) are to be evaluated. Charge carrier mobility tells how fast the charge carriers can move from one contact to the other, while the ON/OFF ratio shows the difference between currents before the device could be turned "ON" and when the device is switched on. The threshold voltage is an indication of the minimum voltage V_{DS} that must be applied before the device can be "turned on". V_{TH} is oftentimes reported with its subthreshold slope (SS) which is the voltage difference required to increase the current between source and drain by a factor of ten. Notice the dependence of the threshold voltage on any fabrication defects, since any pinholes or leakages—contact resistance—would have to be energetically filled before the device can turn on. Also note that the organic-based systems borrow these parameters from the inorganic semiconductors that are used as model systems to derive the parameters.[24] The devices architectures, charge transport mechanisms, the intrinsic structure-to-property dependence have been widely reported and are beyond the scope of this discussion. In the current discussion, we focus on the influence of temperature on electronic performance, more specifically dedicate more effort on high-temperature stability.

1.2 Influence of temperature on charge transport in organic semiconductors

Fundamentally, charge transport in semiconductors is a combination of temperature dependent processes: i) the temperature dependence of the concentration of charge carriers; ii) the activation energy required to excite carriers into higher energy level; iii) temperature-dependent delocalization of carriers; and the iv) temperature-induced lattice expansion and charge scattering.[35] Regardless of the doping level, the intrinsic carrier concentration will increase with increasing temperature. In terms of stability, this increase of carrier concentration is not necessarily detrimental with moderate temperatures. In fact, most semiconductors perform optimally between room temperature and 80°C. In highly crystalline materials, as it is the case for inorganic semiconductors, carrier scattering becomes problematic once the concentrations become too high and charge carrier mobility becomes slower. Charge carrier mobility gradually decreases as the temperature increases due to excessive carrier concentration increases that lead to carriers scattering and ineffective delocalization. This behavior is quasi linear in high performance materials (mostly inorganics) where band transport is the main carrier pathway. As the lattice expands and scattering arises, the performance drops. For lower performance materials, mainly lower crystallinity and "impure" materials, temperature is initially beneficial. This is because in these lightly doped and lower mobility materials, charge transport mechanism typically involves hoping behavior.[36-41] That is, carriers need activation energy to hop between domains. However, this thermally-promoted behavior is only observed with moderate heating. Beyond the optimal range, lattice scattering takes over again, and charge mobilities begin to decline once more.

This behavior becomes of interest not only for fundamental research but also because in real device applications, the increase in temperature typically translates to i) increasing intrinsic carrier density (doping becomes ineffective); ii) exponentially increasing junction leakage current (degrades performance, increases power consumption); iii) increased electromigration in

conductors (lower reliability, shorter lifetime); iv) decreased dielectric breakdown strengths; v) mechanical stress due to coefficient of thermal expansion (CTE) mismatch; and vi) variation in device parameters. These changes are mirrored by the changing transfer characteristics where the transistor device's amplifying abilities begin to decline.[42] Consequently, a lot of efforts are put into insulating and cooling the functional component in integrated circuits to ensure the surrounding temperatures do not elevate beyond optimal ranges. This cooling requirement in most electronics imposes not only a weight burden but also increased manufacturing and maintenance cost. The ideal case to obviate the need for insulation and cooling would be the use of semiconducting materials that are intrinsically thermally resistant. Wide band gap (WBG) materials have been proposed and studied for their thermal stability. With more energy levels to be populated upon temperature increase, materials such as silicon carbides (Si-C) show to maintain much lower carrier concentrations than the ubiquitous silicon.[42-44] In fact, the starting (i.e. room temperature) intrinsic carrier concentration of Si is nearly equivalent to that of 6H-SiC when the latter is studied at 225°C. This thermal tolerance of WBGs has kindled the exploration of carbides and nitrides for high temperature applications.[42] At elevated temperatures, as high as 500°C, doping remains relatively effective in WBGs and signal modulation can still be realized in thermal regimes where the traditional silicon begins to malfunction. However, these materials are still rare, and their crystal growth remains challenging to realize. In addition, these materials tend to be expensive, not to mention heavy. This heavy and brittleness nature makes WBG materials less attractive candidates for technologies such as aerospace engineering. Besides, the use of these highly crystalline would not overcome the bottleneck that is the lattice expansion which leads to decrease in charge carrier mobilities due to scattering.

Organic semiconductors present a special case in the design of high temperature operating electronics. Most organic semiconductors are not highly crystalline in nature which renders charge mobility in these systems thermally favored mostly through the hoping mechanism.[20] In organic transistors, charge carrier mobility, the most common figure of merit for transistor performance evaluation has been shown both theoretically and experimentally to be temperature dependent.[20] Charge transport is mostly affected by structural defects within the organic layer at the interface, the surface topology and polarity of the dielectric, and/or the presence of traps at the interface (that depends on the chemical structure of the gate dielectric surface). Additionally, contact resistance at the source and drain metal/organic interfaces plays an important role. The contact resistance becomes increasingly important when the length of the channel is reduced, and the transistor operates at low fields. In this scenario, any barriers to the injection of carriers from the metal to the channel will easily reflect in the transistor device's performance. Within the device channel, the key parameter that dictates the thermal dependence of transistor performance is the thermally induced disorder which is directly related to the channel resistance. Disorder is commonly described in two different types:[20] i) diagonal disorder which refers to the fluctuations in energy levels of individual molecules witch the materials. This disorder is commonly found in single crystal semiconductors. In less ordered materials such as semiconducting polymers, the ii) off-diagonal disorder is typically observed. It describes the variations in the coupling strengths between adjacent molecules or chain segments in the case of polymers. This type of disordering is commonly contributed by conformational freedom that leads to torsional fluctuations between segments.[20]

Though charge transport in organics shows to benefit from the thermal activation energy, the realization of high temperature operation stability remains challenging in these systems.[45] This

is mainly because with increasing temperature, though the hoping is favored, other factors including lattice expansion and unstable morphology which contribute to the disordering discussed above begin to impede charge carrier transport. For instance, this behavior was found in early studies on thermally sterilizable medical devices by Sekitani et. al.[46]. The authors carried out temperature dependent characterization on pentacene based transistors and showed that the charge transport increases with increasing annealing temperature up to 140°C then declines with further temperature increases. It was found that the morphological changes in the film were the major contributors to the declining performance. The disorder within the crystal-based film lead to ineffective charges delocalization and therefore poor transistor performances. To improve the thermal stability window, the authors further utilized the conjugation extension strategy and made dinaphtho-thiophene (DNTT) as pentacene derivative.[47] They found that DNTT exhibits a much better packing in comparison to pentacene and that this improved ordering could help maintain ordering even after high temperature pasteurization. DNTT based transistor devices thus offered improved thermal stability as well as improved mobilities. To further induce efficient stacking between the DNTT molecules the group introduced phenyl groups to extend the conjugation, improve processability, and thus synthesize DPh-DNTT.[48] With this molecular design, transistor devices that can remain functional after annealing at 250°C could be realized owing to the improved stacking within the crystalline films. In this approach, the use of phenyl pendant groups was found more beneficial than using long alkyl chains. The latter were found to be more prone to disordering at high annealing temperatures as the films packing behavior could be altered by annealing effects. This thermal stabilization approach by inducing better packing was further adopted by other research groups either by introducing "V-shaped" cores[49] and by extending the conjugation using conjugated pendants groups.[50] With these strategies, organic small-molecule

based transistors for medical devices that could survive sterilization temperatures up to 300°C could be fabricated From these series of studies, the following could be learned in quest for high temperature operation: [46, 50-54] i) the thermally promoted transport in organic materials is mainly hampered by unstable morphologies and defects formation at elevated temperature. ii) Improved ordering achievable through molecular design strategies, leading to retain close packing at elevated temperature leads to improved thermally-stability. And iii) large pendant groups which help prohibit molecular rearrangement upon heating can improve the semiconductor's thermal stability. Though the use of these small molecule semiconductors has promised relatively excellent stability at high temperatures, their difficult processability into thin films, complicated device architectures, and limited scope have limited the emergence of these materials as potential candidates for applications. Besides, most of the studies on such devices have merely focused on the effects of annealing and unstable performances remain an issue when in-situ thermal stressing is in effect.[51, 55] The pursuit of thermally stable and even thermally insensitive material systems remains of great interest to the field as recent theoretical predictions show that by marrying the degree of charge delocalization with the available density of states, a temperature independent charge transport regime is attainable.[36] Though such a behavior has yet to be demonstrated in practice where disorder is more challenging to foresee than in theory, the fundamental understanding and the need for high temperature electronics are still important drivers for this field both towards the design of new semiconductors and the devices demonstrations.

1.3 Influence of temperature on charge transport in conjugated polymer thin films

Semiconducting polymers, commonly in their thin film form exhibit a rather more complex charge transport behavior.[38, 39, 56] Since the mobility extraction involves channels that are several micrometers long and up to a millimeter wide, for the charge carrier to reach the drain contact from

the source, the carriers will not only hop between neighboring polymer chains but will also have to overcome the energy barrier in less ordered domains. It is also to be noted that given the bundle-like nature of polymers, it is nearly inevitable to hit dead-ends for the hopping carriers. In polymer thin films, charge mobility has thus been defined as thermally-activated process due to the inherent required activation energy for charge hopping. At elevated temperatures, similarly to small molecule based thin films, polymer thin films will undergo disordering. As mentioned in sections above, torsional fluctuations in polymer chains are the main source of disordering. This distorting nature is accentuated when enough thermal energy is added into the material systems. The disordering is most likely promoted when the lattice thermally expands, giving the chains enough degree of freedom to disentangle, unfold, and unpack.[57-59] For instance, through in-situ temperature dependent analyses of diketopyrrolopyrrole (DPP)-based donor acceptor polymer thin films, Zhao et al. found that with increasing temperature, the thermal expansion within the π-π stacks leads to worsened interchain packing in the polymer films.[57] The crystallographic peak corresponding to the π-π stacks showed to decline in intensity concomitant to the thermal expansion. The corresponding transistor devices further exhibited a thermally dependent behavior with increased mobilities up to near 140°C and a decline with further increase in temperature.

This poor morphological and electronic stability in polymers has thus limited the investigation on thermal stress effects on the operation of polymer-based devices. A few strategies including tuning the HOMO energy levels, high temperature pre-annealing, and sidechain engineering have been proposed to enable stability towards annealing temperatures,[45] but no demonstration on high temperature stable operation has been reported despite recent growing interest in polymer-based electronics. Despite the fact polymers are classified amongst the most thermally resistant materials known to date, semiconducting properties have yet to benefit from

such robust nature. We believe this is mainly because most fundamental studies on electronic performance in organics have focused on low temperature regimes. Consequently, both materials design fundamentals as well as organic electronics characterizations have seldomly explored the other end of the spectrum. Though the field of "high temperature electronics" has existed for many years, organic materials have barely taken part in such a discussion in terms of charge transport.

In retrospect, organic materials are mostly understood to be soft in nature. The higher the temperature, typically the softer the polymeric materials, for example, will get. As we mentioned above, this softening has been believed to be detrimental to the electronic performance. However, given the structural tunability offered by polymers, we don't believe that the discussion should be halted simply because the semiconductor softens. We believe there exist several tools to tune such properties either through sidechains and backbone engineering or composites formation without sacrificing the electronic properties of the semiconducting polymers. Since, such approaches have been used to attain ultra-soft and even stretchable semiconductors,[60-65] the same could be said about realizing ultra-rigid counterparts. This dissertation will thus focus on the rigidification approaches for high temperature semiconducting polymers and polymer blends.

1.4 Objectives of this dissertation

In the following chapters, we aim to fully understand the governing factors towards unstable electronic performances in semiconducting polymers and how to mitigate such factors to realize high temperature operation stability. Inspired by the reports on small semiconductors, we will focus on minimizing disorder in polymers as a venue towards high temperature electronic tolerance. To attain the rigidification concept in polymer films, we will explore the use of blend composites. We will discuss the design strategy towards high temperature semiconducting polymer blends through an original approach that utilizes high glass transition temperature host

materials. Through a systematic materials selection, we aim to demonstrate that this approach is a simple and generalizable route towards the fabrication of thermally stable organic transistors. We will then demonstrate the ability of our blending design to enable all-plastic transistors devices that are extremely thermally stable. From both the materials design approach and device manufacturing viewpoint, we will highlight how to fabricate transistors that are functional even under baking oven conditions. We will then discuss factors to be considered when designing thermally stable blends including the size of polymers, i.e. the molecular weight, the processing conditions, as well as the selection of the chemical nature of the blending components. After demonstrating the generality of the blending strategy, we will also discuss principles to optimize the electronic performance of the blend films especially by selecting low dielectric rigid materials We will close our discussion with an outlook on the potential found in polymer-based high temperature electronics both for applications and for fundamental investigation on temperature dependence of charge transport.

CHAPTER 2. HIGH TEMPERATURE OPERATION IN SEMICONDUCTING POLYMER BLENDS

2.1 Introduction

Although high temperature electronic operation (i.e., beyond 150°C) is of great interest for many applications, it is fundamentally challenging to achieve stable carrier mobilities for semiconductors at elevated temperatures. Applications requiring electronics that can withstand harsh temperatures range from daily appliances (ovens, cellphones, computers, etc), to vehicles, space shuttles, and oil drilling devices. Despite the growing demand for high temperature electronics, both inorganic and organic semiconducting materials have yet to deliver the needed stability. For inorganic semiconductors the performance is typically optimized for operation at ambient temperatures and degrades at elevated temperatures. In these highly crystalline materials, when the operating temperature increase, a lattice expansion accompanied with increased charge carriers concentration results. Charge carriers will be thermally promoted across the band gap, which leads to increased carrier densities, ineffective doping, and junction leakages; the expanding lattice also leads to scattering and reduced charge carrier mobility [42, 66, 67]. To improve the device performance and lifetime in these harsh thermal conditions, wide-band gap materials as well as the use of increased amounts of insulating components have been utilized [43, 44]. For wide band-gap materials (e.g. carbides and nitrides), more energy levels become available which enables the semiconductors to remain functional at much higher temperatures. However, these materials are rare, challenging to process, and their heavy nature limits the scope of their application. Commonly, active or passive cooling, as well as thermally-engineered packaging are needed to maintain the optimal electronic performance [68], but these approaches impose cost and weight and are thus inefficient for the applications mentioned above.

In contrast, organic semiconductors commonly display thermally-activated charge transport features [69, 70]. Most organic semiconducting materials are not highly crystalline in nature as it is the case for inorganics. This implies that charge transport is facilitated with moderate temperature increases, leading to improved performance [20]. This thermally-promoted behavior is a result of the hoping of charge carriers between ordered domains. With increasing temperature, the charge carrier mobility along with other electronic parameters typically improve. However, this thermally-activated charge transport becomes counteracted by unstable morphologies and disrupted molecular packing at higher temperatures, especially in polymer thin films [52, 57]. For example, it was shown in organic small molecules that, the electronic performance could increase up to 150°C but then the morphology began to vary, the molecular packing started to become weaker, and the electronic performance started to decline. In most reports on small molecule semiconductors, high-temperature annealing effects have been the main focus and a few studies explored the effect of in-situ thermal stress,[46, 51, 53, 55] but in all reports, charge-carrier mobilities have been temperature-dependent and start to decline beyond 150°C. A similar behavior was also observed in conjugated polymer thin films. In-situ temperature dependent crystallography analyses could reveal that the excess thermal expansion results into a complete dissolution of the π-π stacks which could be mirrored in decline charge transporting ability.[57] Since organic electronics have shown attractive features such as their low cost processability, flexibility, and in many cases biocompatibility, [71] it is important to explore their potential in the manufacturing of thermal stable electronics.

In this chapter, we will introduce a general strategy to make thermally-stable high-temperature semiconducting polymer blends, composed of interpenetrating semicrystalline conjugated polymers and high glass-transition temperature insulating matrices. We first

demonstrate that by physically rigidifying polymer thin films by adding a high Tg matrix, the thermally activated charge transport can be rendered stable at higher temperatures in comparison to the pristine conjugated polymer film. To explain the observed thermal stability, we will look at the effect of blending of film morphology, chain packing and ordering, and utilize computational tools as a guideline. We will also discuss the generality of the blending method by, first utilizing several high Tg matrices to demonstrate high temperature operation, then expanding this design onto other conjugated building blocks, even n-type polymers. We will close the chapter by laying out important aspects towards achieving high temperature operation in semiconducting blends, and by outlining current challenges as well as the potential that is found in these composites.

2.2 Experimental

2.2.1 Materials

P1, P2, P3 were synthesized and the corresponding molecular weights were evaluated by gel permeation chromatography (GPC) as previously reported.[72-74] Poly(9-vinylcarbazole) (PVK, average Mw 25,000-50,000), polyacenaphthylene (PAC, average Mw 5,000-10,000), and polymethyl methacrylate (PMMA, average Mw 15,000) were purchased from Sigma Aldrich and used as received. Polycarbonate (PC), polyetherimide (PEI), and Matrimid® 5218 (MI) were purchased from PolyK Technologies and purified by precipitation and filtration in methanol before use. All polymer solutions for thin film formation were obtained in chloroform (10 mg/ml) and allowed to stir for 10 hours. The blends were obtained by mixing the appropriate volume percentages for at least 1 hour. Poly(dimethylsiloxane) (PDMS, Sylgard 184, Dow Corning) was prepared at ratio of 10:1 (base/cross-linker, w/w) and cured at 80 °C for 4 hours and used for film delamination. Octadecyltrichlorosilane [75] used for surface modification was purchased from Sigma

Aldrich and used as received. The molecular weight distributions of the studied semiconducting polymers are summarized in Table 2.1 and the glass transition temperatures of the studied matrices are shown in Table 2.2.

Table 2.1 Summarized molecular weight values of the studied semiconducting polymer materials. Low molecular weight extracts were used in this study as they could be easily solution processed into thin films from the blend solutions with the matrices. [a]Trichlorobenzene was used as the eluent at 150 °C.

Semiconducting Polymer	M_n **(kDa)**[a]	$Đ$
DPP-P1	30.7	3.6
DPP-P2	26.5	1.7
Isondigo-P1	28.0	4.0

Table 2.2. Summarized glass transition temperatures (T_g) of the studied host matrices and the corresponding molecular weights. [b]Dynamic scanning calorimetry (DSC) scans were taken at 10 °C/min heating/cooling rates. [c]Tetrahydrofuran was used as the eluent at room temperature.

Matrix Polymer	T_g **(°C)**[b]	M_n **(kDa)**[c]
PVK	210	23.7
PAC	265	67.0
PC	182	23.4
PMMA	109	15.0
PEI	263	37.8
MI	325	7.2

2.2.2 Thermal transition measurements

The glass transitions of the studied matrix polymers were verified by dynamic scanning calorimetry (DSC). The DSC thermograms were measured using a TA Q5000 calorimeter. The polymer sample was sealed in a hermetic aluminum pan and measured under nitrogen purge (50 mL / min). The sample was heated and cooled in two cycles between -30 to 400°C (or otherwise as indicated), with the first cycle removing any thermal history of the sample. The heating and cooling rates for all measurements were 10°C / min.

2.2.3 OFET devices fabrication and characterization

A heavily n-doped Si wafer with a 300 nm SiO_2 surface layer (capacitance of 11 nF/cm^2) was employed as the substrate with Si wafer serving as the gate electrode and SiO_2 as the dielectric. The gold source/drain electrodes were sputtered and patterned by photolithography technique. The device channel width was 1400 µm and the channel length was 50 µm. For the octadecyltrichlorosilane surface modification, the silicon wafer (with Au bottom contact) was first cleaned with hot piranha solution (H_2SO_4 (98%):H_2O_2 (30% water solution) = 7:3) followed by a copious rinsing with water. It was then further subjected to sonication sequentially in water and acetone for 5 minutes each. After drying at 80°C inside an oven, the silicon wafer was then put in a clean and dried Petri dish with a small drop of OTS in the center. The dish was then covered and heated in a vacuum oven at 120°C for 3 hours, resulting in the formation of an OTS self-assembled monolayer on the surface. The OTS-modified substrates were rinsed with hexane, ethanol, and chloroform and blow-dried by nitrogen. During the temperature-dependent analyses, the contribution from the thermal expansion of the substrate was assumed to be negligible for the studied temperature range. The semiconductor layer was deposited on the OTS-treated Si/SiO_2

substrates by spin-coating with speed of 2000 rpm for 30 seconds. The solvent used is chloroform. The concentrations of the solutions used for spin coating were 10 mg/mL. The devices were annealed in a N_2 glovebox up to 200°C then slowly cooled to 25°C prior to electrical measurements.

OFET devices characterizations were carried out using a Keithley 4200 both in ambient and under N_2 environment. The field-effect mobility was calculated in the saturation regime by using the equation $I_{DS} = (WC_i / 2L)\mu(V_G - V_T)^2$, where I_{DS} is the drain-source current, μ is the field-effect mobility, W is the channel width, L is the channel length, C_i is the capacitance per unit area of the gate dielectric layer, V_G is the gate voltage, and V_T is the threshold voltage. OFET performances were obtained by applying a gate bias from −60 V to 6 V, with the potential gradient between the source and drain contacts kept at −60 V. To control the thermal conditions, the HFS600E-PB4 Linkam stage was used, and for the measurement carried under inert environment, the stage chamber was first purged for 10 minutes and hermetically filled with N_2 gas prior to measurement. The heating and cooling rates were maintained at 10°C/ min and OFET devices were allowed to reach thermal equilibrium for 30 minutes at each temperature before measuring.

2.2.4 Morphology analysis

Polymer thin films were spin cast on cleaned and OTS-modified Si/SiO_2 substrates. The film thickness was measured to be around 170 nm when chloroform was used as a solvent. AFM images were taken using Cypher Asylum AFM and processed through Gwyddion Software. For the in-situ temperature dependent morphology study, the films annealed at 50ºC for solvent removal were first imaged with the temperature on the sample stage maintained to 25ºC. The sample stage temperature was then increased to 120ºC (the instrument limitation), and the films were re-imaged for comparison. The same samples were further heated to 220ºC in open air and re-imaged.

2.2.5 In-situ temperature-dependent Grazing Incidence X-ray Diffraction (GIXD)

GIXD measurements were performed at the Stanford Synchrotron Radiation Lightsource (SSRL), generated with a 24-pole, 2-Tesla wiggler insertion device. Beamline 11-3 utilizes a beam of energy of 12.7 keV with a 2 x 10^{12} photons/s flux. The beam grazed the sample at an incidence angle of 0.12 for 180 seconds, and the resulting diffraction pattern was collected onto a 2D area detector 315 mm away. Lanthanum hexaborate; a polycrystalline material, was used to calibrate the sample-to- detector distance as well as the scattering vector. The beam footprint is 3.0 x 0.15 mm and was shaped with adjustable slit widths. TIFF files were generated at beamline 11-3 and were processed in WxDiff. Prior to collecting any GIXD measurements, the film on Si/SiO_2 substrates was annealed thermally at 200°C in a He atmosphere. The sample was allowed to "equilibrate" at a given temperature for 5 minutes prior to collecting the respective diffraction pattern.

2.2.6 UV-Vis spectroscopy

Samples were prepared by spin casting the chloroform polymer solutions onto cleaned glass substrates. All absorption spectra were collected using a UV/Visible/NIR Cary 3000i spectrophotometer. To compare aggregation behavior between films of pure P1 and its PVK blends, and to probe the effect of temperature on the formed aggregates, all films were annealed to 200ºC and slowly cooled down to room temperature inside a N_2 glovebox before each measurement. In-situ absorption spectra were recorded at different temperatures using the HFS600E-PB4 Linkam stage. Each sample was first carefully mounted inside the stage and hermetically encapsulated in the N_2-purged chamber. The stage was then brought into the light path of the UV/Visible/NIR Cary 3000i spectrophotometer. Prior to each measurement, each sample was allowed to reach

thermal equilibrium for 30 minutes. The HFS600E-PB4 Linkam stage with a clean glass slide hermetically mounted in the chamber was used as the baseline and the background spectra were obtained after heating the blank sample for 10 minutes for each temperature. Temperature-dependent spectra were then obtained with corresponding baseline correction.

2.2.7 Molecular dynamics (MD) simulations

All simulations were performed on atomistic models of the P1 polymer, using the GAFF force-field to describe bond, angle, dihedral, and Lennard-Jones terms[76]. The partial charges were parameterized based on density function theory (DFT) calculations of the monomer unit with ethyl substituted side-chains. The monomer was geometry optimized at the ωB97X-D/def2-TVZP level of theory[77, 78] and the electrostatic potential was calculated using the CHELPG methodology as implemented in Orca [79]. The partial charges were fit using a least-squares optimization to minimize the deviation between the monopole-based and quantum-chemically calculated electrostatic potential on the surface of the molecule. During the fit, the point charges of identical atom types were constrained to be identical. The partial charges of the side chain carbons were set to achieve charge neutrality based on the number of bonded hydrogens. Improper dihedral terms were added to all three-coordinate atoms to promote planarity using harmonic potentials centered at 0° with a force constant of 100 kcal/mol.

LAMMPS was used to perform the MD simulations [80]. All simulations used a one fs integration timestep and shrink-wrapped conditions. Electrostatics and LJ interactions were truncated at 14 Å. The initial polymer geometry was generated in an extended all-trans configuration for the backbone and side-chains. The dynamics were integrated using the Velocity-Verlet algorithm and temperature was fixed using a Langevin thermostat with 100 fs damping coefficient. The simulations were first relaxed in the NVE ensemble with restrained atomic

displacements of 0.01 Å per timestep for 10 ps, followed by 100 ps of further equilibration with the Langevin thermostat and 3 ns of production simulations. To avoid chain-folding and mimic the condensed-phase packing, a harmonic restraint was applied between the terminal hydrogen atoms on each polymer backbone with a 10 kcal/mol force constant and minima corresponding to the displacement of the terminal hydrogen atoms in the initial all-trans structure. All results and errors are reported as the average and standard deviation, respectively, of the reported quantities over five independent trajectories.

The "unconfined" simulations consisted of a pentamer of DPP-P1 (MW of ~5kD) with a single harmonic restraint on the terminal hydrogens as described above. The "confined" simulations consisted of three pentamers of P1 with individual harmonic restraints on the terminal hydrogens as described above. These simulations were initialized to avoid overlaps by aligning a single extended chain so that its long axis and π-system were maximally aligned in the x-y plane, making two replicas of this geometry, then displacing the replicas +/- 10 Å along the z-axis from the original structure. To systematically investigate π-π confinement, additional harmonic potentials were applied between subsets of the flexible dihedral atoms in each chain to restrain the chain separations and lateral registration. These restraints were grown during the equilibration phase of the simulations (from a force constant of 0 kcal/mol to 10 kcal/mol) to avoid forming kinetically-trapped structures. The confinement lengthscale in the reported results corresponds to the harmonic minima in the applied restraints. The effect of lateral registry, or slip, between the π-stacked chains was also investigated by performing simulations with restraints between subsequent pairs of flexible dihedrals. In all confined simulations the dihedral statistics of the central (confined) chain were calculated and reported. In the main text, the confined simulations

correspond to restraints of 3 Å in the π-π separation with full lateral registry between the chains. We observe qualitatively identical behavior for the slipped simulations.

2.3 Thermal stabilization of conjugated polymer thin films by blending

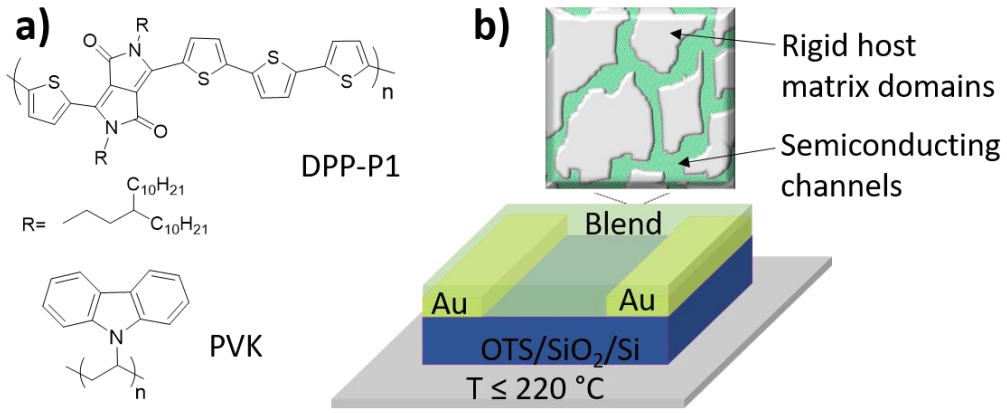


Figure 2.1 Blending strategy to beating the heat. a) Molecular structures of both the semiconducting polymer and the high-Tg insulating host used in the study of high temperature semiconducting polymer blends. b) Design rigid blend morphology where the rigid host domains are mixed with semiconducting crystalline channels to form a thermally robust blend composite. Also show is the transistor device architecture used for temperature dependent electronic measurements.

Blending semiconducting polymers with insulating hosts has been used as a general strategy to improve electronic performance, processability, mechanical and environmental stability in electronic devices. [81-83] Commodity insulating polymers such as poly-styrene (PS), poly-methyl methacrylate (PMMA) are the most commonly used for these purposes. Typically, the blending leads to the accumulation of the conjugated polymer at the interface, a strategy that has been used to improve performance as well as the environmental stability.[84-87] Given the relatively soft nature of these insulator however, these films are still subject to morphological changes. To attain high temperature stability in polymer thin films, preserving close intermolecular

interactions and packing motifs with increasing temperatures is the key challenge.[45, 57] In this chapter, we hypothesized that instead of utilizing the common low glass transition temperature matrices, for interpenetrating networks between semicrystalline conjugated polymers and high glass-transition (T_g) insulating polymer can confine conformational changes of semiconducting polymer chains at elevated temperatures. To test this concept, we first fabricated transistor devices using diketopyrrolopyrrole-thiophene (DPP-P1), a high-performance conjugated polymer, and compared its thermal stability in comparison to its blends with poly(vinyl carbazole) (PVK, T_g ~220ºC) as the high-*T*g host (Figure 2.1). We studied blends from 40 to 90 weight percentage (wt%) of PVK in spin-cast films. In situ temperature dependent measurements on fabricated field-effect transistors (FETs) under ambient air (Figure 2.2.) and inert conditions (Figure 2.3), revealed that the blends can out-perform the pristine films especially at high temperatures up to 220°C. Figure 2.2 shows the extracted temperature dependent hole mobilities revealing high performance in the blends containing as high as 40 % of the high Tg matrix in elevated temperatures ranges. As expected, the pristine film of DPP-P1 exhibit a thermally favored behavior up to 150°C, but a noticeable gradual decline takes over with increasing temperature. The mobility of the pristine DPP-P1 decreases to 8 % at 220°C. Hole mobilities as high as 2.5 cm^2/Vs at the blend ratios of 55 to 65 wt % PVK could be attained and remain stable even under extreme temperatures.

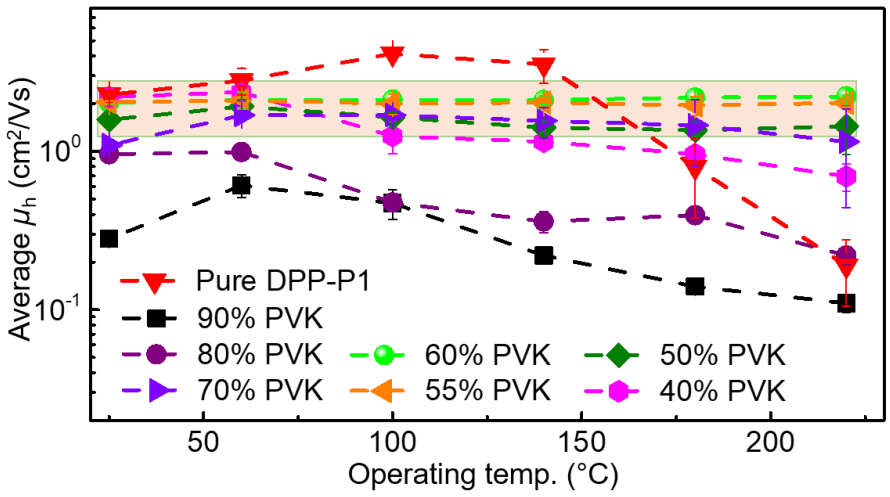


Figure 2.2. Temperature dependent hole mobility extracted from FETs with varying blend composition.

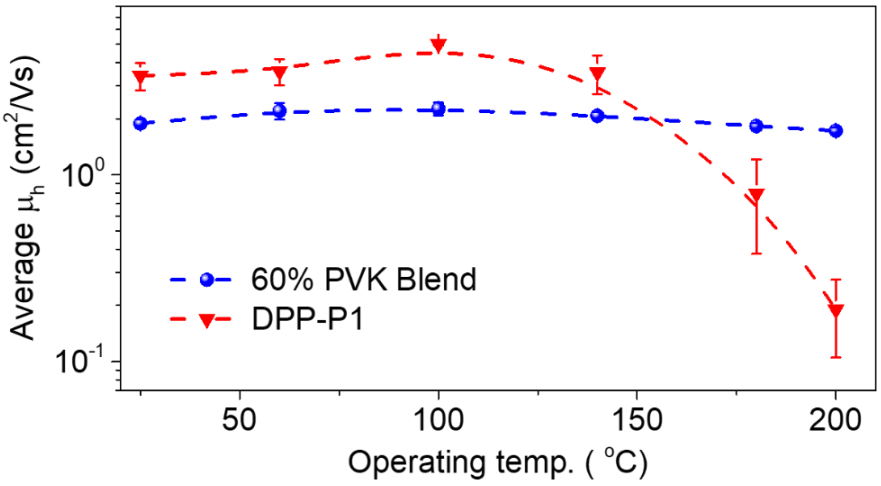


Figure 2.3. Temperature dependent hole mobility from representative transistor devices measured under a nitrogen-filled environment.

We further subjected the polymer films to constant thermal stress and test their tolerance to heat. We placed the transistor devices on a 150°C hot plate in the opened air and measured the device performance over time. In real life applications, electronic devices for high temperature

applications would have to tolerate high temperature stress for prolonged period of times either for data collection or for signal transmission. When the devices based on pristine films of DPP-P1 were brought to contact with the hot surface, the original performance dropped immediately. In contrast, the PVK blend film showed to retain the original performance even after several minutes of baking. As shown in Figure 2.4, the blend films showed to maintain nearly 100 % of the original charge mobility even after 6 hours of constant heating. Other parameters including the ON to OFF current ratio which are typically sensitive to heat could also be maintained stable in the case of the blend. This ability to retain high ON to OFF ratio would determine the lifetime of the electronic devices based on these transistors. As shown in Figure 2.5, stable transfer characteristics are observed in the blend film while the current stability begins to worsen after 1 hour of heating in the pristine film. These unstable currents are typically the main cause of junction leakages, loss of amplification, and increased power consumption in high temperature electronics.[42] The blend films showed excellent thermal tolerance and proved to be excellent candidates for the manufacturing of high temperature organic electronics.

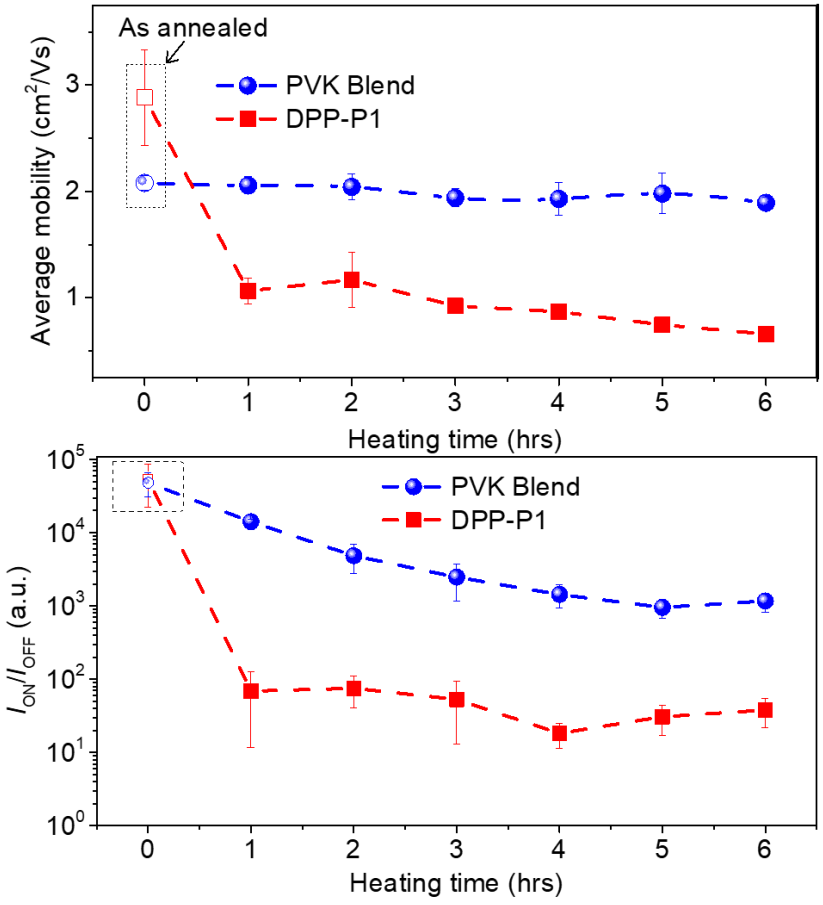


Figure 2.4. Transistor behavior under constant thermal stress. After six hours of thermal stress, stable transistor performance is retained in the blend films.

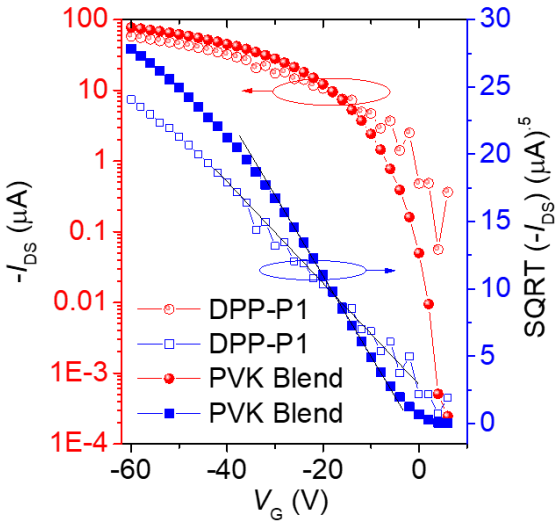


Figure 2.5. Characteristic transistor curve after 1 hour of thermal stress at 150°C comparing the thermal stability of the studied blend film to the pristine film.

2.4 Rationalizing high temperature operation stability in polymer blends

2.4.1 Impact of blending on morphology

The miscibility between the two blending composites was envisioned to be important for the observed thermal stability. Without the interaction between the components the following would occur: i) either the blend films phase separates vertically or ii) the two polymers form large domains laterally separated. In the first scenario, the transistor performance would be achievable on one interface, but the blend would behave similarly to the pristine film. The latter scenario would lead to poor charge transfer since the domain isolation would prevent efficient hoping of the carrier in the transistor devices. We then characterized the blend morphology to not only visualize the degree on miscibility in our films, but to also understand why only a narrow blending percentage shows excellent stability in comparison to others. The AFM height images revealed that the conjugated polymer formed nanoscale domains that showed to increase in connectivity

with increase semiconductor amount, and plateau around 55% of the semiconductor added (Figure 2.6). We then delaminated the film and imaged the bottom interface to find that interconnectivity nature persists on both sides of the thin film as shown in the AFM images in Figure 2.7. We could thus conclude that in our blends, we do not have a complete vertical nor a large lateral phase in accordance to the efficient electronic performance observed in the transistor devices. The two components form an interpenetrating network of the semiconducting domains surrounded by the insulating matrix. This close housing of the semiconducting domains by the rigid insulator could thus explain the observed thermal stability.

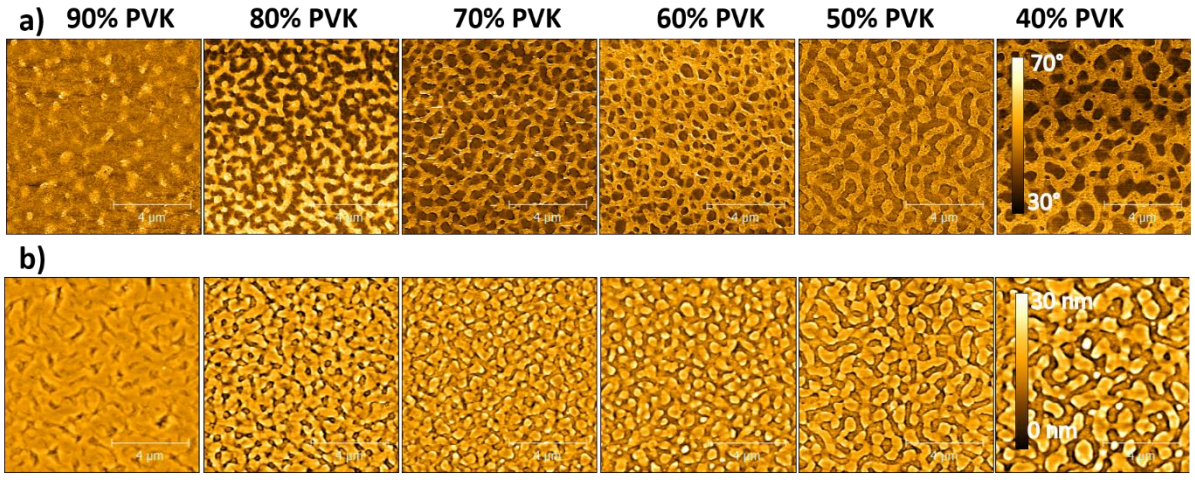


Figure 2.6. Morphology evolution with varying content of the insulating matrix. With optimal blending ratio, interpenetrating network of the crystalline conjugated polymer domains is formed surrounded by the host matrix.

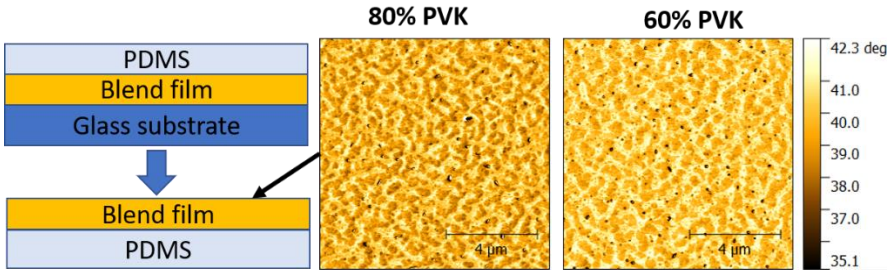


Figure 2.7. Morphology of the bottom interface revealing interconnected domains of the conjugated polymer analogous the top face morphology.

To probe the impact of temperature on the formed morphology, we subjected the blend films to extreme heat (220^{o}C) and monitored any morphological changes in comparison to the pristine DPP-P1 film. The AFM height images revealed that the blend film morphology remains unchanged even after thermal treatment near the Tg of the matrix for 1 hour (Figure 2.8). The pristine conjugated polymer film treated in the same conditions exhibited detectable variations in the domains' sizes. This thermal robustness of the blend morphology could thus support the stable performance observed in transistor devices. This robustness was observed for the pristine PVK film. When heated 220^{o}C, the matrix itself also revealed a stable morphology indicative of an excellent candidate as a rigid host in the blend film. Up to this point, it was understood that the matrix polymer brings the overall rigidity to the film while the semiconductor provides the electronic properties. The embrace of the two features in a mixed manner yields thermally stable electronic performance in transistor devices.

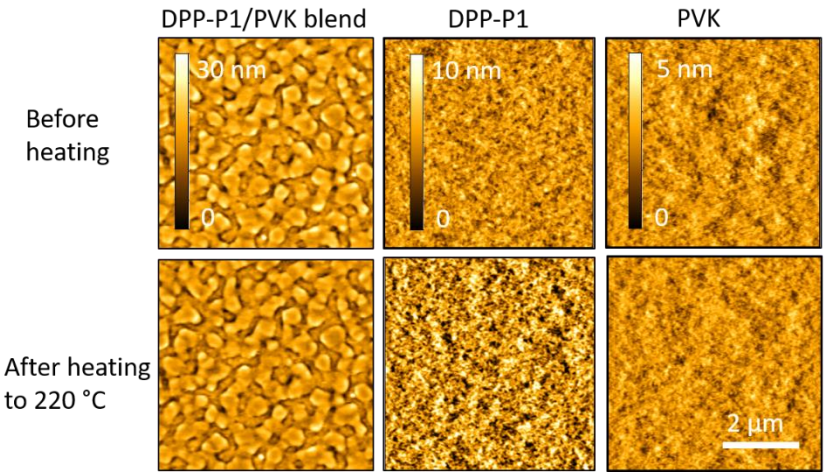


Figure 2.8. Effect of thermal stressing on thin film morphology. The blend film as well as the pristine matrix film show no changes after heating while the pristine conjugated polymer film reveals slight changes in the domain sizes.

2.4.2 Impact of blending on ordering and packing

To further understand the origin of the blending-induced thermal stability, we also carried out a series of studies on parameters that would impact the charge transport besides the microscale morphology. We wanted to probe the effect of blending on the semiconducting polymer especially in terms of ordering, a key feature towards improved electronic behavior. As suggested from the morphology analysis, the blending induces the aggregation of the conjugated polymer domains into a network of crystalline domains that are confined by the matrix polymer. At this stage we understand that the interconnectivity is key to reaching efficient charge delocalization within the blend films and that the confinement by the rigid host is the contributor to the stable morphology at high temperature, hence the stable charge transport in harsh thermal environments. We are however interested in probing the thermal stabilization much deeper especially within the conjugated polymer domains. We predicted that the absorption profiles as well as the crystallographic features of the DPP polymer chains would reveal the impact of blending on their ordering behavior both with and without the thermal stress.

2.4.2.1 UV-Vis spectroscopy

Since the blend formation showed to yield films morphologies drastically different from that of the pristine conjugated polymer films, we examined the UV-Vis absorption spectra and their relevant signatures on the observed thermal stability for the blend films. Figure 2.9 shows normalized absorption spectra of the blend films with varying blend content. In the presence of PVK we observe the following: 1) a slight red-shift in the absorption spectrum indicative of induced aggregation as revealed by the AFM images. 2) An increase in the *0-0* vibronic peak intensities signature of improved chain planarization and interchain stacking. Both features showed to not benefit significantly from further increase in the amount of the semiconductor beyond 40 % which suggested that there exists a threshold blend ratio at which the morphology is optimized. The first feature was not surprising since from the AFM images we observe the formation of DPP-P1 aggregates into a network which would explain the observed red-shifting in the spectra. This behavior is also common in other blending systems that use insulating matrices.[84-87] Furthermore, the red-shift showed to plateau, just as the domain connectivity showed to begin to disrupt beyond 50 % of the fully conjugated polymer present. The second feature was less obvious from the morphology results. From the aggregation behavior, we would expect that the semiconducting polymer chains would form bundle inside the aggregates. Instead, we observe that the presence of PVK leads to a disentanglement of the DPP-P1 chains and improves their ordering. According to previous works on signature absorption spectra in polymer films, the increase in the *0-0/0-1* vibronic peak ratio is indicative of chain planarization and improved stacking.[88] This feature will greatly benefit the efficient charge transport in our blends especially since we have a minority percentage of the semiconductor.[85, 88, 89] Coincidently to the electronic measurement results, both these features showed to be optimal for the blend ratios that revealed both high performance as well as excellent thermal stability.

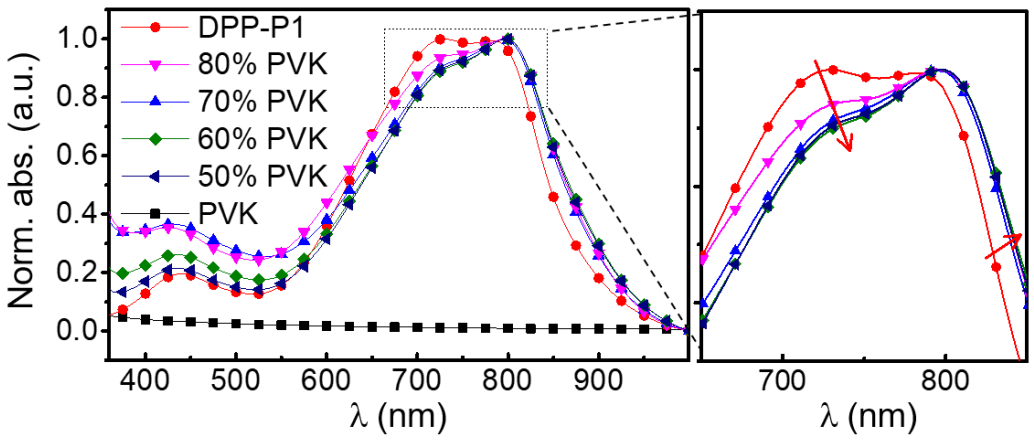


Figure 2.9. Effect of blending on ordering. Normalized absorption spectra from DPP-p1 films when blended with different contents of PVK.

Given the hinted blending-induced ordering, we further carried out in-situ temperature dependent UV-Vis measurements to probe the blend stability. The annealed films on glass substrates were subjected to temperature increase and monitored were the changes in the signature vibronic peaks comparing the blend film (60 % PVK as a representative) to the pristine DPP-P1 film. For DPP-P1 films, the vibronic peaks showed to both blue-shift and decrease in intensity with increasing temperature (Figure 2.10). At 220°C, the maximum absorption peak that is associated to the inter-chain stacking was no longer detectable. This indicates that the ordering was nearly lost in the pristine film at such high temperature in accordance to previous reports.[57] In contrast, the blend film which began with much improved ordering between polymer chains, relatively higher ordering could be retained at all temperatures. At 220°C the strong *0-0* vibronic peak could still be observed as evidence of persistent ordering in the blends. This observation came to support the stable morphology as well as the stable electronic performance that we discussed in sections above. From these in-situ studies we could thus gain a better understanding on the role played by the blending approach: the insulator induces molecular ordering in the aggregated domains, rigidifies the microscale morphology, and thus minimizes disordering with increasing

temperatures. UV-Vis absorptions which captures a large sample scale while accounting for both the crystalline and amorphous domains within the film was a great indicator of this thermal stabilization. To compliment these results, we further probed the crystalline domains of the conjugated polymer using x-ray crystallography.

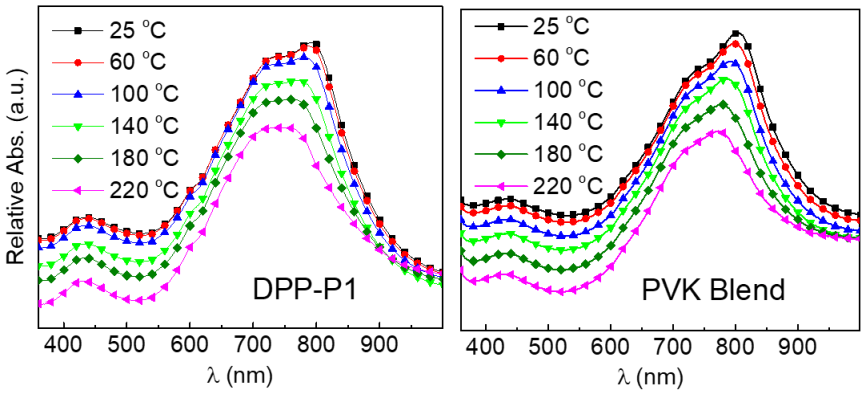


Figure 2.10. Temperature dependent absorption spectra of the pristine DPP-P1 film compared to the blend film containing 60 % of PVK.

2.4.2.2 X-ray crystallography

Since charge transfer processes in polymer films are understood to occur both along the polymer backbone and between the crystalline domains, we wanted to gain further insights on the influence of blending on crystallization of our conjugated polymer and the resulting thermal tolerance. We thus performed in-situ temperature-dependent x-ray diffraction studies on the pristine polymer and compared the DPP-P1 behavior to that of the corresponding PVK blend (Figure 2.11 and 2.12). As hinted by the UV-Vis absorption spectra and morphology results, we observed that the blending induced an improved packing for the DPP-P1 domains leading to closer π-π stacking distances (Figure 2.12). Upon blending the π-π packing distance shortened from 3.70 Å to 3.63 Å. This shortening could be explained by the observed ordering, planarization, and aggregation discussed above. The temperature-dependent results revealed that this improved

packing also persists when the diffraction patterns are collected up to 200°C. In agreement with the induced ordering observed from the absorption spectra, the crystalline domains of the blend films show to remain ordered at all studied temperatures. With the increase in heat, the lattice shows to expand, but in the blend films the expansion proved to be much slower than that of the pristine DPP-P1 film. At 200°C, the blend film could retain the inter-chain π-π stacking distances of around 3.73 Å while the pristine DPP-P1 film showed to expand up to 3.8 Å (Figure 2.12). This efficient stacking at elevated temperatures could thus support the observed high performance in the transistor devices and supports why the blend films showed to outperform the pristine ones at elevated temperatures.

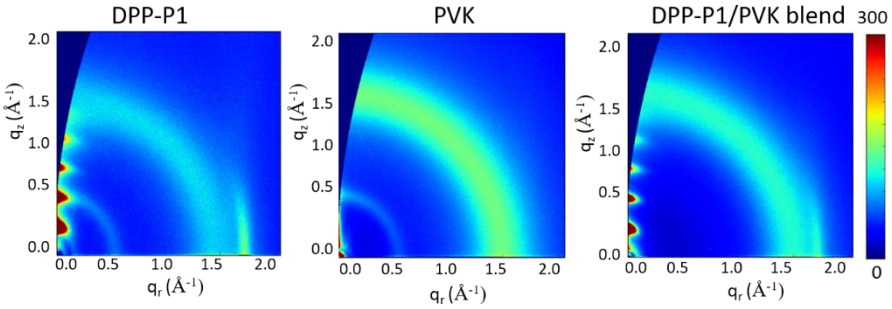


Figure 2.11. Diffraction patterns of DPP-P1 and corresponding PVK blend. The blend shows to inherit the π-π stacking nature of the conjugated polymer while retaining the amorphous domains of the insulator.

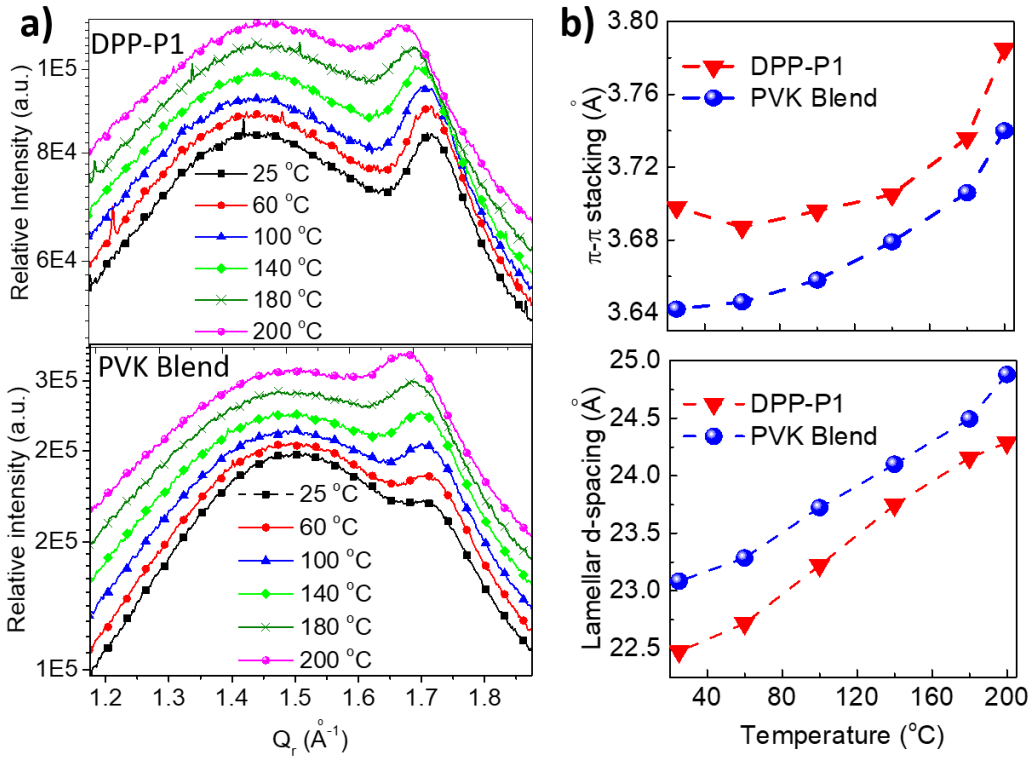


Figure 2.12. In-situ temperature dependent diffraction analysis. a) In-plane line profile obtained from the 2-D diffraction patterns of DPP-P1 and its PVK blend at different temperatures. b) Extracted π-π stacking distances as well as the lamellar d-spacing of the films studied with increasing temperature.

These diffraction behaviors of the blend films were thus both encouraging and inciting. Our discussion above had focused on the fact that the presence of the matrix polymer merely brings the confining effect to the conjugated polymer domains and restricts the disordering upon heating. It evidenced from both the UV-Vis absorption and crystallography results that the matrix polymer is responsible for more than the microscale ordering; induces the molecular ordering. The blend-induced chains aggregation is concomitant to their planarization which leads to closer π-π packing. This intricate combination of features that are beneficial to charge delocalization is thus believed to be at the heart of the observed thermally stable charge transport at high temperatures. The positive contributors at high temperature are now understood to be i) the thermal activation of

carriers, ii) stable microscale morphology, iii) retained ordering and efficient chain packing which are being counteracted by the a) the lattice thermal expansion, b) the excessive increase in carriers' density, as well as c) environmental factors. One could argue that the opportune combination of these factors could yield a thermally insensitive charge transport behavior. This agrees with the recently proposed model that we briefly discussed above, i.e. a generalized Einstein relation in which the marriage of degree of delocalization and density of states is predicted to yield a temperature independent charge mobility.[36] We believe that in our blend system, these compete factors are the main contributors to the mobility linearity that we observe within our studied temperature ranges. We now turn to theoretical analysis to predictively rationalize our observation and, in retrospect, establish the design principles for the blending approach.

2.5 Molecular dynamics simulations

With all the experimental evidence directing towards the improved ordering and close packing upon blending, we now seek a theoretical understanding through molecular dynamics simulations. We believe that the induced chain planarity and closer packing is one of the key elements towards the observed stable charge transport at elevated temperatures. With the chains closely packed, their degree of freedom for rearrangement, twisting, and vibrations is expected to be minimized enabling efficient charge transport at high temperature. As discussed in the introductory chapter, disordering is the major factor to declining performances in organic systems under thermal stress. In the case of conjugated polymer, the main form of disordering is the backbone torsional variations. The torsional and orientational variations between neighboring chain segments will lead to both ineffective charge delocalization within the channel and the formation of dead-ends along the polymer chains. We believe that at high temperature, though the carriers are now given enough energy for delocalization, this thermal activation is concomitant to

more degrees of distorting and reorienting. The semiconducting system would only benefit from the thermal activation if it can maintain its ordering at the same time. We thus believe that the confinement induced by our blending approach in the aiding the ordering of semiconducting component, thus helping the blend film maintain improved thermally stable charge transport.

To evaluate the effect of this π-π stacking confinement on the polymer dihedral distribution molecular dynamics modeling was performed on a pentamer of DPP-P1 (Figure 2.13) as described above with the atomic assignments shown below. We chose five repeat units as the representative length which is reasonably long enough to depict the chains within the π-π stacks but also short enough for reasonable computational times. Here we aim to evaluate the effect of confining the polymer chains on their degree of disordering under thermal stress. As illustrated in Figure 2.13, we hypothesize that once the polymer chains are tightly packed together, the thermal stress will have minimal effect on their ordering. We hypothesize that the effect from the neighboring chains within the stacks will lower the degree of freedom for rational and torsional disordering. To test this hypothesis, the pentamer will them be simulated by varying the degree of confinement and analyzing the thermal response given the spatial restrictions.

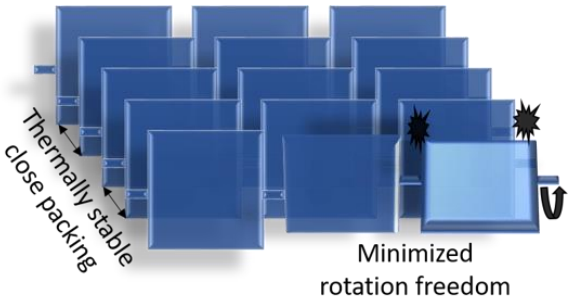


Figure 2.13. Illustration of the impact of close packing of conjugated polymers chains on their degree of torsional disordering.

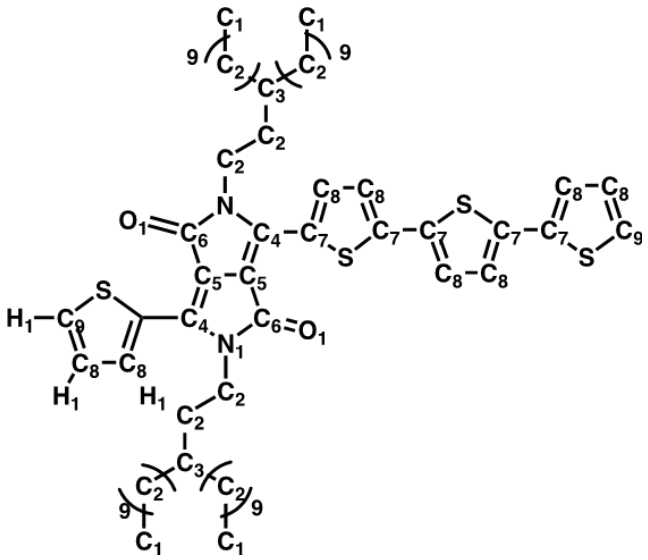


Figure 2.14. Atom type assignment for the partial charges used in the molecular dynamics simulations.

Table 2.3. Summarized partial charges of each atom type parameterized based on ωB97X-D/def2-TVZP calculations of the minimized geometry.

Atom Type	**Partial**
C1	-0.439660
C2	-0.298968
C3	-0.149484
C4	0.039690
C5	0.111411
C6	0.038846
C7	-0.007710
C8	-0.157400
C9	-0.144707
O1	-0.311233
N1	0.000374
S1	0.036663
H1	0.149484

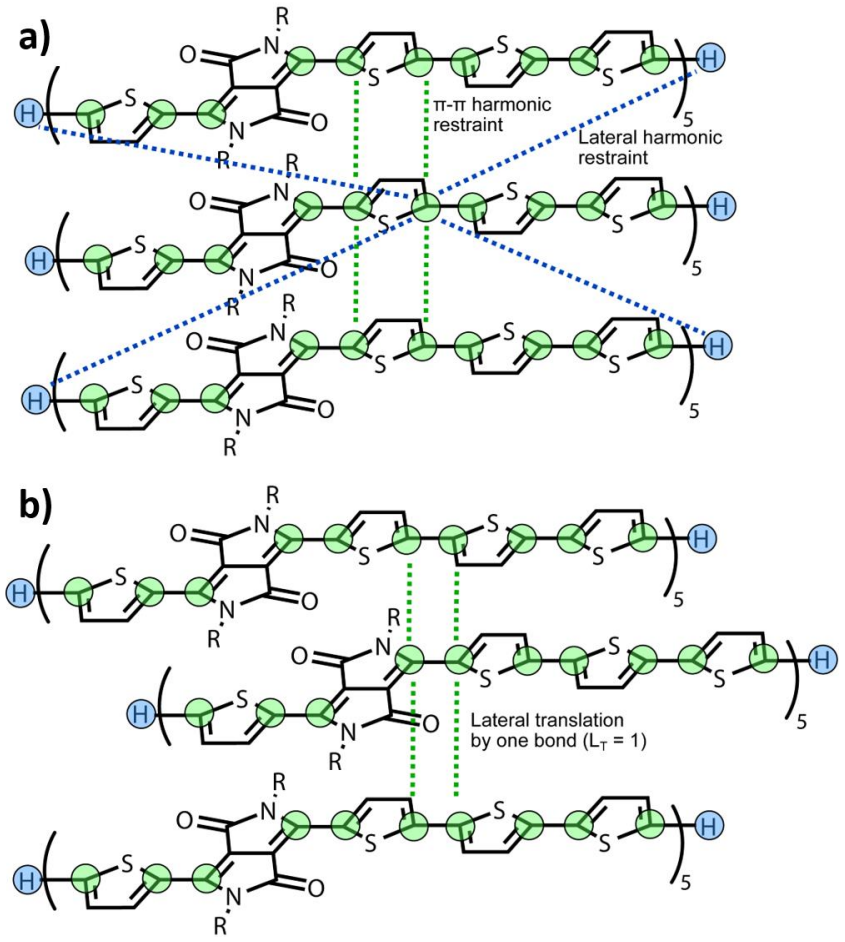


Figure 2.15. Description of the restraints used to confine polymers during the MD simulations. A) Atoms show in green correspond to the 1-2 atoms in flexible dihedrals. Harmonic restraints were used between identical atoms on each chain to maintain a prescribed separation (green-dotted), while lateral restraints were used (blue-dotted) between the terminal hydrogens and the backbone atoms of the central chain to avoid slip. B) Definition of lateral translation unit (L_T) whereby the π-π constraints are shifted by L_T bond(s) to simulate slipped configurations.

In these simulations, the π-π separation of the semiconducting polymer chains were restrained to model varying levels of confinement (as illustrated by the green dots in Figure 2.15), and the resulting dihedral distributions were compared to characterize the polymer reorganization dynamics at different temperatures. To mirror the x-ray diffraction results, the confinement distances were varied from 3.0 Å up to 6.0 Å. As detailed in the experimental section, the simulations also accounted for the slipped configurations by adding a lateral translation restrains

as shown in Figure 2.15. The translations were varied from no slip ($L_T = 0$) to a four shift ($L_T = 4$); Figure 2.15 b) shows and example of a lateral translation of one bond. The molecular dynamics results for all studied temperatures, lateral translational restraints, as well as the π-π separations are summarized in Figures 2.16 and 2.17. The results showed that when the π-π confinements were restricted to 3.0 Å, complete conservation of the dihedral distributions at all temperatures could be observed. Notably, the CCCN dihedral, corresponding to the diketopyrrolopyrrole-thiophene (DPP-T) conformations, exhibited interconversion between gauche conformers, but there was no evidence of gauche to trans interconversion (i.e., the onset of chain twisting) at any temperature. Likewise, the SCCC dihedral angle, corresponding to the thiophene-thiophene conformations, broadened with temperature but remained sharply peaked. In contrast, at longer π-π confinements (> 5.0 Å), the SCCC dihedral distribution is broadened at all temperatures and the CCCN dihedral begins to exhibit gauche to trans interconversion at temperatures of 700 K (425°C). These systematic studies of the dihedral distributions under confinements from 3 Å to 6 Å allowed us to conclude that large-scale DPP-T reorganizations began relatively abruptly once fluctuations in the interchain π-π separation reach ~5 Å.

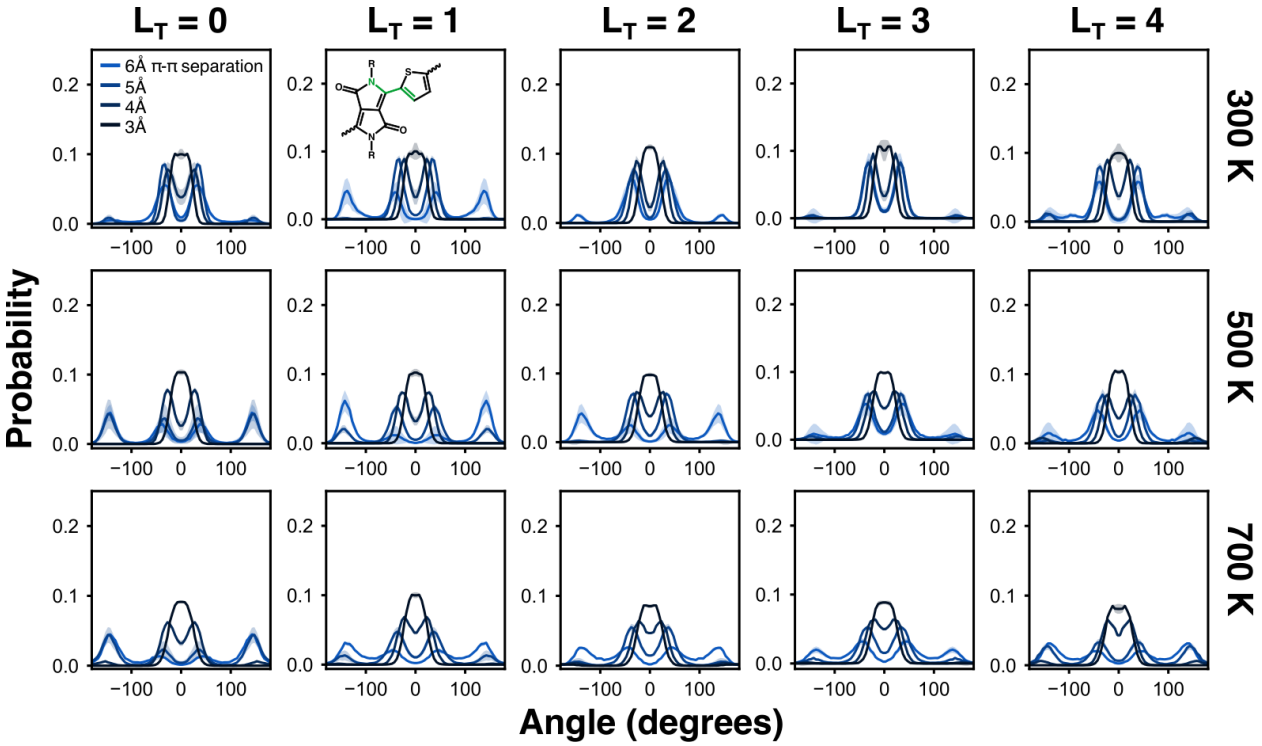


Figure 2.16. A systematic investigation of the dihedral distributions for the CCCN dihedral in DDP-P1 (inset) under varying levels of confinement (color), temperature (row), and lateral displacement of the chains (column).

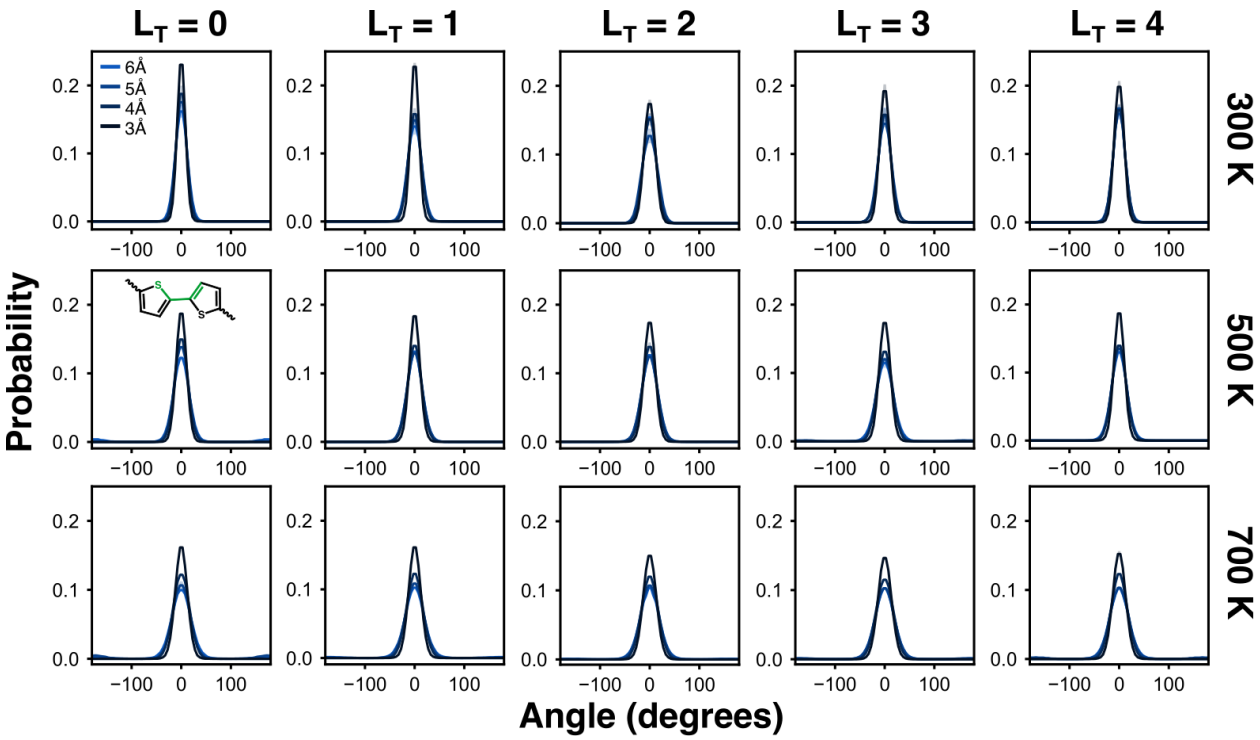


Figure 2.17. A systematic investigation of the dihedral distributions for the SCCC dihedral in DPP-P1 (inset) under varying levels of confinement (color), temperature (row), and lateral displacement of the chains (column).

These computational results thus indicated that the torsional freedom of the DPP chains is indeed dependent on the stacking distance between neighbors. This was in good agreement with our hypothesis that the induced close packing by the blend confinement effect minimizes the degree of freedom for the polymer chains to undergo disordering. In fact, as we had illustrated in Figure 2.13, when we captured a snapshot from the simulated pentamer, we could see that with close the π-π confinements (3 Å), the chains remained tightly packed at high temperature (425°C) while the larger separations (5 Å) allowed both the backbone and the sidechains to adopt random orientations. The screenshot is shown in Figure 2.18 when the chains where subjected to high temperature with varied confinement levels. These simulation results thus served as a guideline to deduce that if we can improve the packing within our films, maintain the ordering amongst the semiconducting stacks, we would be able to conserve the fastest charge transfer pathway (polymer

main chain) by reducing the torsional disorder even at elevated temperatures. With this guideline in mind, this spatial confinement approach would be a general strategy for stabilizing charge transport at high temperatures either by spatial templating or choosing other high Tg matrices.

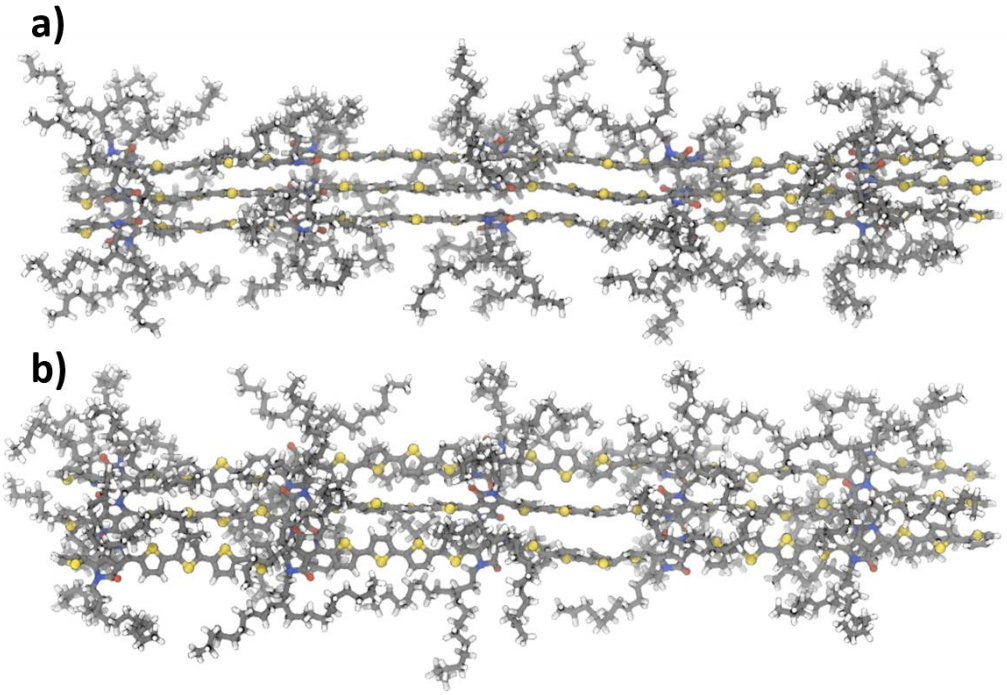


Figure 2.18. Screenshot from the MD simulations of the pentamer chains at 425°C with no lateral translation when the confinement is varied from a) 3 Å and b) 5 Å. The more confined chains show to remain ordered with planar backbones while the less confined ones exhibit more torsion and even folding along the polymer chains. The atoms are labelled as grey (C atoms), white (H atoms), yellow (S) atoms, blue (N atoms), and red (O atoms) for clarity.

2.6 Generalization of the blending approach

Since it was understood that once we can confine the semiconducting polymer domains within a rigid host, thermally resistant charge transport behavior could be attained, we proceeded to investigate the generality of this approach. Though the effect from blending is sought out to be more a spatial confinement than a molecular interaction, instead of using other methods generally used for spatial confinement such as templates formation,[90, 91] he we aim to prove the blending

generality as a much simpler approach. To do so, two questions ought to be addressed: 1) Would any insulating host matrix work given it possesses a glass transition temperature high enough to remain rigid within the studied thermal range? 2) Would our blending approach work for any semiconducting polymer? We then investigated these aspects by selecting a wide library of high Tg insulators and form blends with the conjugated polymer and by selecting other building blocks for the semiconducting polymer and test the stability of the resulting blends.

2.6.1 Host matrix generality and scope

First, we selected four additional high Tg insulators to demonstrate the generality of our blending strategy. We explored the FET thermal stability of DPP-P1 blended with these insulators as shown in Figure 2.19. The Tg was chosen to be near that of PVK which was used for the proof of concept. Poly-acenaphthylene, [92] an insulator that is structurally close to PVK could afford a Tg as high as 265°C. To reach even higher rigidities, we select polyetherimide (PEI) which has a Tg of 263°C and Matrimid® 5218 (MI) with a glass transition temperature beyond 320°C. We also selected polymethyl methacrylate (PMMA, Tg 109°C) and polycarbonate (PC, Tg 180 °C) to probe what would happen if we carry out the measurement above the Tg of the insulator. To ensure the mixing and the formation of the interpenetrating network morphology, we first tuned the blending ratios for each pair to attain the nano-concrete-like morphologies (Figure 2.20). We then fabricated FET devices like the ones using PVK and the matrix host. The devices based on these optimized blends exhibited hole mobilities as high as 2.0 cm^2/Vs that were stable up to 220°C in open air (Figure 2.21) proving that our blending approach is a general method, apart from PMMA and PC-based blends. For instance, the optimized blend of DPP-P1 and PC (T_g ~182^{o}C) only provided thermally-stable operation up to 180^{o}C, which is near the T_g of the host. This indicated that the thermal operation stability relies of the rigidity of the host matrix. Once the matrix begins

to soften, nano-scale morphology fluctuations will begin to deteriorate the ordering in the films and the charge transport properties with be negatively impacted.

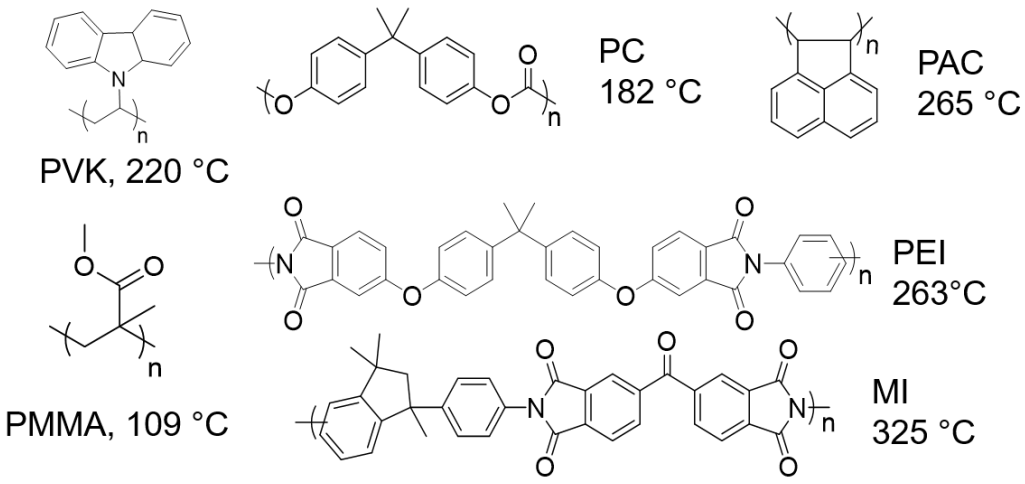


Figure 2.19. High glass transition temperature matrices. Molecular structures of the selected high Tg matrices studied for high temperature stability in semiconducting polymer blends. Also shown are the corresponding glass transition temperatures.

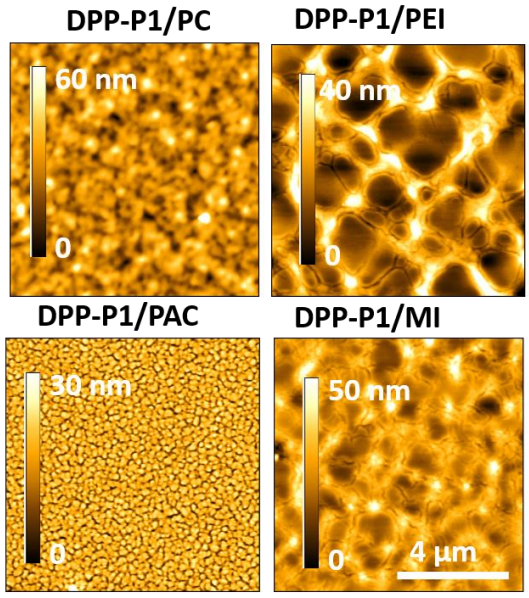


Figure 2.20. Blending universality in DPP-P1. AFM height images of DPP-P1 blended with various high Tg matrices.

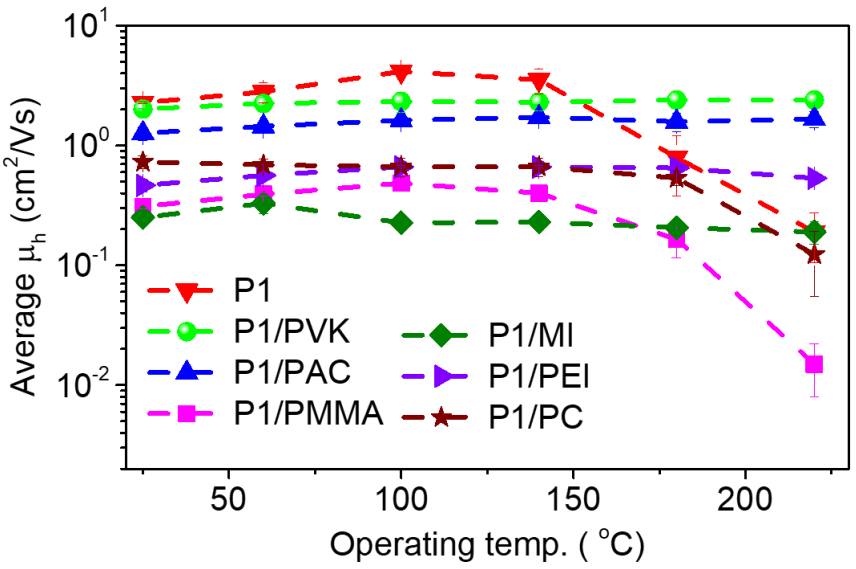


Figure 2.21. Blending generality in DPP-P1 films. Temperature dependent hole mobilities extracted from transistor devices of DPP-P1 when blended with different high Tg matrices.

To probe the effect of the matrix softening on the blend morphology, we carried out in-situ temperature dependent AFM imaging. Since the thermal limit of the Asylum AFM instrument was 120°C, we selected the PMMA-based blends to image the blend morphology above the Tg of the matrix. The pristine DPP-P1/PMMA films first exhibited a uniformly interconnecting morphology as shown in Figure 2.22. We then heated the film to 120°C and reimaged its morphology to find that the fibral structure was thermally disrupted forming expanded and flat features. We could rationalize such drastic morphology change to the fact we significantly exceeded the glass transition of the rigidifying component. We also concluded that such major morphology instability was the root of the unstable transistor performance in PMMA blends as shown in Figure 2.21. As we mentioned above, the same behavior was observed in PC blends (Tg 180°C) when the devices were heated to 200°C and higher. These observations thus suggested that in order to realize the thermal stability, we ought to select a matrix who Tg is significantly higher than the operating temperature.

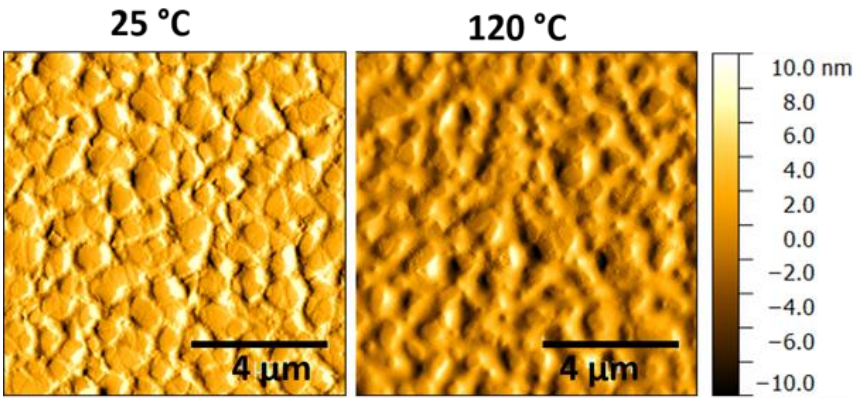


Figure 2.22. Limitations of the rigidification abilities of the blending conception. AFM height images of DPP-P1/PMMA films revealing morphology changes when scanned below and well above the glass transition temperature of the matrix.

From the studied blend pairs, we thus observed the following: i) PVK and PAC blends offered the highest electronic performance most likely because these hydrocarbon-based matrices do not contain any functional groups that will function as charge trapping sites. ii) MI and PEI blend pairs offered the lowest starting electronic performance most likely owing to the discussed charge trapping. iii) Even though the Tg of the matrix could be increased beyond 300°C, the electronic properties were found to start decline above 220°C. We explained this behavior by the fact that though the host matrix might minimize large morphology changes, the lattice expansion still occurs especially among the π stacks of the conjugated polymer. Beyond a certain degree of heating, effective charge transport becomes impossible. We envision further investigation would establish the turning point for this behavior to determine the thermal limitation of the blending strategy.

In accordance to the AFM, UV-Vis, and x-ray crystallography results, once our blends can an interpenetrating network between the conjugated polymer and the rigid host, the thermal stability of the thin-film transistor devices could be improved. We observed that as long as the operation temperature does not significantly exceed the Tg of the matrix, in which case its

confining abilities will be lost, thermally stable operation can be realized. As a generalized rule, it can be concluded that to make thermally stable organic transistors one ought to choose a conjugated polymer, mix it with a high Tg host matrix, text their morphology to ensure the semiconducting network formation, and operate below the Tg of the insulator. However, as we discussed above, the chemical structure of the insulator showed to have an impact of the performance which warrants further investigation on what functional groups are detrimental to charge transport; we will revisit this concept in later chapters. Also, to be considered are the limitations of the conjugated polymer itself, thermally, since though the Tg of the host matrix could be increased up to 320°C, the charge transport properties seemed to begin to exhibit a negative slope above 220°C. This behavior though beyond the scope of the current discussion would be of great interest in terms the limits of semiconducting properties in confined spaces given that the conjugated polymer is not decomposed or degraded structurally.

2.6.2 Semiconductor generality and scope

Whether the blending approach could be extended onto other semiconductors besides DPP-P1 was of great interest to us to prove the blend generalization. We then tested other commonly studied high-performance diketopyrrolopyrrole (DPP-P2)[89] and isoindigo (Is-P1)[93] based donor-acceptor semiconductors (Figure 2.23), and studied the thermal stability of their blend films with the champion high-Tg matrices, i.e. PVK and PAC. To ensure the aggregation and ordering as it was the case for DPP-P1 blends, we tested the UV-Vis absorptions and imaged the morphologies of the blend films with varying blend ratios. After optimizing the blend ratios to obtain an interpenetrating morphology (Figure 2.24). We then fabricated FET devices using the blends in the same manner as previously described. The transistor devices showed excellent electronic properties as well as excellent thermal stability up to 220°C especially for Is-P1-based blends

(Figure 2.25). Surprisingly, Is-P1 on its own showed to be more heat tolerant than the other two studied polymers. Furthermore, the blend pair of DPP-P2/PVK showed poorer stability compared to the PAC analogue.

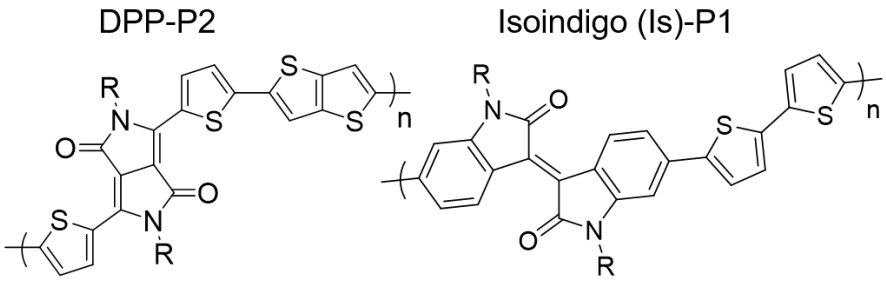


Figure 2.23. Blending universality. Molecular structure of additional semiconducting building blocks studied for high temperature thermal stability.

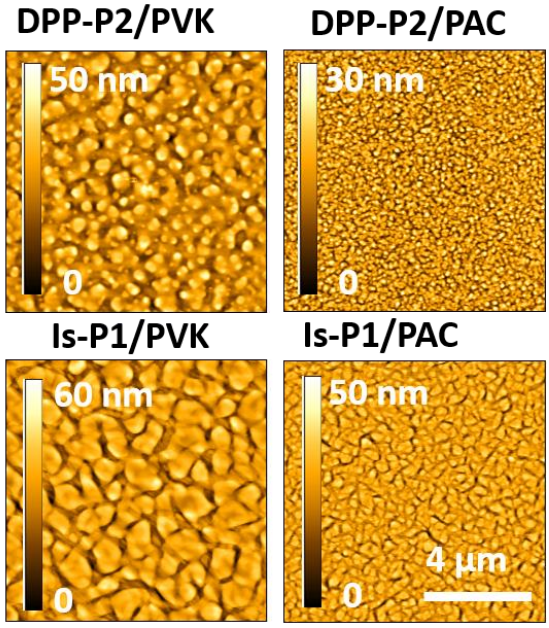


Figure 2.24. AFM height images revealing the formation of an interpenetrating morphology between the DPP-P2 and Is-P1 and the representative insulating matrices.

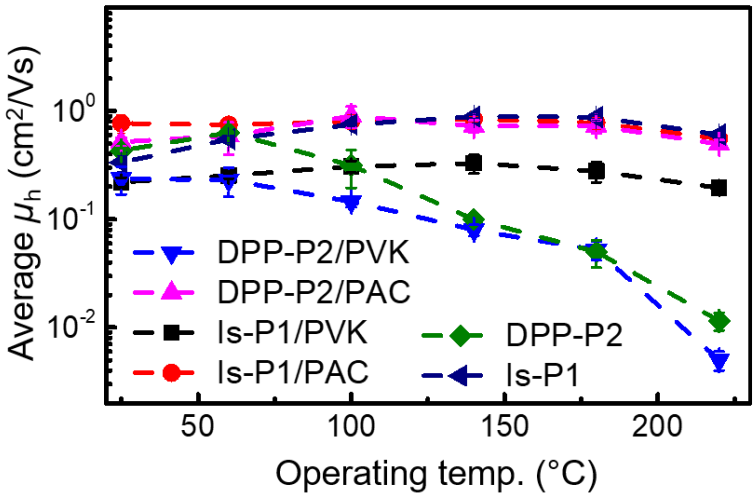


Figure 2.25. Temperature dependent hole mobility extracted from transistor device made from DPP-P2 and Is-P1 blends.

To rationalize these observed differences in electronic behavior, we once again resolved to temperature-dependent UV-Vis absorption analyses on the blend films of both the pristine polymers as well as the corresponding blends. From the absorption spectra we observed the following: i) DPP-P2 has a weak absorption signature of π stacks ordering and main chain planarization as we described above. Its maximum absorption peak around 820 nm showed to be relatively weak and to significantly decline upon heating (Figure 2.26). This loss in ordering at high temperatures would explain the poor thermal tolerance as shown above (Figure 2.25). In addition, this ordering showed to not greatly benefit form blending with PVK as it did for PAC. The maximum absorption showed a significant decline with increasing temperature in the case of PVK while PAC blends showed to preserve this peak even at 220°C. We believe this less pronounced ordering in DPP-P2/PVK blends were the cause of the lesser thermal tolerance observed in the corresponding FET devices. Besides, as it could be seen in the AFM images above, the PVK blend pair showed poorer miscibility in comparison to the PAC analogue. ii) Is-P1 on its own has a strong absorption peak around 720 nm associated with the π stacks ordering and main

chain planarization. This ordering was also found to be retained even at high temperatures (Figure 2.27). In agreement to the results obtained from the DPP-P1 blends, this ordering again showed to be a key factor towards high temperature operation stability. The pristine films of Is-P1 showed to withstand the heat relatively well which hints that with proper choice of the semiconducting backbone, thermal stability might attainable in pure polymers. iii) Consistent with our blending approach, the Is-P1/PVK and PAC blends showed to improve the ordering in the films and showed to yield thermal stable transistor devices.

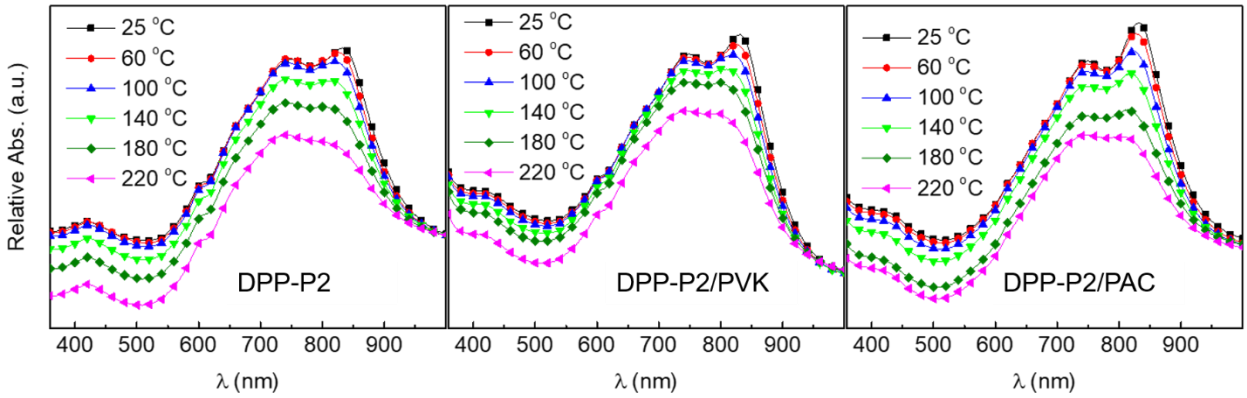


Figure 2.26. Normalized absorption spectra of DPP-P2 and its blends with the studied matrices.

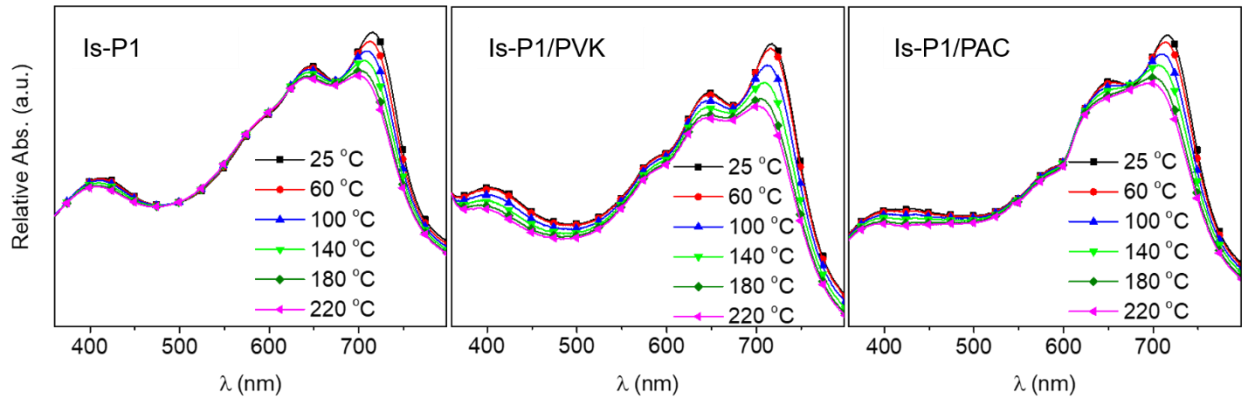


Figure 2.27. Normalized absorption spectra of Is-P1 and its blends with the studied matrices.

Lastly, we wanted to test the blending concept on n-type polymers, i.e. electron transporting conjugated polymers. In this regard, since n-type polymers are typically known to have poor stability in open air,[94, 95] our discussion was not intended to improve such stability. Instead we selected conjugated polymer systems that have shown to exhibit relatively stable charge transport in ambient conditions[96-100] and probed how our blending approach improves the thermal stability by comparing the pristine polymer film to the blend film. Also, since n-type performance is known to be tuned by the selection of the metal contacts and or surface modifications, in the current investigation, we selected to fabricate the transistor devices in the same manner as the p-type polymers and simply compared the thermal response of the devices based on the pure polymer versus the blend. We thus selected a BDOPV-based polymer with the molecular structure shown in Figure 2.28 and blended it with PVK and PAC as the host matrices.

We then fabricated the transistor devices as previously described and measured the resulting performances at ambient. We could successfully measure the electron transport at room temperature both from the pristine polymer film as well as the corresponding blend films as shown in Figure 2.29. However, when the films were treated to high temperatures, as high as 200°C, the devices based on the pristine films exhibit to become extremely unstable and the current becomes nearly undetectable. On the contrary, the blend films treated to the same conditions show to remain operational. We thus believe that superior stability observed in the blends was due to the improved ordering that we discussed above which suggests that our blending concept is essentially a general strategy for realizing thermally tolerant transistors, both n-type and p-type.

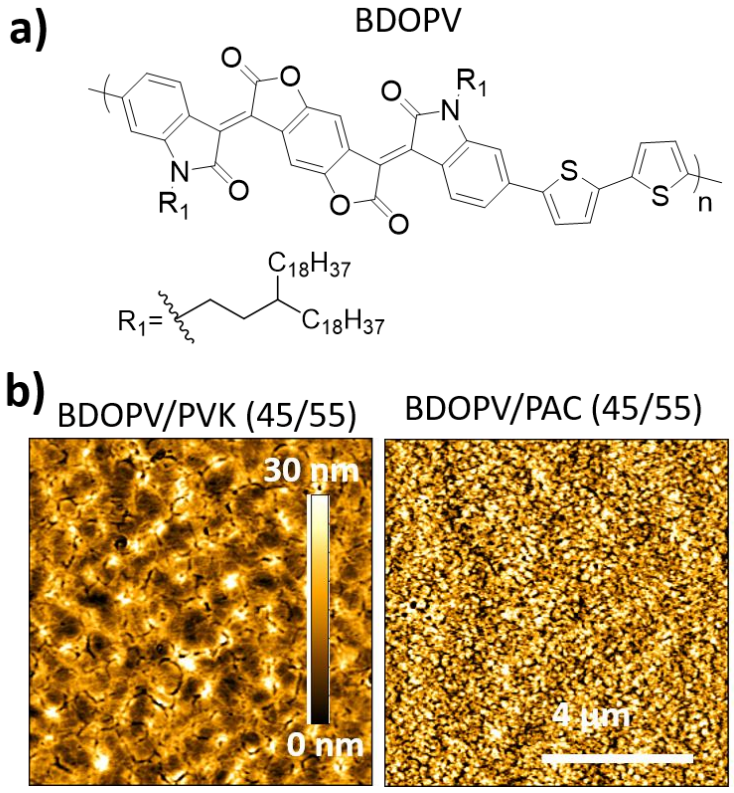


Figure 2.28. Thermal stabilization of n-type charge transport. a) Molecular structure of BDOPV based polymer. b) AFM height images showing the morphology of the blends of BDOPV polymer with the representative matrices.

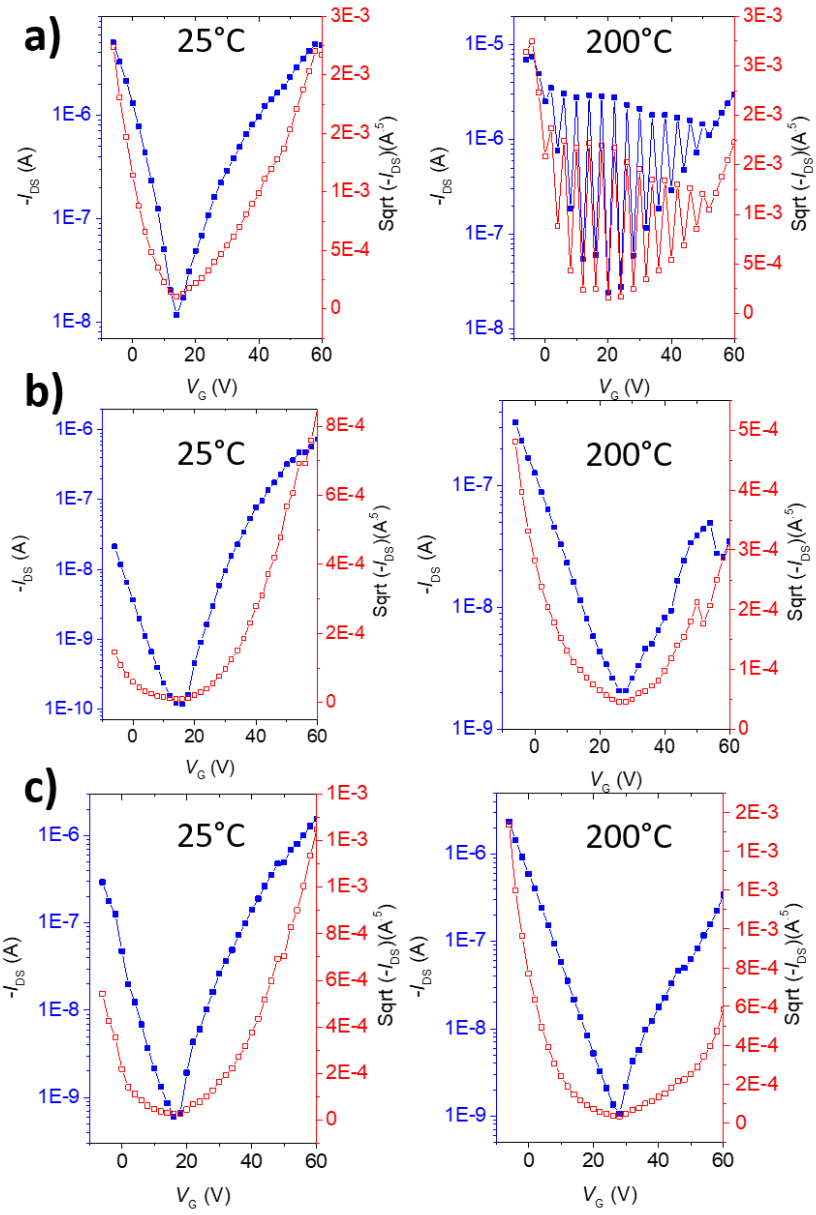


Figure 2.29. Transfer curves from the transistor devices based on a) pristine BDOPV films, b) PVK based blend films, and c) PAC based films both at room temperature and high temperature under ambient air. Stable currents are measurable for the blend films at elevated temperature while the pristine films become extremely unstable.

2.7 Conclusions

To design high-temperature semiconducting polymer blends, a few requirements appear to be essential: (i) a host matrix with a glass transition temperature higher than the desired operating temperature; (ii) a semicrystalline semiconducting polymer; (iii) the interpenetration of the semiconducting component into the host matrix; and (iv) improved intermolecular π- π stacking within semiconducting channels that can be retained at high temperature. The use of high-T_g matrices was demonstrated to be a general strategy to attain these properties by minimizing spatial rearrangements within the polymer films at elevated temperatures. We believe that the superior ordering in the confined channels enhances charge transport by reducing activation energy and trap density through improved ordering therefore providing positively contributing factors to counter the thermal expansion and potential charge scattering that would typically deteriorate the charge transport efficiency in the polymer films.

CHAPTER 3. ALL-PLASTIC THERMALLY STABLE ELECTRONICS

3.1 Introduction

Organic-based electronics that are conformable, flexible, low-cost, and lightweight have been studied for the past two decades as alternatives for silicon-based technologies.[9, 101] Today, flexible electronics are on the verge of becoming a commodity in daily life applications such as flexible displays and wearables. One class of application that is yet to benefit from these lightweight and cost-effective electronics is for high-temperature applications, especially in aerospace engineering, automobile industry, as well as gas and oil drilling industries.[42, 68] These applications require lightweight materials that can sustain harsh thermal conditions for prolonged operation times without requiring additional insulation or cooling. Currently, active or passive cooling and insulation are needed for such applications pausing a weight and cost burden especially in aerospace engineering.[35] Carbides and other wide-band gap inorganics have been studied as thermally-robust alternatives, but their cost and complicated processing limit their wide adoption.[42] With such requirements, plastic electronics based on thermally-stable plastic substrates, dielectrics, as well as semiconductors potentially become excellent candidates.

Polymers are common as thermal shields for high temperature applications. This makes them excellent substrates for the fabrication of lightweight electronics. Besides, polymer materials, mainly polyimides have shown excellent dielectric breakdown strengths making them excellent candidates as dielectric layers in transistor designs.[102-106] The long-standing challenge towards achieving thermal stability has been the design of thermally-stable semiconductors as electronic properties are temperature-dependent and degrade especially at extremely high temperatures.[36, 107] Organic semiconductors, a class of materials which exhibit a thermally-activated electronic behavior, were discussed above to be rendered thermally-stable through strategical blending and

composites formation.[108] High glass-transition temperature (Tg) matrix polymers were used as hosts in thin films to increase the thermal stability of the semiconducting blends up to 220 °C. With this approach we demonstrated excellent high-temperature operation stability as opposed to other works that mostly investigated the effect of annealing temperatures.[47, 50, 51, 109, 110] The blending strategy allows for common semiconducting polymers to be processed into thermally-robust thin films to fabricate transistor devices that can function under thermal stress. This strategy thus offers the opportunity for facile fabrication of largescale plastic electronics functional under extreme temperatures.

In this chapter we discuss a sequential layering approach to fabricate all-plastic, thermally-stable transistor devices comprised of all-polyimide layers. We explore the design principles to yield thermally resistant transistors and demonstrate their performance abilities in harsh thermal conditions. We close the chapter by discussing potential electronic applications in which these lightweight devices would be either complementary to the current technologies or even constitute excellent alternatives.

3.2 Experimental

3.2.1 Materials

Kapton® HN (100 HN and 500 HN) substrates were obtained from DuPont as a gift and were rinsed by sonicating for 5 minutes in hexanes, isopropanol, then acetone prior to usage. Poly(pyromellitic dianhydride-co-4,4-oxydianiline)(PAA) was obtained from Millipore Sigma and used received. Matrimid® 5218 (MI) was purchased from PolyK Technologies and purified by precipitation, filtration, washing with methanol and drying before use. Is-P1 was synthesized and purified as reported in our previous works.[73, 108] All polymer solutions were obtained in chloroform and allowed to stir overnight prior to forming corresponding blends. High purity Au

and Al pellets were purchased from Kurt J. Lesker Company and subject to high vacuum before deposition.

3.2.2 OFETs fabrication and characterization:

Polyimide substrates were first cut into desired shapes and rinsed in hexanes, isopropanol, then acetone. After nitrogen-drying, the substrates were carefully transferred into a high-vacuum chamber ($2x10^{-6}$ mbar) and Al gates were deposited at a deposition of 5.0 Å/s to a final thickness of 70 nm. A film of PAA was then spun onto the Al-covered substrates as previously reported[104] (spin rate of 6000 rpms for a minimum of 2 minutes). The substrates were then allowed to heat up to 300°C for 1 hour at ambient for a complete imidization and PI film formation. These processing conditions yield 200 nm thick films of PI after curing. After cooling down, the substrates were then rinsed with hexanes, ethanol, then chloroform and dried with nitrogen gas. A semiconducting layer of Is-P1/Matrimid blend was then deposited by spin coating chloroform solution (10 mg/mL, 3000 rpms, 30 s) then annealed at 220°C for 30 minutes inside a nitrogen-filled glovebox. For the temperature dependent studies, the 50/50 blend ratio was chosen for the bi-continuous morphology. Au source/drain contacts were then deposited through a prepatterned shadow mask (channel length of 40 μm) at a rate of 0.8 Å/s to a final thickness of 30 nm.

OFET devices characterizations were carried out using a Keithley 4200 in ambient environment. The field-effect mobility was calculated in the saturation regime by using the equation $I_{DS} = (WC_i / 2L)\mu(V_G - V_T)^2$, where I_{DS} is the drain-source current, μ is the field-effect mobility, W is the channel width, L is the channel length, C_i is the capacitance per unit area of the gate dielectric layer, V_G is the gate voltage, and V_T is the threshold voltage. A channel area of 1500 μm was carefully isolated and a channel length of 40 μm was used for mobility calculations. OFET

performances were obtained by applying a gate bias from −15 V to 6 V, with the potential gradient between the source and drain contacts kept at −10 V.

3.2.3 Capacitance measurement:

To extract the capacitance of the PI dielectric, polyimide substrates were first cleaned and transferred inside a thermal-deposition chamber. A thin layer of Au was then deposited, followed by spin coating and thermal curing the dielectric layer. Using 1.1 mm x 1.1 mm stainless steel shadow mask, the Au/PI/Au sandwich structure could be achieved. The capacitance was then measured using a GW Instek LCR-6100 Precision LCR Meter in the Au/PI/Au sandwich configuration. The frequency could be varied from 100 Hz to 100 kHz. The capacitance was calculated to be around 4.5 nF/cm^2 in good agreement with previous reports.[103, 104] To probe the thermal stability of the dielectric layer, the Kapton/Au/PI/Au sandwich assembly was brought to different temperatures and the measurements were taken in ambient air.

3.2.4 In-situ temperature-dependent measurements:

To control the thermal conditions both for FETs characterization and capacitance measurements, the HFS600E-PB4 Linkam stage was used with the heating and cooling rates maintained at 10 °C/ min and the devices were allowed to reach thermal equilibrium for 30 minutes at each temperature before measuring unless indicated otherwise.

3.2.5 Morphology analysis

The AFM height were obtained using Cypher Asylum AFM and processed through Gwyddion Software. All films were processed on cleaned Kapton substrates and film morphology was imaged after annealing the blend onto top of the imidized PI film. To extract the thickness, a sharp probe tip was used to form a notch through the thermally cured film or the semiconducting blend film.

3.3 Thermally stable plastic transistors fabrication

3.3.1 Thermally stable plastic substrates

In transistor fabrication, substrates selection constitutes on the important steps in the optimization of the electronic performance. The ideal substrate material should be highly smooth and defect-free to allow the formation of a smooth gate contact or should exhibit excellent wettability in the case of thin film processing directly on the substrate's surface. Commonly, silicon substrates are used because they can readily be heavily doped to serve as the gate and at the same time allow the growth of a thin silicon dioxide layer to serve as the insulating dielectric. For non-conductive substrates, it is common to coat the substrates with conductive layers: vacuum-deposited metals and metal oxides, nanowires, conductive polymers or even graphene.[14, 111-116] One of the most widely studied plastic substrate is ITO-(Indium tin oxide) coated polyethylene terephthalate (PET) For high temperature applications however, the use of PET becomes limited. Typically, PET substrates will begin to wrinkle above 150°C and the corresponding sheet resistance ITO-coated PET will greatly increase.[117] This has thus limited the use of these substrates in high temperature electronics.

With the recent celebration of the 50th anniversary of the moon landing, we were reminded that polyimides have been used for long as heat-resistant materials. In high temperature transistors designs, they have been investigated as substrates for fabricating thermally-stable and flexible electronics.[46-48, 118, 119] For instance Kuribara et. al. utilized polyimide substrates and fabricated transistor devices for sterilizable medical devices.[47, 110] By using thermally-resistant organic small-molecule semiconductors, the fabricated flexible devices showed to remain functional after annealing at temperatures up to 250 °C. The use of polyimide substrates thus enables the fabrication of flexible electronics able to sustain thermal environments in which the commonly used plastic substrates such as PET would not survive.[117] In this chapter, we thus proposed that by

utilizing thermally resistant plastics, i.e. polyimides, we can pattern the gate metal contacts, and retain the electrical performance at elevated temperatures. We selected Kapton as one of the most robust polyimides that is commercially available. Besides its thermal durability, Kapton offers flexibility and lightweight, and most importantly its compatibility with the dielectric layer which we will discuss in the sections below. Kapton substrates were also available in different thickness gauges (25 µm for Kapton® HN 100 and 125 µm for Kapton® HN 500) which allows to tune the flexibility and the overall weight of the devices. Figure 3.1. a) shows the molecular structure of Kapton; b) the proposed approach of processing large area transistor patterns for the manufacturing of plastic electronics; and c) shows a micrograph of the actual Kapton® HN 100 with Al gates patterned on it for transistor fabrication. In this study we could pattern hand-size substrates which would enable the fabrication of transistor arrays for future applications.

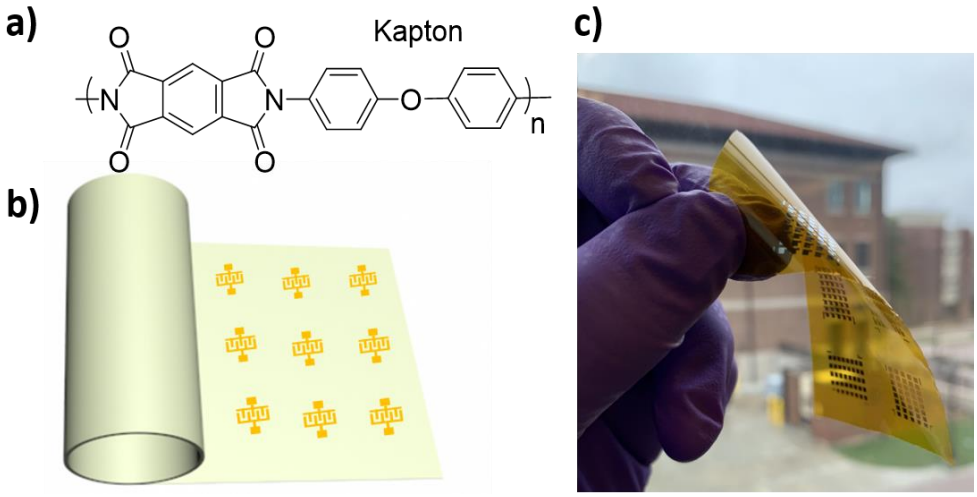


Figure 3.1. Thermally stable plastic substrates. a) Molecular structure of polyimide (Kapton) selected a thermally robust substrate. b) Design approach of large area processing of patterned electronic circuits onto plastic substrates. c) Micrograph of a Kapton substrate with transistor devices patterned.

3.3.2 Thermally stable dielectrics

To complement the thermal stability of the substrates, thermally stable dielectrics layers are needed for the fabrication of thermally stable transistors. To separate the gate contact from the semiconductor and the source drain contacts, a dielectric material must form a thin, smooth, pinhole-free layer that allows the accumulation of induced charges and their flow upon biasing. Polymer dielectrics have been studied and have shown excellent performances especially in flexible transistors.[25, 120-124] Some of the most widely studied dielectric polymers in plastic based electronics include poly(methyl-methacrylate) (PMMA), poly(styrene) (PS), and poly(vinyl-phenol) (PVP),[125, 126] but their low Tg and melting points negate their relevance to the current discussion of high-temperature electronics. Other polymeric dielectrics such as polylactide (PLA) have been studied by thermal stability also limited to around 200°C [127] To circumvent this issue, in the reported sterilizable transistor devices, metal oxides such as AlOx were utilized as thermally resistant dielectrics.[46, 47, 101, 109, 110] These metal oxides which are typically thermally processed enable high temperature annealing stability.

A much better match to our selected substrates is polyimide-based dielectric layer. Serendipitously, polyimides constitute a class of excellent dielectric materials as they exhibit excellent capacitive response to electric field, as well as high capacitive breakdown ability with low power consumption in transistor devices.[102-106, 128, 129] For instance, the polymerization of pyromellitic dianhydride (PMDA, $C_{10}H_2O_6$) with 4, 4′-oxydianiline (ODA, $C_{12}H_{12}N_2O$), followed by a thermal curing step, has been used to process highly uniform and smooth films of polyimide dielectrics used in transistor devices.[128-130] Figure 3.2. shows the molecular structures of the polyimide dielectric made from the thermal imidization of a precursor poly-amic acid (PAA) solution in dimethylacetamide (DMAc). The precursor is readily made from the polymerization of pyromellitic dianhydride with 4, 4′-oxydianiline.

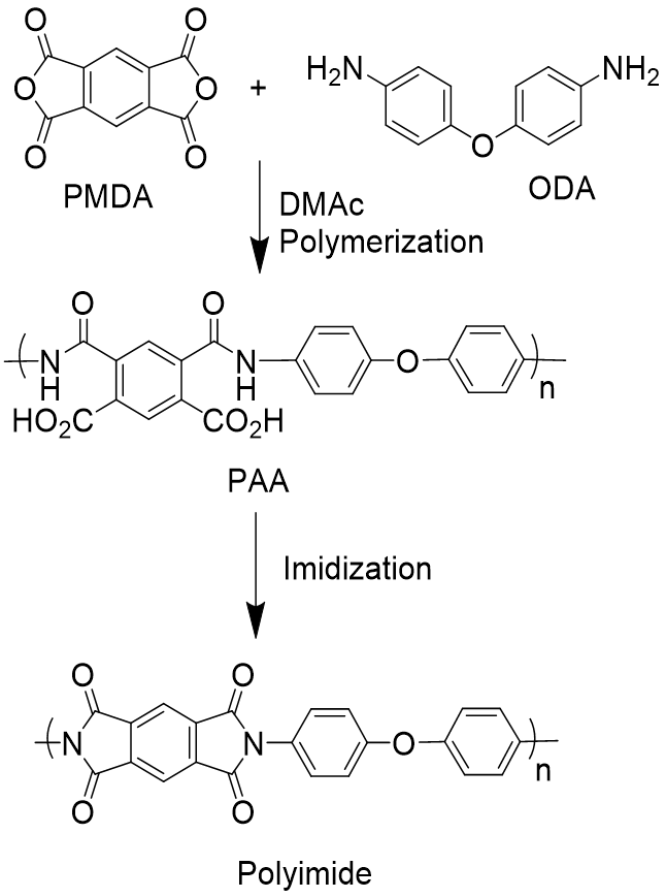


Figure 3.2. Polyimide-based dielectric. Illustration of precursor solution formation followed by thermal imidization step to form polyimide-based dielectric films.

In our design for all-plastic transistors, this facile formation of polyimide-based dielectrics from readily available precursor solution thus allowed to us to process the insulating layer atop of the pre-patterned Kapton substrates. Furthermore, the polyimide-based dielectric, which is in structure similar to Kapton offered the following: i) thermal durability similar to that of the substrate; ii) structural compatibility which enables intimate layering; iii) the chemical and mechanical resistance needed to process the semiconductor layer and the source/drain contacts; and most importantly iv) minimal mismatch in thermal expansion coefficient between the substrate and the overlaying dielectric.

Figure 3.3. a) shows a micrograph of the PAA precursor solution which could be processed by spin coating then thermally cured to form smooth films of the polyimide as revealed by the AFM height image (Figure 3.3. b). We were able to obtain the desired highly uniform and smooth films on top of the Kapton substrates. Since the dielectric layer ought to meet thinness requirement for efficient charge storage, we measured the thickness on the formed layer by introducing a notch and measuring the depth by AFM. Figure 3.3. c) reveals extracted thickness of 200 nm when the PAA films was cured. This thickness has been reported to yield an optimal capacitance around 4.0 nF/cm^2.[104] In the case of polyimide-based high temperature dielectrics, we are more interested in whether the capacitive properties will be retained after exposure to harsh thermal conditions. Figure 3.4 shows the capacitance measurement of our thermally-cured dielectric under different heating temperatures. Independent of the frequency, the dielectric shows excellent capacitive properties from room temperature up to 200°C. This behavior is important for the transistor performance at high temperature as we look for material candidates that can store charge upon biasing and do so under extreme conditions.

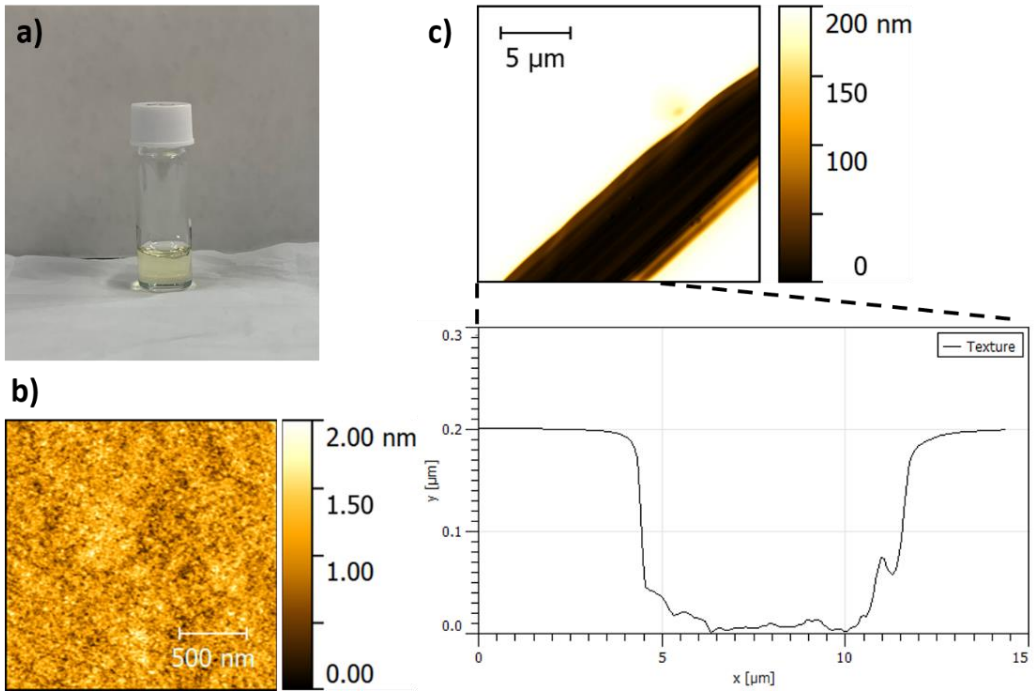


Figure 3.3. Polyimide dielectric processing. a) Micrograph of the poly-amic acid used for solution processing of polyimide dielectric. b) AFM height image demonstrating the smooth film obtained after thermal imidization. c) Thickness evaluation of the imidized dielectric layer.

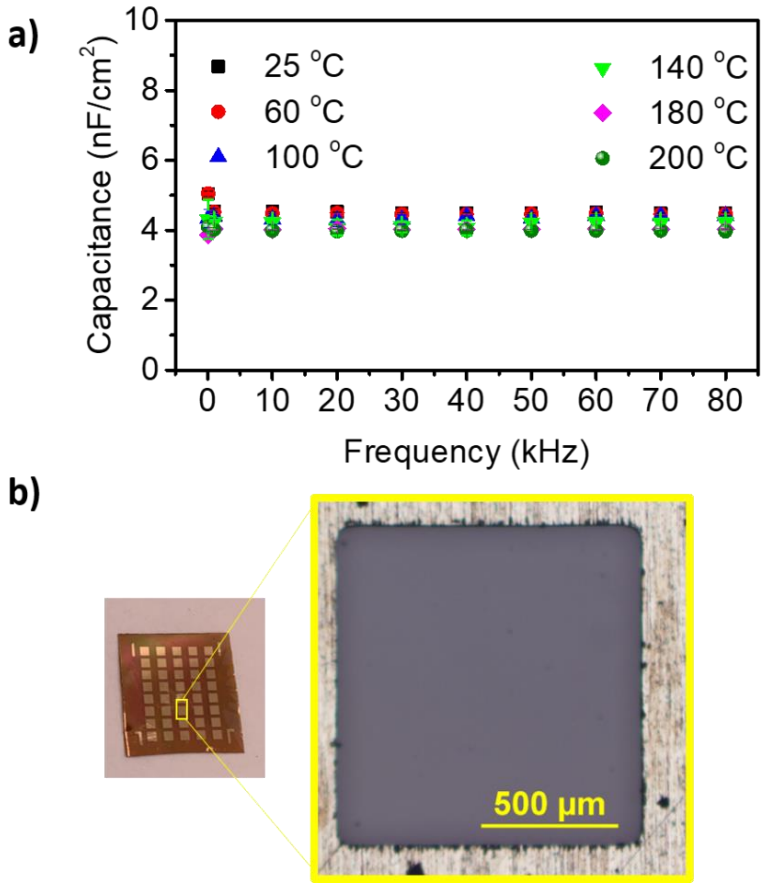


Figure 3.4. Capacitance characterization of polyimide. a) Temperature and frequency dependent capacitance measurements demonstrating the thermally stability of the thermally cured polyimide dielectric. b) Micrographs of the Au/polyimide/Au sandwich assemblies used for capacitance measurements.

3.3.3 Sequential layering approach

To complete the all-polyimide transistor device, we solution-processed polyimide-based semiconducting polymer blend as described in previous chapters. Matrimid a high-Tg polyimide was thus selected as the solution processable matrix to attain the functional semiconducting layer. Matrimid (Figure 3.5. a) offers excellent processability in chloroform (among other solvents), a good solvent for most conjugated polymers for blending purposes. Besides, both our Kapton substrates and thermally cured dielectric exhibit excellent chemical resistance towards chloroform. Furthermore, utilizing a polyimide as the host matrix in the active layer adds to minimization of

the structural differences between layers. With this fabrication strategy, we not only facilitate and generalize the device fabrication process, but also reduce the mismatch in thermal expansions between different layers and therefore improve the overall thermal stability in all-plastic device assemblies. To form the semiconducting layer, we selected the previously discussed isoindigo-based Is-P1 (Figure 3.5. b) as the conjugated polymer for demonstration as a semiconductor. This polymer, alone, was found to have heat resistant semiconducting properties.[108] As discussed in chapter 2 above, we aim to form an interpenetrating network of the semiconducting polymer domains for two main reasons: 1) to attain efficient charge transport across the whole film; and 2) to ensure the local physical confinement by the high Tg host.

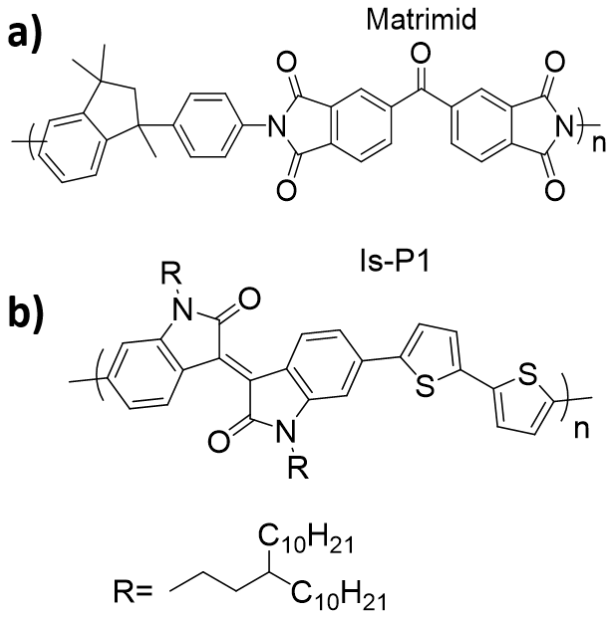


Figure 3.5. Semiconducting layer design for thermally stable all-plastic transistors. a) Molecular structure of Matrimid used as the polyimide host in the semiconducting layer. b) Molecular structure of the isoindigo-based semiconducting polymer used in the semiconducting blend.

To probe the formation on interpenetrated networks of Is-P1 in the thin films, we used utilized AFM imaging on the films processed on top of the polyimide-based dielectric layer. We

first varied the content of Is-P1 in the blend films and found that with small contents (> 20 wt%), the semiconductor forms isolated domains as shown in Figure 3.6. a), which as previously discussed are detrimental to both the charge mobility and confinement induced stability. We find that with enough content (~ 50 wt%) of Is-P1, its domains begin to interconnect forming the desired interpenetrating network as seen from AFM images in Figure 3.6. b). We then select this blending range for the study of thermally stable all-plastic devices. Note that here we aim to utilize the host matrix as the majority in the blend since the high Tg polymer is designed to dictate the film rigidity especially at very high temperatures. We also extract the thickness of the semiconducting layer to find that a very thin layer could be formed through this processing route as seen in Figure 3.7. It was found to be beneficial for the device performance to form films that are 100 nm (or thinner) in thickness. This thickness level enables efficient charge accumulation without any leakages followed with effective injection into the functional channel.

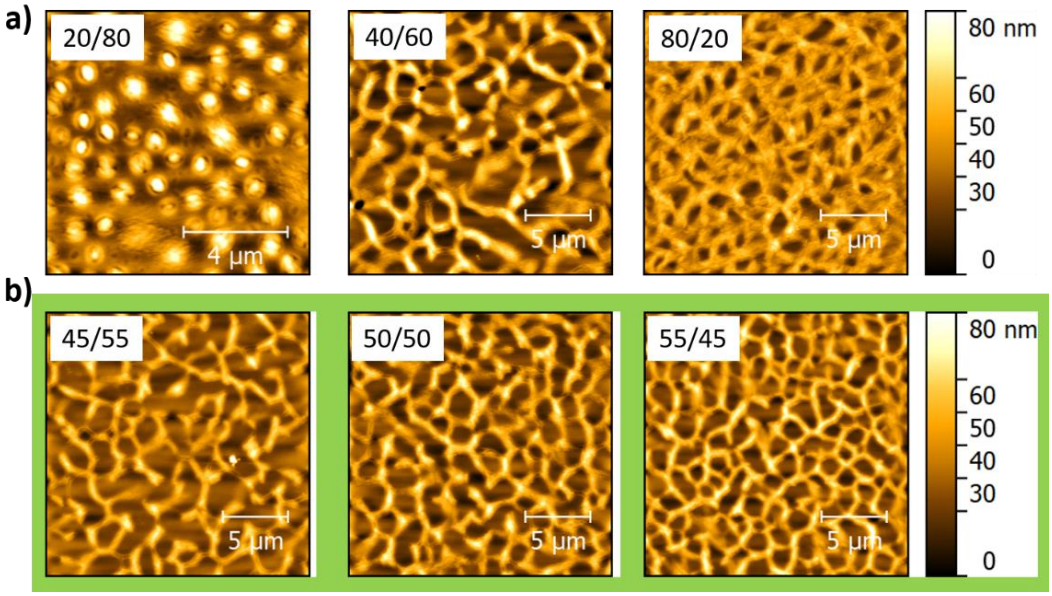


Figure 3.6. Morphology evaluation for the semiconducting polymer blend. a) AFM images of films with varying contents of the conjugated polymer in the blend. b) Optimized blend rations reveal interpenetration of the semiconducting domains uniformly in the thin film.

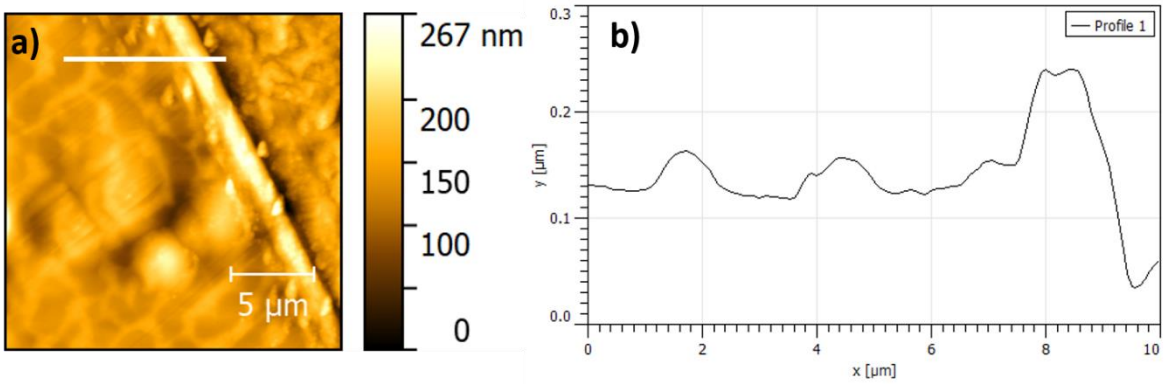


Figure 3.7. Thickness evaluation of the semiconducting blend. a) AFM height image of the Matrimid/Is-P1 film processed on top of the polyimide substrate and dielectric. b) A notch is cut through the semiconducting film and the line profile is extracted from the AFM image.

Figure 3.8 shows the transistor device fabrication processing using the sequential layering of all-polyimide layers. With this approach we can fabricate the bottom gate top contact architecture, preferably, using all-polyimide components. This geometry is dictated by the fact that the solvent (DMAc) used to process the dielectric layer might chemically dissolve the organic semiconducting layer. In order to study other device geometries such as tog gate, chemically-robust blends would be of interest in order to tolerate the processing conditions of the dielectric as well as the gate deposition. Nonetheless, the current FET configuration allows us to extract the thermal tolerance of the plastic devices and the resulting charge transport properties.

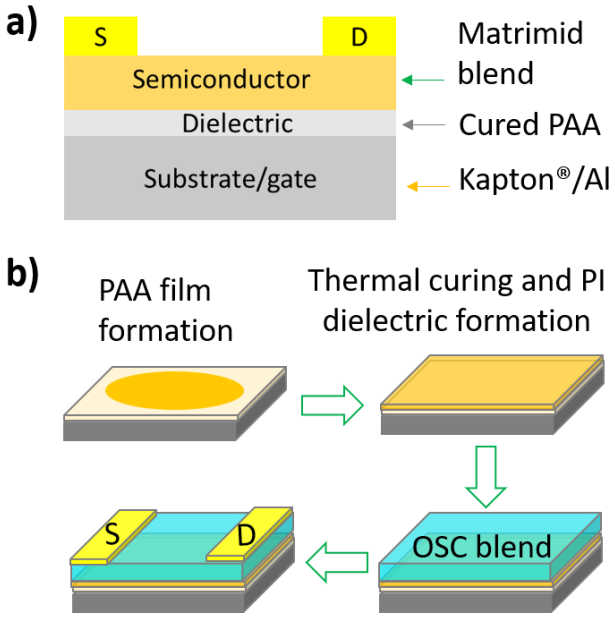


Figure 3.8. All-polyimide transistor processing. a) Studied device architecture for thermally stable plastic electronics.

We first characterized the plastic devices under ambient conditions to evaluate and optimize their electronic performance. The fabricated transistor devices are which flexible, light-weight exhibited charge carrier mobilities as high as 0.20 cm^2/Vs, ON to OFF current ratios around 10^4, and threshold voltages of 3 V. On average charge mobilities of 0.15 cm/Vs could be obtained among 10 different devices. Figure 3.9 shows the characteristic transfer and output curves obtained from the plastic devices measured in the open air. Ideal characteristics could be obtained in combination with the outstanding parameters mentioned above. Figure 3.10 shows the statistical distribution of the charge carrier mobilities extracted from 10 different devices. This distribution ensured us that the designed fabrication route is readily repeatable and that excellent device performances can be attained in plastic devices. In fact, this approach was robust enough that even the undergraduate students could independently replicate the plastic devices during their training. Noteworthy here was the difficulty off penetrating the thermally cured dielectric layer to make

intimate contact with the underlying gate for the electronic measurement. We found it to be useful to use sharp probe tips to easily penetrate the polyimide layer to access the gold gate contact. More interestingly, the transistor devices could be operate using extremely low voltages. This is advantageous especially for high temperature applications where power consumption is targeted to be minimal.[44] Due to the low capacitance of the polyimide dielectric layer, the charge accumulation and injection processes required the application of voltages that are as low as 10 V. This in contrast to other dielectrics such as SiO_2 which typically require operational; drain voltages as high as 100 V.

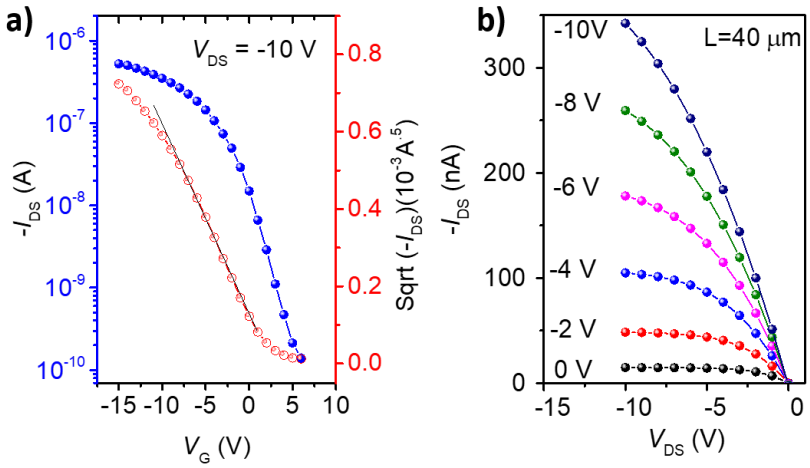


Figure 3.9. Electronic characterization of the plastic transistor devices. Characteristic a) transfer curve and b) output curve of the measured transistor devices showing ideal behavior as well as low power consumption (V_{DS} of -10V).

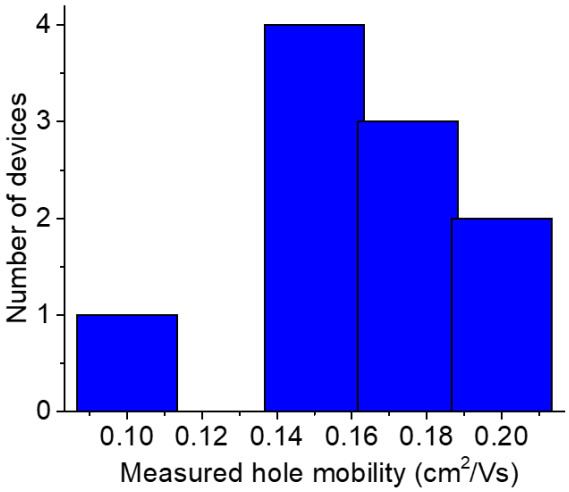


Figure 3.10. Statistical distribution of charge mobilities measured from 10 different transistor devices selected at random from multiple batches.

3.4 Temperature resistant plastic transistors

To test the thermal stability of the fabricated plastic devices, we measured their electronic properties from room temperature up to 220 °C in ambient air. In typical electronics, such thermal stress will lead to uncontrolled increase in charge carrier density leading to excessive doping levels and carriers scattering resulting into the loss of the amplifying power of the transistor devices. Especially for conventional organic semiconductors, in this temperature regime, morphological fluctuations and thermal expansion normally will lead to significant decline in device performances.[46, 51, 55, 57] As previously discussed, the main form of disorder in polymer chains is torsional disordering along the polymer backbone. With our blending strategy, we have now established that this freedom to distort the main conduit for charge carriers is minimized. Other forms of disorder in transistor devices can result from the mismatch in thermal responses between layers. This mismatch would induce detrimental strain either at the interface or even with semiconducting channel. As stated in the design of the all-plastic devices, we aim to lift this barrier

by utilizing components that are compatible in nature and thus have similar responses to thermal stress.

Figure 3.11 illustrates the behavior of our plastic devices under different level of thermal stress. Part a) shows the evolution of the transfer curve with increasing temperature. As expected, the charge transport exhibits a thermally activated behavior where the current increases with increasing thermal energy. It is obvious however than upon heating, excellent overlapping transfer currents can be measured with no decline even when operating at as high as 220C. Note that this not expect to be the stability; in our studies we only measured up 220°C as it would be experimentally challenging to further increase the surface temperature at ambient. Besides, we aimed to match our measurements under inert conditions, which due to instrumentation limitations are bound to around 200°C. Part b) shows a micrograph of our plastic device being heated to 220°C at ambient using the Linkam hot stage and temperature control.

We extracted the ON and OFF currents from the transfer curves and plotted their evolution with increasing temperature in Figure 3.11 c). These plastic devices can retain their I_{ON}/I_{OFF} even when operating at 220°C in the open air. We observed a slight increase in the OFF current due to the thermally activated filling of shallow traps in the channel. This increase was however accompanied with the increase in the "turn-on" current which allows our devices to retain their amplifying properties even under extreme thermal stress.

Another parameter indicative of thermal stability is the threshold voltage. That is the amount of bias needed for the devices to switch from OFF to ON state. With a decline in the amplifying abilities of the transistor at high temperature, it would require much high potential to drive the device. For our plastic devices, the extracted threshold voltages showed minimal variation as the operating temperature increases as shown in Figure 3.11. d). At 200°C, the

threshold voltage shifted from 3 V (at room temperature) to 2 V. This slight decrease indicates that it requires less potential to drive the current in the plastic devices at high temperature that it does at room temperature. This behavior supports our blending design which aims to take advantage of the thermally activated charge transport, given that the detrimental disordering is minimized. This indicates that the plastic transistor devices can function under high temperature while requiring low power consumption. These transistors would be excellent candidates for signal amplification at high temperatures for various applications as well as fundamental studies.

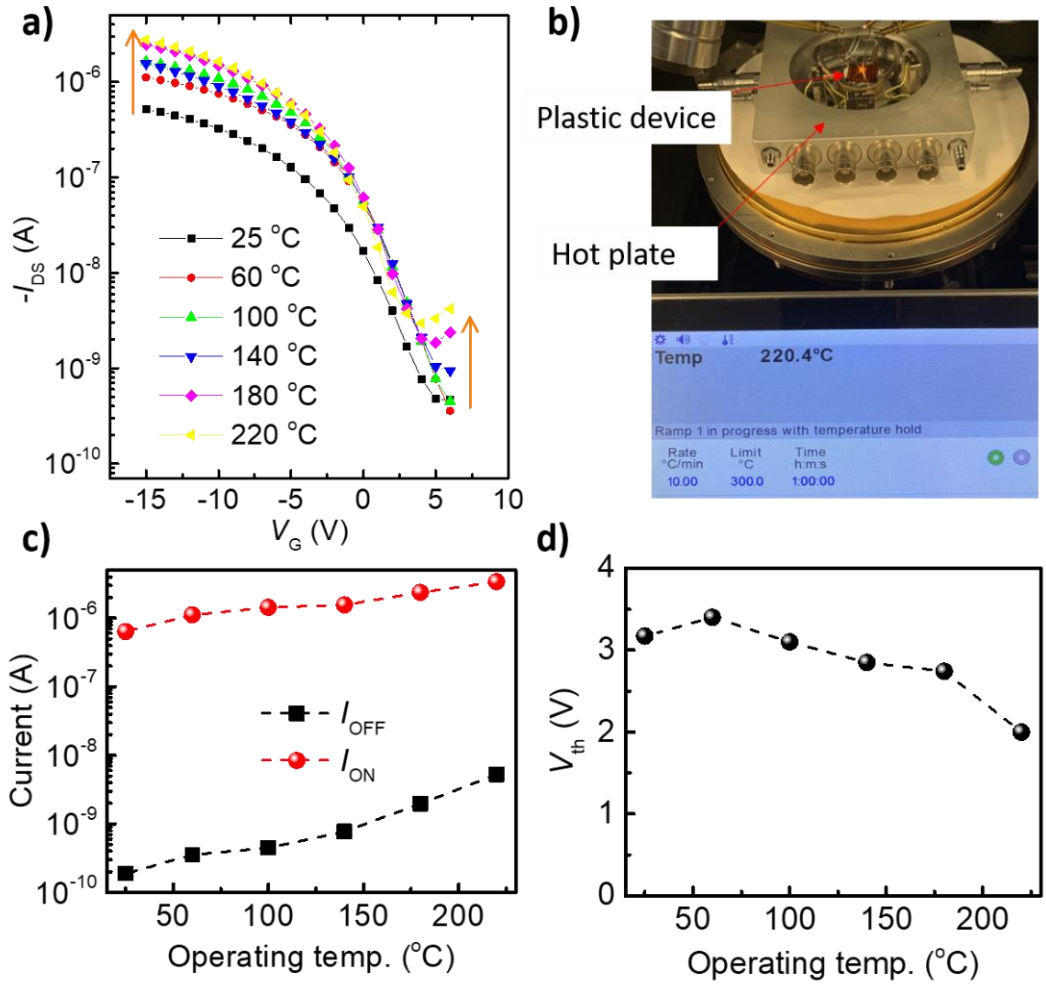


Figure 3.11. Temperature dependent characterization of the plastic devices. a) Thermal response of the transfer current showing increasing ON currents due to thermal activation. b) Experimental setup for the in-situ temperature dependent measurement of the plastic devices. c) Temperature dependent ON and OFF currents obtain from the representative average transistor device. d) The extracted threshold voltage with increasing temperature showing minimal variation upon heating.

We also probed potential leakage currents in our devices especially at high temperatures. To do so, we measured the gate-source current compared to the source-drain current. A high gate-source current would signify that our transistor devices are unable to store the induced carriers upon gate biasing. In the case of leakage, the current would freely flow from the gate contact to the source contact. Figure 3.12 shows the gate current compared to the drain current both at room

temperature and at oven-like temperatures. Our devices exhibit gate current that are essentially lower than the OFF drain current Even upon applying the gate bias, the current remains to 10^{-9}A which his below the current flowing between the source and drain before the device is turned on. This indicates that the current flow between the gate and the overlying contacts is, independently of the applied bias, negligible compared to the exponentially amplified source-drain signa. This indicated that our dielectric layer can store the induced carriers at the gate interface and that the functional is able to allow their flow strictly from the source to the drain contact with no leakage. These properties are also maintained at elevated temperatures This behavior could be supported by the in-situ temperature-dependent capacitance study discussed above which revealed that the polyimide dielectric layer can retain their excellent capacitive behavior even when under baking conditions in agreement with previous reports.[103]

To evaluate any potential excessive charge trapping, we also carried out hysteresis measurements on our plastic devices both before heating and under thermal stress. The hysteresis measurement is commonly used in transistor devices as a direct indicator of any irreversible charge localization or trapping. In this experiment, the gate bias is swept from lower values to high values and then backwards. In the ideal scenario, the resulting transfer currents should overlap perfectly meaning that the induced charge carriers are able to move freely within the channel upon source drain reverse biasing. Figure 3.12 shows the overlapping forward and backward scans of the transfer current at room temperature and at 200°C under open air. Our devices exhibit minimal hysteresis in both conditions which indicates that there is no significant charge trapping within the devices in the measured voltage ranges. We attribute this excellent overlap to the fact that we employ a low capacitance dielectric layer which allows for the devices to operate at low voltages.

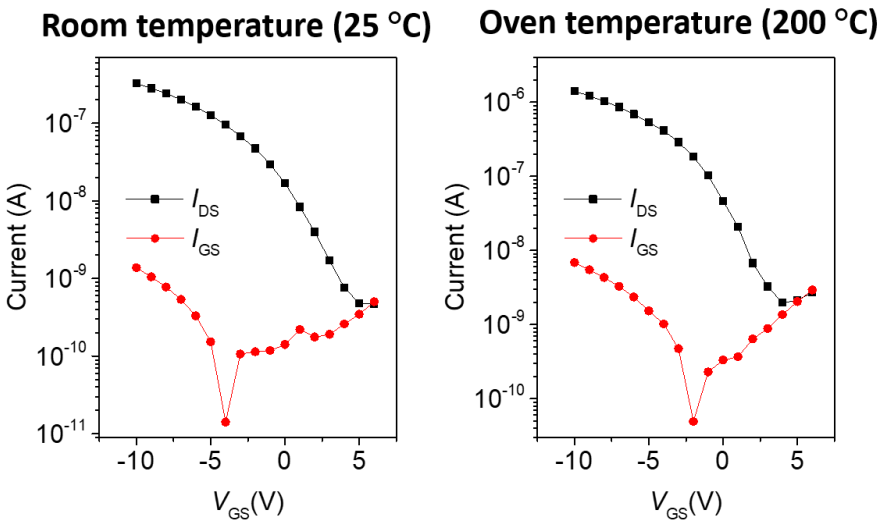


Figure 3.12. Leakage current evaluation. The voltage dependent gate current is measured and compared to the drain current. Both room temperature and high temperature measurements indicate that the plastic devices have leakage-free behavior.

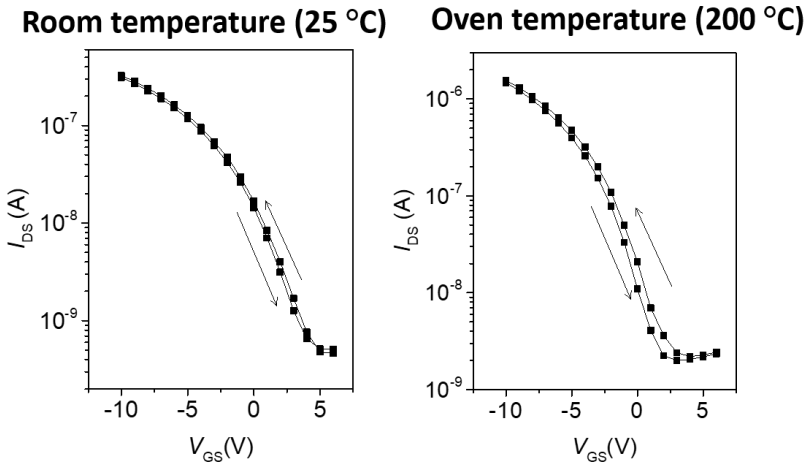


Figure 3.13. Hysteresis characterization. Forward and backward scan on the transfer current both at room temperature and under oven-like conditions.

3.5 Baking of plastic electronics

To further test the thermal durability of our plastic devices, we tested the transistor properties under continuous heating at 195 °C equivalent to a baking oven environment. In such conditions, other electronics both organic and inorganic exhibit high leakage currents, unstable

drain currents, and increased operating voltages. Since we employed thermally robust components in all layers of our transistor devices, we expect to greatly improve the thermal stress tolerance in our devices. Figure 3.14. shows the thermal stress test setup for our plastic devices under baking oven-like conditions. Also shown are the overlapping transfer characteristics as the devices are baked over long periods of time. The plastic devices ideal characteristics and show little to no change in the current with increasing baking time. This confirms that our devices are thermally tolerant.

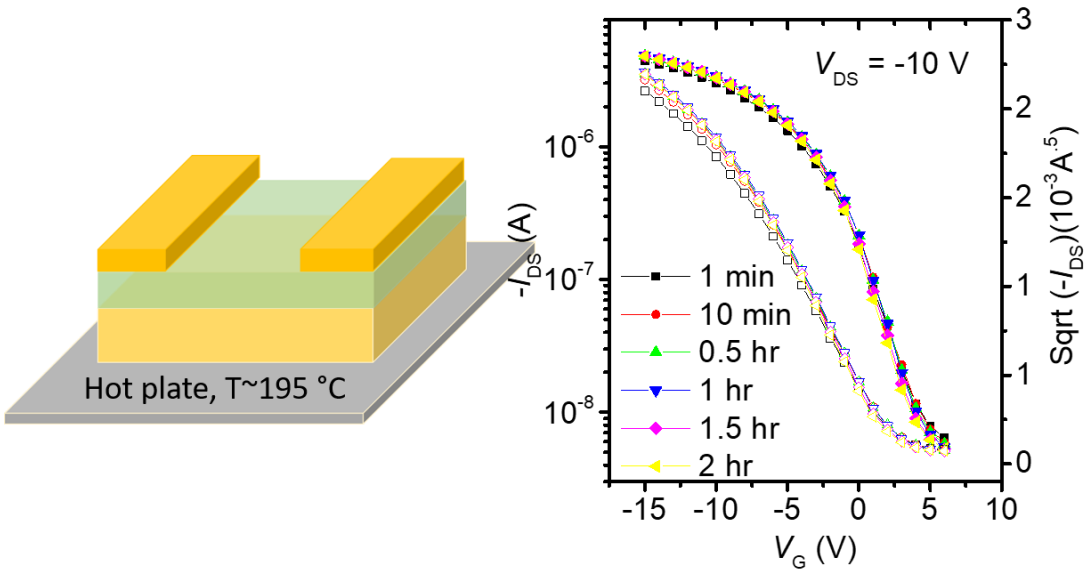


Figure 3.14. Effect of baking study on the transfer characteristics of plastic transistors. Ideal behavior is retained even after 2 hours of thermal stressing.

We also examined the output current on the plastic devices upon baking. The output curve tells about the current modulation with varying gate bias and source-drain potential. It also gives the quantitative information on the difference between the OFF state and the ON state of the transistor device. In case of high leakage currents, the transistor will remain "on" even without any gate potential applied. This would lead to the inability to modulate the current flow between the

source and drain contacts. As shown in Figure 3.15, the output currents were also found to be highly stable as we overlapped the measurement results after 30 minutes, 1 hour, and 2 hours. Effective current modulation with varying gate voltage, dependent of the drain potential can be observed even after baking for 2 hours at ambient. Furthermore, the current did not show to start to increase until the gate voltage was increased to 2 V. This indicates that without any gate potential applied, there is essential no current flow which supports the minimal leakage in our plastic devices. This behavior was true both before thermal stressing and after 2 hours of baking.

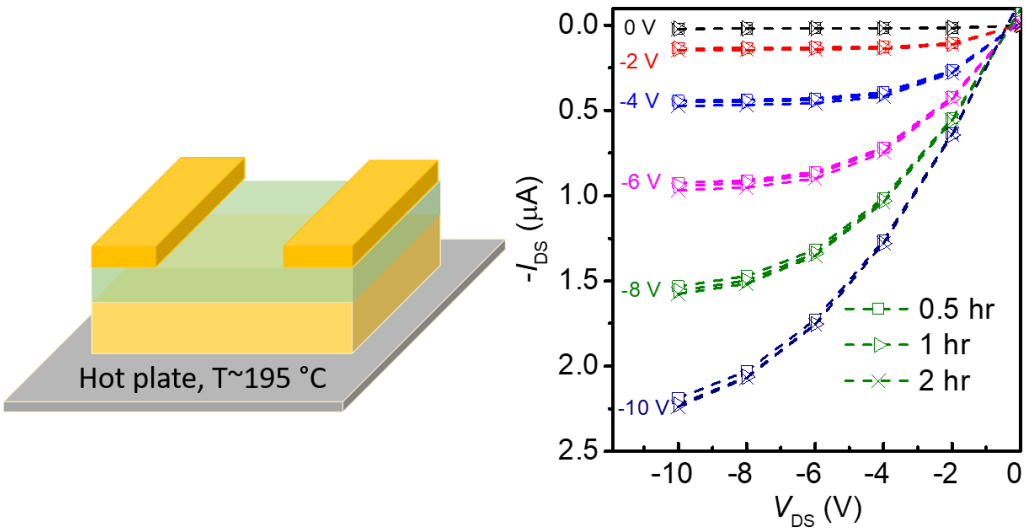


Figure 3.15. Effect of baking on the output characteristics of plastic transistors. Excellent output behavior is retained even after 2 hours of constant thermal stress.

Lastly, we extracted the ON and OFF current values as well as the threshold voltages as the devices were constantly baked. These parameters are important indicators of the stability on the transistor devices. As previously discussed, the ON to OFF current ratio tells the amplifying abilities of the transistor and threshold voltage indicates how much voltage is needed to operate the device. For a thermally stable device, the ON to OFF ratio should be kept stable under thermal stress. In addition, this current amplification should require a stable potential to obtain. Figure 3.16

shows the extracted OFF and ON currents from our plastic devices under the baking oven-like conditions for prolonged heating times. Up to 2 hours, our devices showed to maintain their original current ratio indicating an excellent tolerance towards thermal stress. Furthermore, the required threshold voltage also showed excellent stability and remained between 3.2 and 3.0 V. Here we recall that the drain-source potential required to drive these transistors was only 10 V. Such low potentials needed to drive these devices signify that low powers are needed to operate our transistor devices even at elevated temperatures.

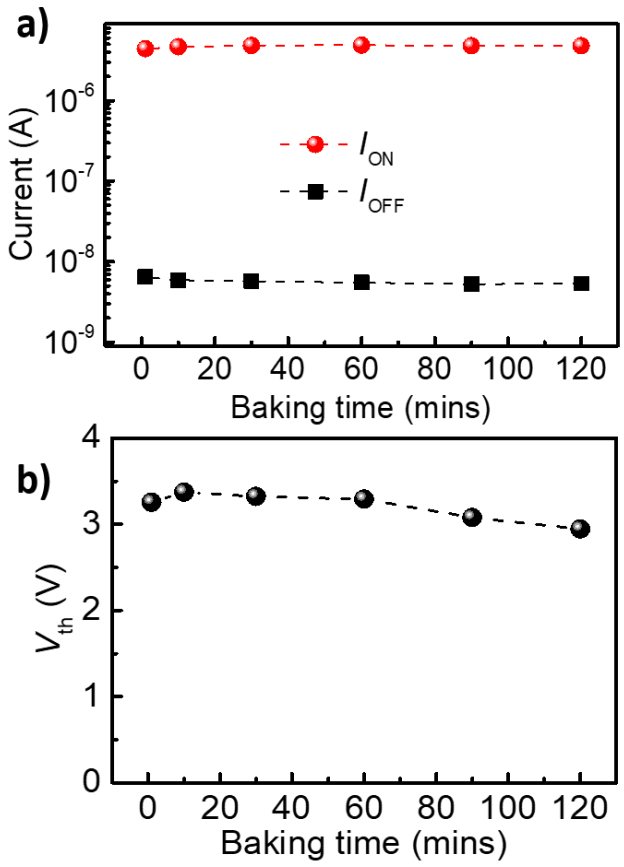


Figure 3.16. Effect baking test on FET parameters. Stable a)ON and OFF currents and b) threshold voltage could be observed when the plastic devices were heated for as long as 2 hours in the open air.

3.6 Conclusions

In this chapter, we investigated the demonstration of all-plastic thermally stable transistors. We used polyimide-based substrates, dielectrics, as well semiconducting polymer blends. This approach enabled the sequential layering of all components to fabricate transistors arrays that are flexible, lightweight, and high performing. The temperature dependent studies reveal that our plastic devices are extremely stable, and they can sustain long term baking. We attribute this excellent thermal stability of our plastic devices, first, to the compatibility in thermal expansion between all polyimide-based components of the transistor devices. Second, to the blending strategy which enables the semiconducting polymer chains to remain confined by the polyimide host. This confinement in bi-continuous morphologies minimizes morphological variations and reduces carriers scattering. In conventional transistors, prolonged heating normally leads to increased charge carriers scattering and uncontrolled changes in threshold voltages resulting into increased power consumption. In our devices, the required operational voltage (V_{DS}) was kept at -10V and the transistor devices could still exhibit excellent electronic properties. This ideality renders our approach an excellent candidate for high temperature sensing in which functional device components can sustain long-term heating with minimal power consumption.

CHAPTER 4. INFLUENCE OF MOLECULAR WEIGHT ON THERMAL STABILITY OF SEMICONDUCTING POLYMER BLENDS

4.1 Introduction

After our discussion in previous chapters, organic semiconducting materials have demonstrated the ability to function at elevated temperatures.[45, 46, 48, 51, 53] This is a feature that is needed both for fundamental understanding of charge transport mechanism and for a multitude of applications such as smart textiles, automobile and aircraft designs, downhole gas and oil drilling, and most importantly aerospace engineering.[20, 35, 66, 68, 107] To enable high temperature stable operation in the case of conjugated polymers,[57, 58] our discussion has been based on the use of high glass transition temperature (Tg) host matrices—as opposed to commonly studied softer insulators,[82, 85, 89, 131, 132] to form rigidified composites with conjugated polymers, process bi-continuous blend morphologies, and attain high electronic performance that is stable at temperatures as high as 220 °C.[108, 133] In this blending approach, the rigid matrix domains showed to confine the crystalline semiconducting chains, induce their closer packing and ordering, minimize microscale morphological changes in the film, leading to thermally resistant semiconducting properties.

One of the most important aspects of this blending strategy is its generality, meaning that once the blend components can form the nanoscale concrete-like morphology, a thermally-stable operation can be achieved. We found that when the matrix can physically confine the semiconducting chains hence minimizing their torsional freedom, effective charge transport becomes attainable at high temperatures. The physical confinement of the semiconductor at the mesoscale was thus discussed to be crucial in these systems. In an earlier report, Zhu et al. studied this physical confinement as an engineering tool for a complete mixing in polymer blend films.[134]

The authors demonstrated that in systems where the formation of micelles limits the miscibility of the blend components, instead of tuning the chemical composition, physically confining the polymer chains can induce complete mixing. It was shown that compatibilization (miscibility) results from entropic inhibition of phase separation into micelles, owing to confinement. The work demonstrated a formation of an intimately mixed microemulsion with a perfectly flat surface and a two-dimensional maze-like structure with columnar domains that extend through the film made from two highly incompatible polymers. This formation of uniformly distributed short range spinodal-like structures showed to be the key to thermal stability observed in our high Tg blends. We have so far referred to such morphology as interpenetrating. In our blending design where thin films are processed at room temperature with minimal control on the temporal quenching, the crystallization is rather rapid. This makes the accurate physical description of the resulting morphologies both intriguing, yet challenging.[135]

In polymer-polymer phase formation, the equilibrium polymer-polymer phase behavior is controlled by four factors namely (i) molecular architecture, (ii) the choice of monomers, (iii) the blend composition, and (iv) degree of polymerization.[135] To take advantage of our proposed universal physical confinement to induce mixing, tuning the blend composition and the molecular weight are the two experimentally accessible parameters in order to control the dynamics of the morphology formation. In this analysis, we target the spinodal decomposition morphology in which the two blend components are interpenetrating throughout the entire film. It is understood by Cahn's theory that during the spinodal decomposition, almost immediately after the bi-continuous pattern begins to form, interfacial tension is the driving force for the system to reduce its surface area by increasing domains size.[136] For our blend system, we would thus expect that the crystallization as well as the resulting blend morphology is highly dictated by the much more

crystalline conjugated polymer, which will crystallize first during the quenching process and that the matrix domains will be dispersed throughout the films between the crystalline conjugated domains. The formation of an interpenetrating morphology will then depend highly on the ability of the semiconducting domains to mix with the matrix domains during the film formation. In the search for high performance and thermally stable blend combinations, an extensive investigation on the miscibility criteria between our blend components is warranted.

In this chapter we investigated the impact of molecular weight on the crystallization behavior of the semiconductor and its miscibility with the thermally stabilizing matrix. We expect that the aggregation and coiling nature of the semiconducting polymer will highly influence its domains size in the blends and their dispersibility within the less crystalline matrix domains. Through fine tuning of both the degree of polymerization and statistical distributions among weight fractions, we demonstrated that molecular weight selection plays a crucial role in the formation of the bi-continuous morphology of blend thin films that leads to thermally stable charge transport. We selected a highly soluble diketopyrrolopyrrole (DPP) system to attain a wide range of molecular weights with narrow distributions. We then study the molecular weight-dependent morphology evolution in high Tg blends. We found that at extremely low molecular weights the miscibility is diminished, and the blends can only form isolated semiconducting nucleates with not network formation. We further showed that without this formation of the spinodal like morphologies, the thermal stability of the resulting morphology, and hence transistor devices, becomes poor. In presence of well-defined spinodal formation, thin films with excellent electronic properties could be readily processed to fabricate transistor devices that are stable even after being baked for 24 hours at elevated temperatures both in inert and ambient conditions.

4.2 Experimental

4.2.1 Materials

PVK (Average M_n 25-50 kDa) was obtained from Millipore Sigma and used received. To afford other M_n ranges of the PVK, the polymer was synthesized as previously reported.[137] Briefly, N-vinyl carbazole (494 mg, 2.55 mmol) and azobisisobutyronitrile, AIBN (12.6 mg, 0.077 mmol) was added to a Schlenk tube. Then, the Schlenk tube was degassed and filled with N_2 five times, followed by the addition of anhydrous toluene. The mixture was heated to 70°C and then poured into 200 mL of methanol. The precipitated solid was washed with methanol and died under vacuum to afford a white solid. The polymers with different molecular weights (M_n of 7.0, 35, and 48 kDa, as characterized by gel permeation chromatography, GPC) were synthesized by controlling reaction time and reagent amount. P2TDPP2TFT4 in four molecular weights was obtained from Corning as previously reported by their research team.[138] DPP-P2 and BDOPV were utilized following our previous reports and two different molecular ranges could be obtained by fraction extraction. High purity Au were purchased from Kurt J. Lesker Company and subjected to high vacuum before deposition.

4.2.2 UV-Vis absorption characterization

Samples were prepared by spin casting the chloroform polymer solutions onto cleaned glass substrates. All absorption spectra were collected using a UV/Visible/NIR Cary 3000i spectrophotometer. To compare aggregation behavior between films of pure polymers and corresponding PVK blends, and to probe the effect of temperature on the formed aggregates, all films were annealed to 200ºC and slowly cooled down to room temperature inside a N_2 glovebox before each measurement. The absorption spectra of the solutions were collected from chloroform solutions inside of a quartz cuvette.

4.2.3 Morphology analysis

The AFM height were obtained using Cypher Asylum AFM and processed through Gwyddion Software. All films were processed on cleaned silicon substrates and film morphology was imaged after annealing and/or baking of the blends. The films were annealed for 30 mins and allowed to cool to room temperature before scanning. For the baked films, the samples were loaded inside the Linkam stage as described for the transistor devices and the morphology was scanned 12 hours of uninterrupted heating under nitrogen.

4.2.4 OFETs fabrication and characterization

For the bottom gate bottom contact devices, a heavily n-doped Si wafer with a 300 nm SiO_2 surface layer (capacitance of 11 nF/cm^2) was employed as the substrate with Si wafer serving as the gate electrode and SiO_2 as the dielectric. The gold source and drain electrodes were sputtered and patterned by photolithography technique. The device channel width and width used for all the measurements were 1000 μm and 100 μm, respectively. For the octadecyltrichlorosilane modification, the silicon wafer (with Au bottom contact) was first cleaned with hot piranha solution (H_2SO_4 (98%):H_2O_2 (30% water solution) = 7:3). It was then further subjected to sonication sequentially in water and acetone for 5 min each. After dried in an oven, the silicon wafer was then put in a Petri dish with a small drop of OTS in the center. The dish was then covered and heated in a vacuum oven at 120°C for 3 h, resulting in the formation of an OTS self-assembled monolayer on the surface. The OTS-modified substrates were rinsed successively with hexane, ethanol, and chloroform and dried by nitrogen. The semiconducting blend layer was deposited on the OTS-treated Si/SiO_2 substrates by spin-coating with speed of 3000 rpm for 30 seconds. Polymer solutions were prepared in chloroform, and the concentrations were 20, 10, 7.5, and 5 mg/mL for P1, P2, P3, and P4, respectively. Corresponding blends with the same concentrations

were attained by blending appropriate percentages and allow the mix to stir for at least 30 minutes for complete mixing. The devices were annealed at 200°C in a N_2 glovebox and allowed to slowly cool down prior to measurement. For the bottom gate top contact devices, cleaned silicon wafers were used as the gated substrate and the blend film was spin coated as previously described. After annealing, the coated wafers were brought to high vacuum and Au source/drain contacts were then deposited through a prepatterned shadow mask (channel width of 1500 μm and length of 40 μm) at a rate of 0.8 Å/s to a final thickness of 30 nm.

OFET devices characterizations were carried out using a Keithley 4200 in ambient environment. The field-effect mobility was calculated in the saturation regime by using the equation $I_{DS} = (WC_i / 2L)\mu(V_G - V_T)^2$, where I_{DS} is the drain-source current, μ is the field-effect mobility, W is the channel width, L is the channel length, C_i is the capacitance per unit area of the gate dielectric layer, V_G is the gate voltage, and V_T is the threshold voltage. OFET performances were obtained by applying a gate bias from −60 V to 10V (or 20 V when the devices were heated in the presence of oxygen), with the potential gradient between the source and drain contacts kept at −60 V.

4.2.5 In-situ temperature-dependent measurements

To control the thermal conditions both for FETs characterization and capacitance measurements, the HFS600E-PB4 Linkam stage was used with the heating and cooling rates maintained at 10 °C/ min and the devices were allowed to reach thermal equilibrium and the electronic performance was monitored over time. For the measurement taken under inert conditions, after engaging the probe tips, the Linkam stage capped and the inside chamber was purged with nitrogen gas for at least five minutes before hermetically closing the purge valve. The

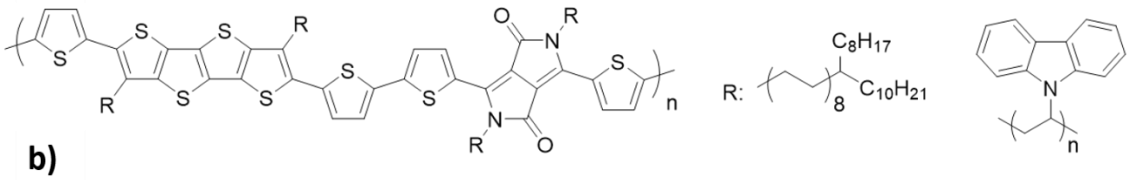
devices where then brought to the appropriate temperature and the electronic properties were recorded every 30 minutes.

4.3 Discovering the influence of molecular weight on high temperature blend performance

4.3.1 Materials selection

To access a wide range of molecular weights with narrows distribution, we selected the highly soluble and highly planar P2TDPP2TFT4, a derivative of the high-performance Corning DPP as the semiconducting polymer for this study (Figure 4.1 a).[138, 139] The high solubility of the conjugated polymer allows us to access molecular weights (M_n) ranging from ~20 kDa up to ~100 kDa without greatly sacrificing processability and electronic performance. The nomenclature of the studied molecular weight distributions follows previous reports on the synthesis and characterization by Niu et al.[138] as shown in Figure 4.1 b. This DPP derivative was also selected for our blending analyses because from the UV-Vis absorption spectra, it has been shown that with the increase in molecular weight, the aggregation shows to plateau beyond the M_n ~50 kDa (P2). The inter-chain interaction *0-0* vibronic peak near 760 nm shows to reach the maximum in P3 (M_n ~77 kDa) and no further increase in P4 (M_n ~93 kDa). This was in agreement with previous reports on the MW-dependent chain folding nature of conjugated polymers.[140-142] This behavior allows us to probe the impact of molecular weight on the miscibility and thermal stability while excluding the contribution from the pre-aggregation of the semiconductor, especially when reaching high molecular weights. For the high Tg matrix polymer we selected PVK, a previously studied highly soluble and readily processable host for the formation of interpenetrating high-performance blend films.

a) P2TDPP2TFT4 PVK



b)

Abbreviation	M_n	M_W	PDI	M_p
P1	19700	31300	1.59	24100
P2	49900	97800	1.96	71400
P3	77300	207300	2.62	133300
P4	93700	183200	1.96	150500

Figure 4.1. Materials selection for the impact of molecular weight on thermal stability. a) Molecular structure of the semiconductor and the insulator used in the blends. b) Molecular weight distribution of the studied fractions of the semiconducting polymer.

4.3.2 Transistor performance demonstration

To readily probe the influence of molecular weight on thermal stability in the semiconducting polymer blends, we fabricated transistor devices in accordance to our previous reports and compared the behavior of the four blends of P2TDPP2TFT4 under constant thermal stress at 150°C in ambient air. Figure 4.2 a) shows the designed blend morphology to attain thermal stability and b) shows the field-effect transistor device architecture. We first compared P1 and P2 based blends to probe the effect of doubling the M_n value on the blend behavior. The transistor characteristics revealed that P2/PVK blends performed better than those of P1/PVK in terms of charge carrier mobility and S/D current values. This observation was not surprising since the parent semiconductors have shown a similar trend. Surprising was the differences in thermal stability when the transistor devices were baked to 150°C for 3 hours. The electronic performance started to drop drastically in the case of P1/PVK with increasing baking time while P2/PVK remained extremely stable as shown by the excellent overlap of the transfer curves (Figure 4.2 c). Figure 4.3

shows changes in the ON current and the hole mobility with increasing baking time. After 1 hour of heating, the P1/PVK pair could barely exhibit the turn-on behavior. Conversely, the P2 pair maintains ON to OFF ratio as high as 10^5, a threshold voltage around -2.0 V, and hole mobility approaching 1.0 cm^2/Vs. Minimal fluctuations could be observed in the OFF current as the carrier density and shallows traps could thermally vary, nonetheless, the P2/PVK could maintain excellent charge transport even after 3 hours of baking. Similarly, all the high molecular weights fractions showed to yield thermally stable transistors devices from their blend films. Thermally stable transfer curves obtained from P3 and P4 blends are shown in Figure 4.4. This drastic instability observed in the P1 blend pair was thus intriguing and probed further analysis on the impact of M_n on the resulting blends. A quick conclusion at this stage was that the higher molecular size of the semiconducting component, the better the thermal stability of resulting blend films. In the following sections we explore the underlying factors towards such behavior.

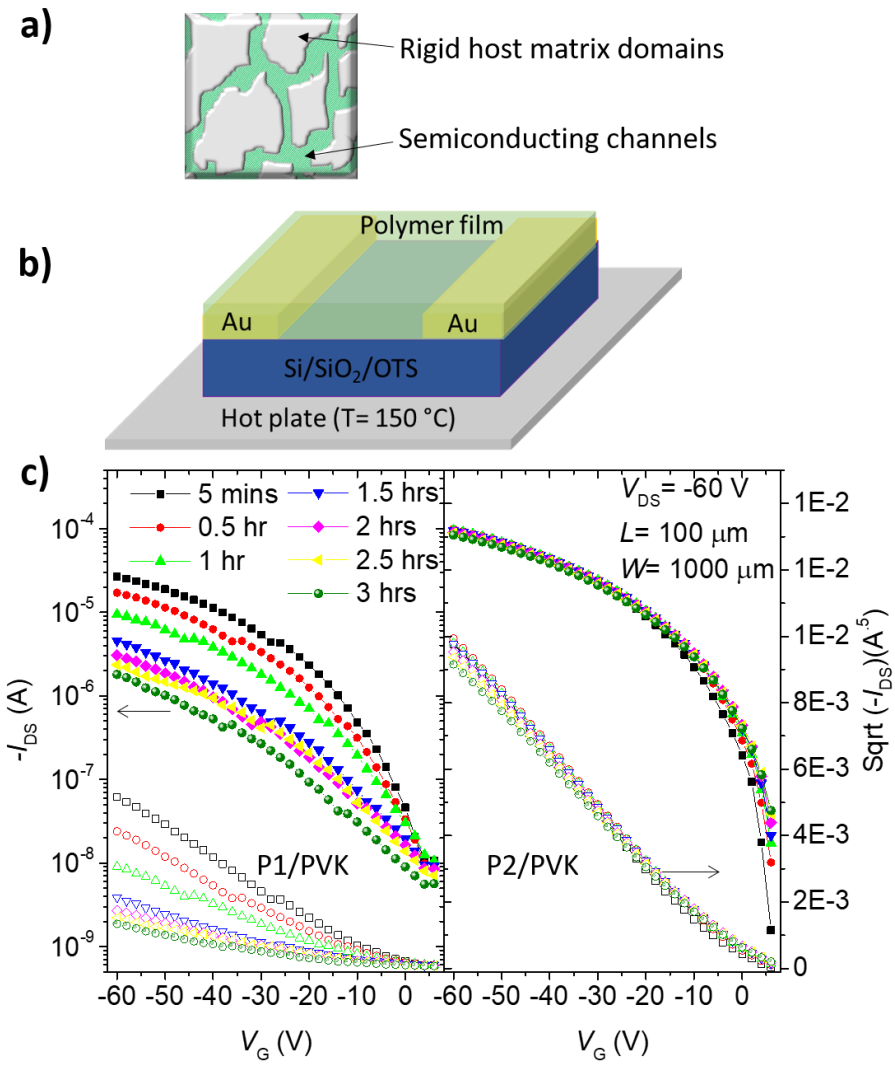


Figure 4.2. Demonstration of the impact of molecular weight on blend performance. a) Bottom-gate bottom contact transistor device architecture used for in-situ bake test. b) Engineered blend morphology for thermally stabilized films in which crystalline domains of the semiconductor are uniformly dispersed within the rigid matrix. c) Representative characteristic transfer curves from transistor devices baked for 3 hours at 150°C in ambient environment. An excellent overlap is observed in the P2/PVK blend pair while an obvious decline in the semiconducting properties was observed in the P1/PVK analogue.

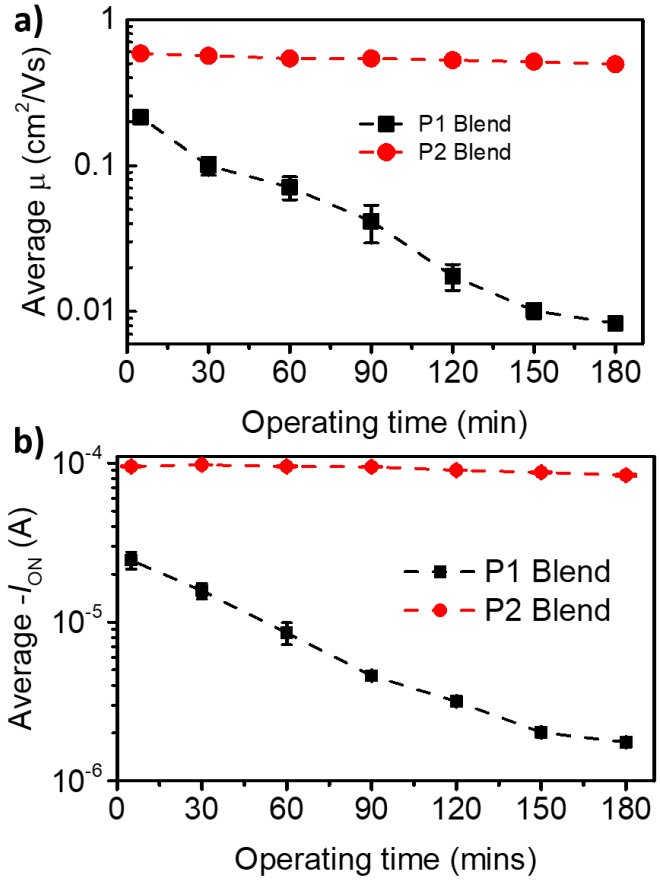


Figure 4.3. Comparison of hole mobility and ON current between P1 and P2 based blend films with increasing baking time.

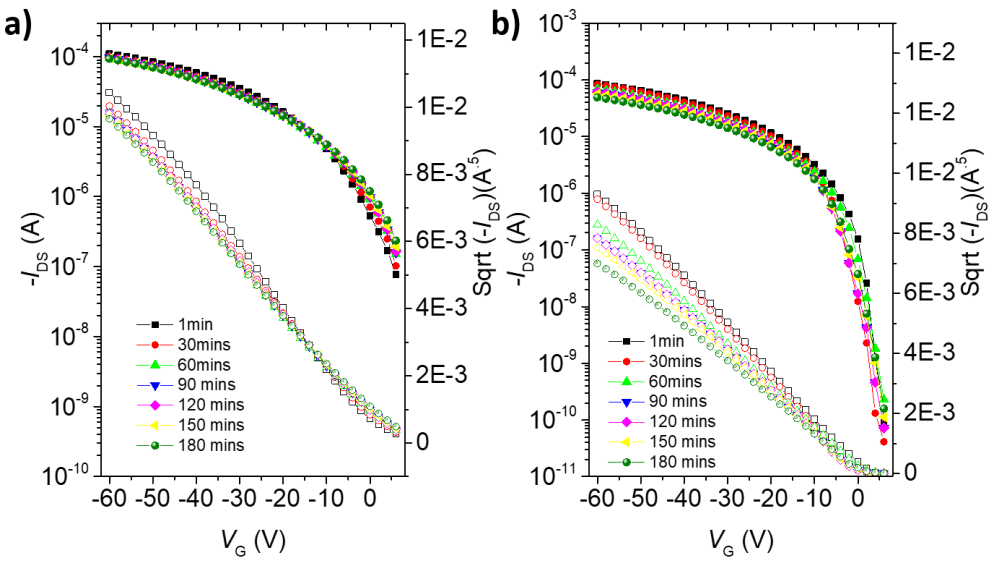


Figure 4.4. Transfer curves from P3 and P4 blend films with PVK under constant thermal stress at 150°C in ambient air.

4.4 Influence of molecular weight on blend morphology engineering

To understand the underlying differences caused by the molecular weight variation, we first probed the thin film morphology of P1, P2, P3, and P4 blends with PVK in the 40 (semiconductor)/60 (insulator) previously reported optimal blend ratio. In this chapter we became interested in the unexpected differences that showed to rise when the molecular size of the semiconductor component was doubled. We expected that the size of the polymer will influence its coiling nature, but we are interested in how this behavior will influence our blending strategy. Since microscale morphological behavior has served thus far served as the starting point of the thermal stabilization in our blend films, we first investigated the effect of the conjugation length on the blend morphology, then probed how the formed morphologies respond to thermal stress.

4.4.1 Impact of molecular weight on miscibility

We imaged the blend films of the four different molecular weights of P2TDPP2TFT4 with PVK via atomic force microscopy (AFM). We first maintained the blending ratio and processing

conditions the same for all samples to only probe the effect of the molecular weight. The AFM images revealed that the lower M_n, P1, forms isolated domains dispersed within the insulator while the increase in molecular weight leads to the formation of a uniform bi-continuous network of the conjugated polymer within the matrix (Figure 4.5). To rule out the possibility that the micelles formation was due to the inappropriate blend ratio in the case of P1, we decided to vary the blend content from 10% P1 up to 80% P1 in the PVK blends. Regardless of the blending ratio, however, the domains size of P1 showed to merely increase in size with increasing content in the blend as shown in Figure 4.6, but no evidence of the spinodal-like morphology was observed.

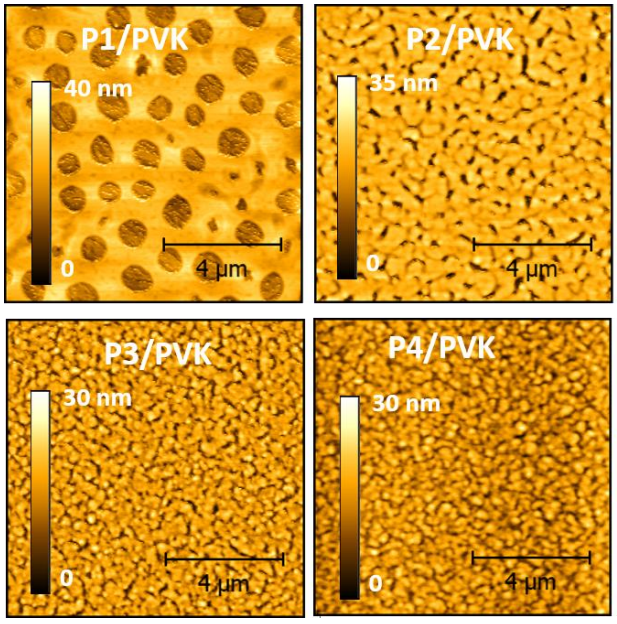


Figure 4.5. Influence of molecular weight of the blend morphology. AFM height images showing morphology evolution with increasing molecular weight in PVK blends.

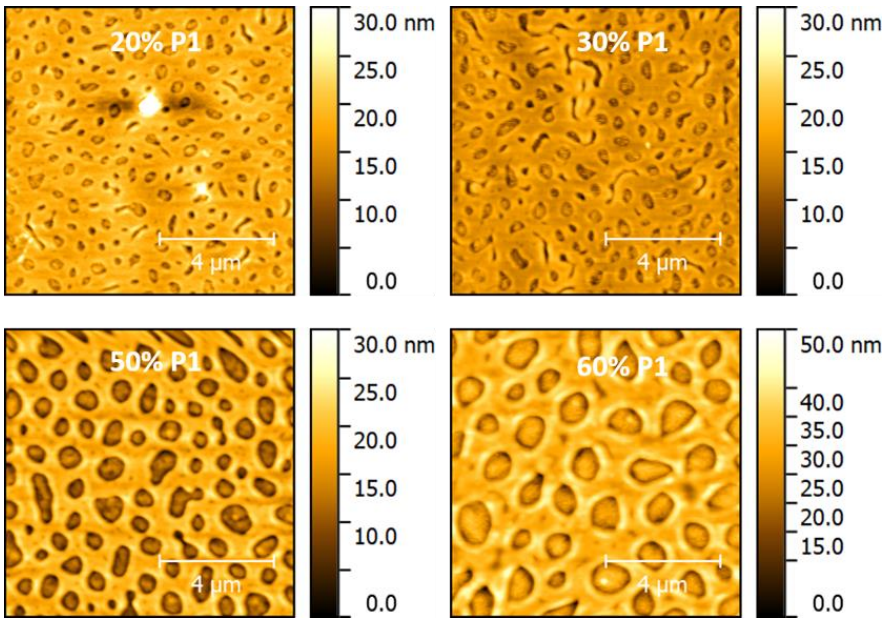


Figure 4.6. Nucleation and growth behavior in low molecular weight polymer blends. Morphology evolution of in P1 blends with varying blend ratio indicating the nucleation and growth behavior.

This micelle formation in P1 blends suggested a nucleation growth morphology behavior. This morphology tells us that there is essentially no mixing between the low M_n component and the host matrix. The isolated micelles are laterally separated from the host across the entire film as illustrated in Figure 4.7 a), following the classical description of the nucleation and growth mechanism.[135] Such description is shown Figure 4.7 b) where we compare the line profiles extracted from the AFM images of P1 blend film (top) and P2 blend film (bottom) to the generalized illustration (insets). The insets show the expected composition versus distance profiles describing the nucleation and growth morphology in comparison to the spinodal decomposition morphology. In the case of spinodal decomposition, a maze-like microstructure with columnar domains that extend through the entire film bulk are formed. For the nucleation and growth morphology formation, isolated domains of one component are formed which yields the discontinuous line profiles as observed for P1 blends.

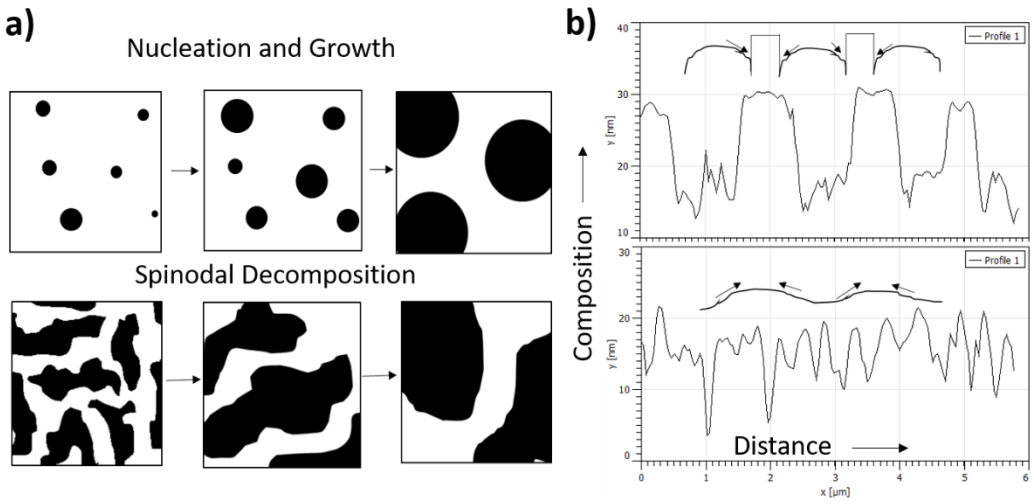


Figure 4.7. a) Illustration of nucleation and growth morphology compared to spinodal decomposition. b) Representative line profiles extracted from the AFM height images of P1/PVK and P2/PVK blend films. P1 films exhibit isolated cylindrical micelles across the hole film indicative of a nucleation and growth composition distribution. The insets represent the classical representative of the blend composition distribution across the film in comparison to the profiles.

This lack of the targeted confinement could also be mirrored in the UV-Vis absorption spectra of the blend films as shown in Figure 4.8 and Figure 4.9. First by comparing P1 and P2 solution absorptions to corresponding PVK blends, we observed that there was no evidence of pre-aggregation in both cases as the spectra of the pristine polymers overlapped very well with those of the blends. In accordance to previous reports on the P2TDPP2TFT4 polymer, the studied molecular weights exhibit essentially the same effective conjugation lengths and similar aggregation behavior. [138] We were thus confident that any differences that we see in our blend films arise from the interaction behavior between the conjugated polymer and the host matrix. As expected, both polymers show to improve in ordering when in solid state compared to the solution state and significant differences arose when the blends were processed into thin films. P1-blend's absorption showed to remain overlapped with the pristine polymer film while P2 blend absorption spectrum exhibit further enhancement in the inter-chains ordering (Figure 4.8 a, b). In the case of

P1, no redshift or change in vibronic peak intensities could be observed upon blending indicating the lack of an induced confinement and ordering. Conversely, for high M_n ranges, the *0-0* vibronic peak intensity increased significantly as an indication of improved of chain planarization and more ordered packing as shown in Figure 4.8 c, d and Figure 4.9. It was thus clear that the shorter polymer chains preferred to simply form isolated nucleates while the longer analogues could be disentangled and become physically confined by the matrix. This was also in good agreement with previous reports, for instance by Ye et al.,[143] which proved that lower molecular weight would lead to poorer interaction in polymer-polymer systems. This poor miscibility and nucleation morphology also came to explain the lower electronic performance observed for P1 blend films as the isolated domains lead to ineffective charge carrier delocalization.

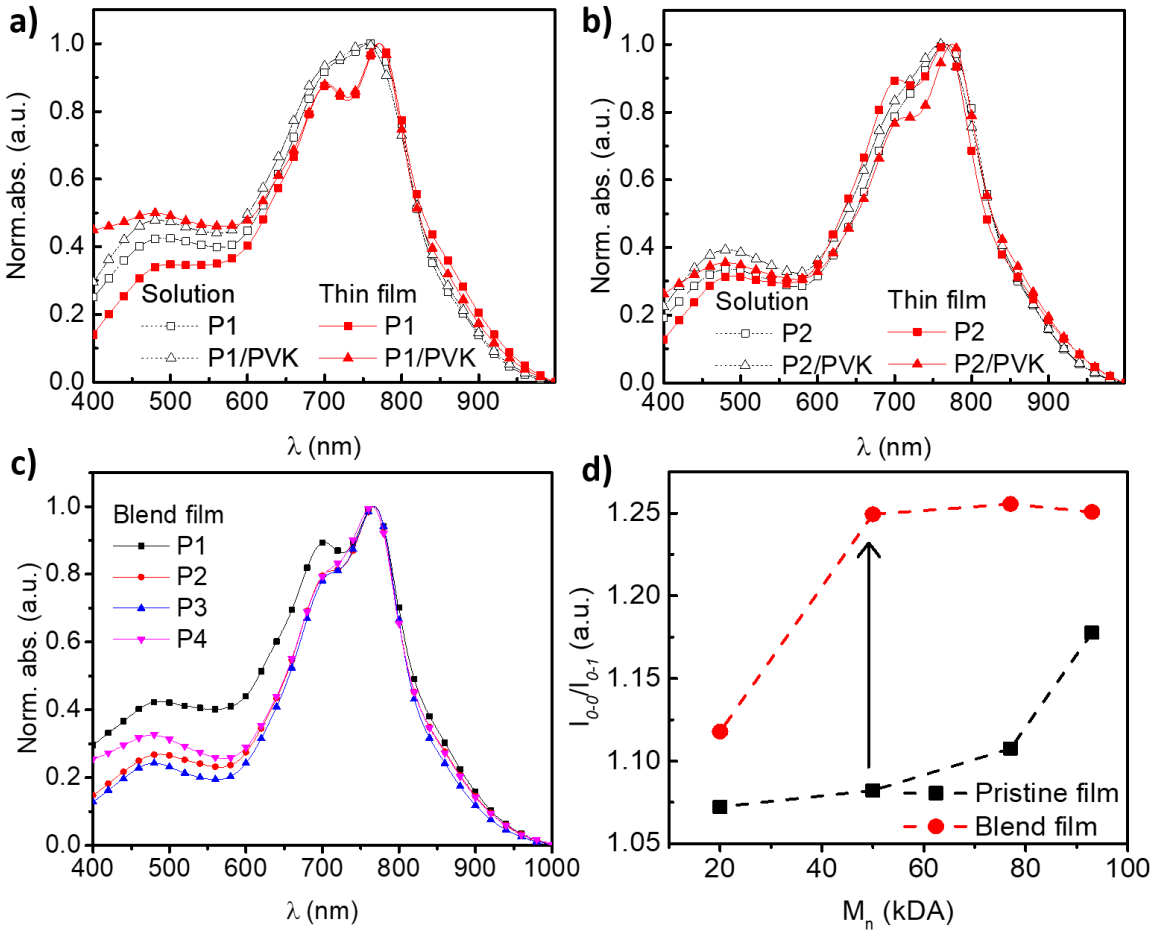


Figure 4.8. UV-Vis absorption comparison with varying molecular in the blends. a) b) Normalized absorptions P1 and P2 solutions and films compared to corresponding PVK blends. c) UV-Vis absorption spectra comparing the PVK blend films with different molecular weights of the semiconducting component. d) Extracted *0-0*/*0-1* vibronic peaks ratio from normalized absorption spectra.

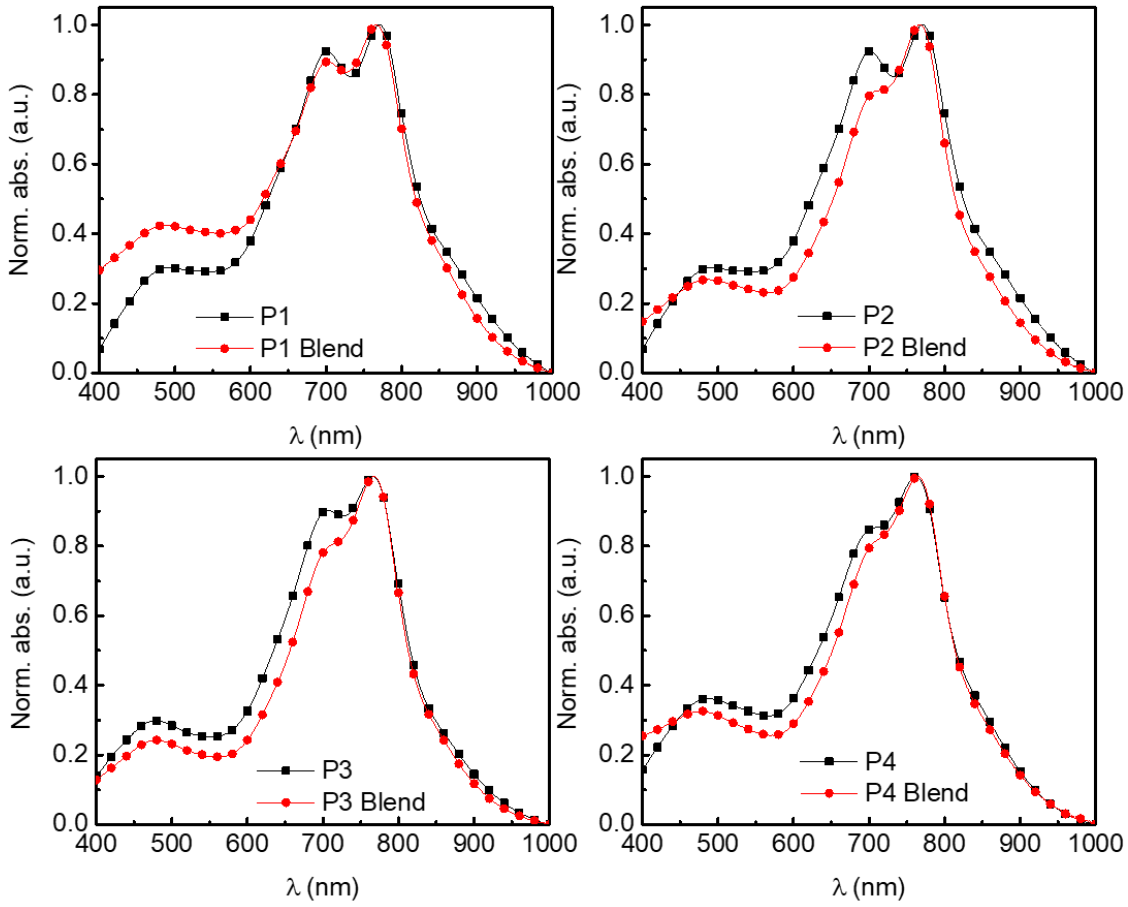


Figure 4.9. UV-Vis absorption spectra comparing pristine films of the studied M_n ranges with corresponding PVK blends. The induced ordering and close packing indicated by the increase in the intensity of the vibronic peak around 760 nm.

We then became interested in whether this behavior is specific to the current blends system. To probe whether this poor miscibility in low M_n ranges could be observed when used other building blocks, we selected two other polymers, DPP-P2 and BDOPV, that we previously reported.[108] We then obtained different molecular weight fractions through solubility tunability in different solvents. That is, the low M_n fractions were selected as the portions that showed excellent solubility in chloroform while the higher M_n fractions were the portions that required the solution to be heated up to 50°C in order to dissolve. Note the poorer distribution control in comparison to the studied P2TDPP2TFT4, but these batches served the purposes of the proof of concept. Figure

4.10 shows the molecular structures of these two polymers as well as the resulting thin film morphologies when different extraction fractions were used to form the blend films. A clear phase separation into round micelles could be observed in both cases when lower M_n ranges were used in PVK blends while the corresponding higher M_n fractions exhibited improved mixing which could be credited to the thermal stability that we previously observed in these blend systems. This apparent generality of the nucleation morphology in low M_n fractions of the semiconducting polymers thus came to support our hypothesis that the blend morphology during the spinodal decomposition depends heavily on the crystallization behavior of the conjugated polymer.[135] Low molecular weight fractions tend to have much better interchain interactions and tend to quickly crystallize into micelles upon blending. It was found as though the low M_n fractions could not sense the presence of the host matrix during the film formation. This observation agreed with the previously discussed high interaction parameter demonstrated in low molecular weight polymer blends.

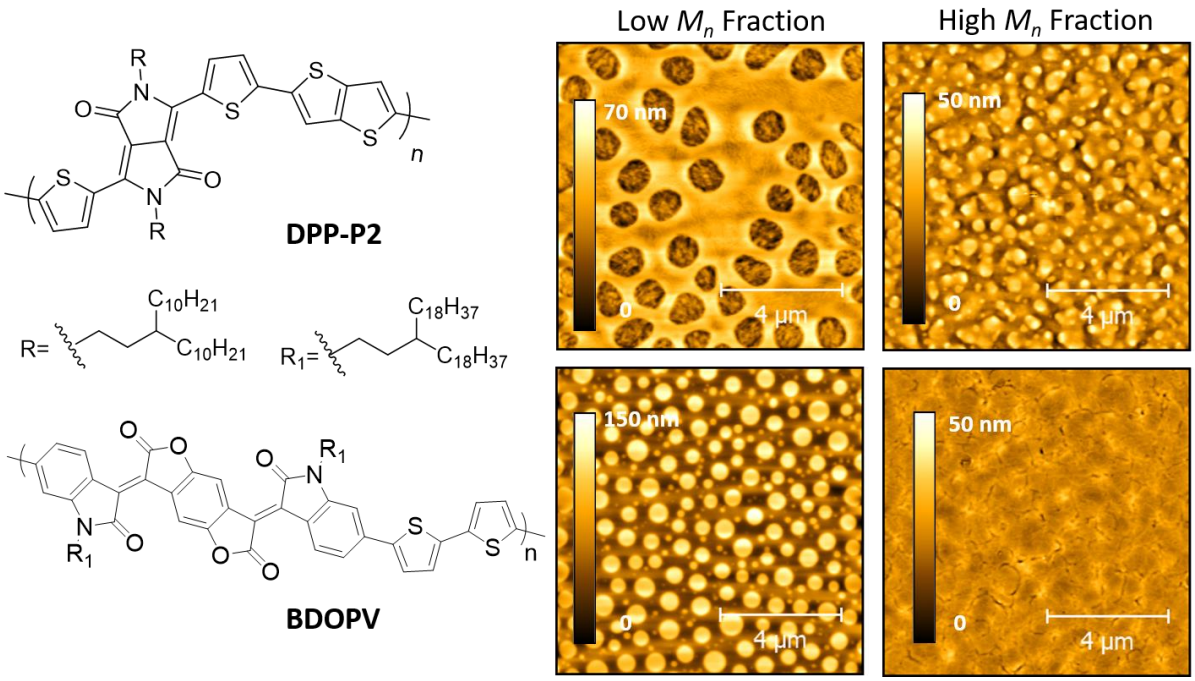


Figure 4.10. Molecular weight dependence of blend morphology. Chemical structure of additional building blocks and corresponding morphologies when different molecular weights are blended with PVK.

Finally, we wanted to probe the impact of varying the molecular weight of insulator component especially when the size of the conjugated polymer is smaller. We hypothesized that the mostly amorphous PVK would have minimal impact on the crystallization process during the film formation. If that was not the case, one would expect that by tuning the size of PVK, the spinodal morphology could eventually be obtained in P1 blends. We then synthesized different M_n ranges on PVK itself and blended them with P1 to probe whether the molecular weight of the insulating host would govern the blend morphology. In agreement to our hypothesis, regardless of the insulator's molecular weight, the nucleation and growth morphology showed to persist even when the M_n was changed from 7 up to 50 kDa. As observed from the AFM images in Figure 4.11, when both components have small molecular weights, smaller domain size are formed most likely due the increased competing micelle formation. With the increase in the insulator's M_n, the

semiconductor domains showed to increase in size but with no evidence of improved miscibility or formation of the spinodal-like morphology. We find that the morphology is much more governed by the conjugated polymer since, regardless of the PVK size, the semiconducting polymer is still able to crystallize into isolated micelles.

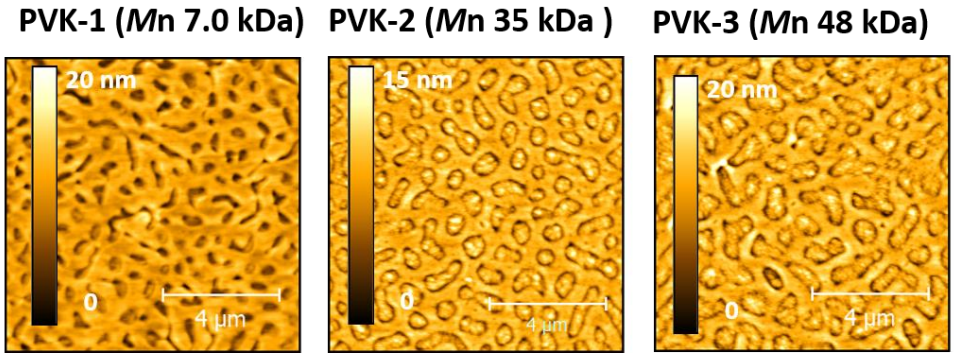


Figure 4.11. Morphology of P1 blends with varying M_n of PVK. In all cases, the micelles formation persists regardless of the size of the insulator.

4.4.2 Impact of miscibility on thermal stability

Up to this point it was understood from the morphology analysis that at low molecular weights, the miscibility became less favored. Instead of forming the interpenetrating network with the insulator, the highly crystalline P1 polymer nucleated and formed isolated micelles which grew with increasing volume fraction with no indication of spinodal decomposition behavior. This was indeed in good agreement with classical description of the Gibbs free energy of mixing of polymer systems.[135, 144] We were then intrigued by the understanding of why the nucleation and growth morphology observed in P1 blends resulted into drastically unstable electronic properties. Revisiting the differences between these two morphology formation mechanisms, we were able to pinpoint the stability differences. Table 4.1 shows the differences between nucleation growth and spinodal morphologies in terms of stability. Though both cases are due to phase separation between

the blend components, the nucleation morphology is prone to constant variation while spinodal is permanent. The constantly increasing nucleates size accompanied with a positive diffusion coefficient suggest that such morphology would be unstable and that the resulting transistor devices would suffer from the fluctuating conformation in the semiconducting channel. We believe that such fluctuations are the main reason why the transistor devices based on P1 blends exhibit an unstable behavior against thermal stress.

Table 4.1. Comparison between nucleation and growth and spinodal decomposition morphological behaviors in binary polymer blends.

Morphology	Nucleation and growth	Spinodal decomposition
Size of phase separated region	**Increases with time**	**Size constant**
Diffusion coefficient	Positive	Negative
Phase structure	Separated	Separated
Activation energy	Required	Not required
Thermal stress	**Unstable**	**Stable**

To visualize these differences in morphological stabilities, we monitored the AFM height images before and after baking of the blend thin films. Since the changes could be at the nanoscale and take prolonged aging to be detectable, we subjected the blend films to 220°C heating (near the Tg of the matrix polymer) for 12 hours under nitrogen. In these thermal conditions, we expect that any morphological changes would be given enough thermal energy to occur and the differences between the two crystallization mechanisms could be readily mirrored. The AFM height images revealed that, as predicted, for the nucleation morphologies where there's no mixing between the two polymers, the morphology changes during the baking process. Compared to the annealed film, the baked film of P1/PVK blend showed a de-mixing behavior where the insulator domains started to begin to delaminate from the surface as shown in Figure 4.12. An obvious expansion in the film

could be observed which came to support the observed unstable electronic behavior in the transistor devices. Conversely, no obvious morphological changes could be detected when the M_n of the semiconductor was increased. The established mixed spinodal morphology could be retained which came to support the stability observed for P2, P3, and P4 blend pairs.

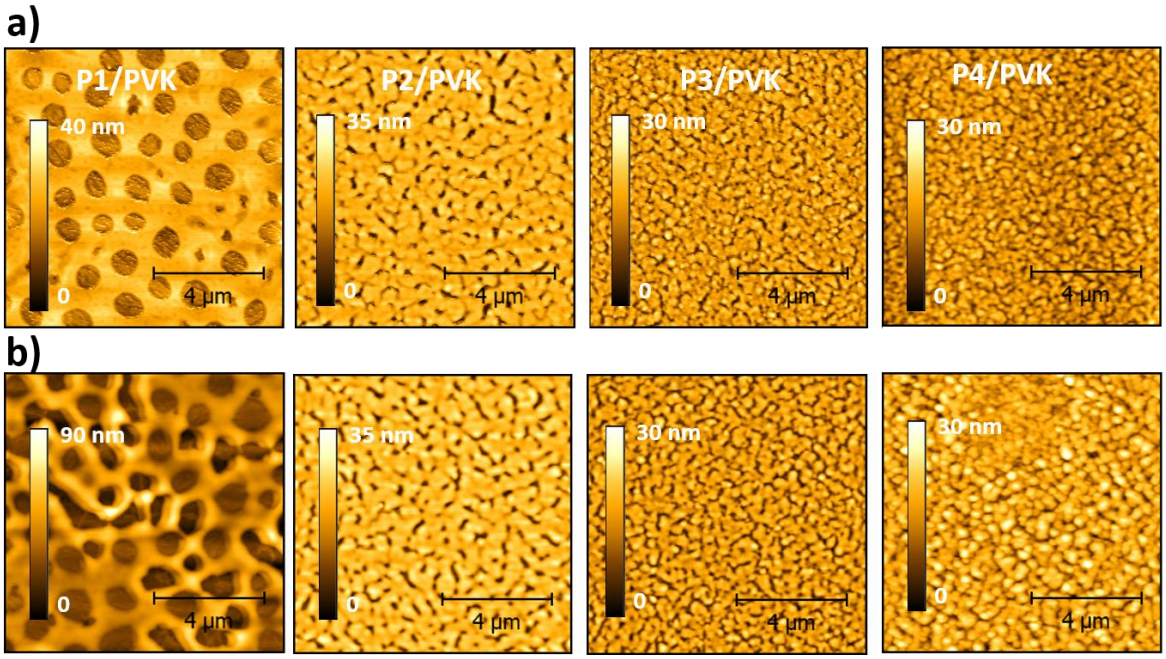


Figure 4.12. AFM height images of blend films a) before and b) after baking near the Tg of the host matrix for 12 hours. An obvious expansion accompanied by a de-mixing is observable in the case of P1 while no significant morphological changes could be observed in the higher Mn based blends.

4.5 Molecular weight guided thermal stability in transistors

To accurately mirror these top-interface morphology differences, we fabricated transistor devices in the bottom-gate top-contact (BGTC) structure. In this devices architecture we could accurately compare the formed morphologies and exclude any possibilities of a formation of vertically-separated thin layer at the bottom interface. A partial phase separation was expected to be the reason why the P1/PVK blend even exhibit any starting charge transport given the formation

of large and highly disconnected domains as shown by the AFM images. Consequently, we fabricated the devices by processing the films the same manner as the AFM samples but extracting the charge mobilities when the source/drain contacts are deposited directly on the top interface as shown in Figure 4.13.

We the repeated the baking analysis as we discussed above where the blend-based devices are heated to 150°C, first under inert and then in ambient conditions. We constantly monitored any changes in corresponding transfer characteristics up to 12 hours. In the BGBC devices, poorer electronic performance was indeed observed in the P1/PVK pair as expected from the discontinuous morphology. In addition, this pair showed unstable electronic performance once the devices were baked over a long period of time (Figure 4.13.a). For the mixed blend pairs, extremely stable devices could be realized even after 12 hours of heating at 150°C as shown in Figure 4.13.b-c). An excellent overlay of the characteristic transfer curves of the transistor devices based on PVK blends with P2, P3, and P4 monitored for 12 hours of heating could be obtained indicative of excellent thermal stability for the high molecular weight fractions. A similar stability behavior could be observed for the devices studied under open air as shown in Figure 4.14. These transistor performances under constant thermal stress were viewed as a direct demonstration of a molecular weight guided stabilization of high temperature organic electronics.

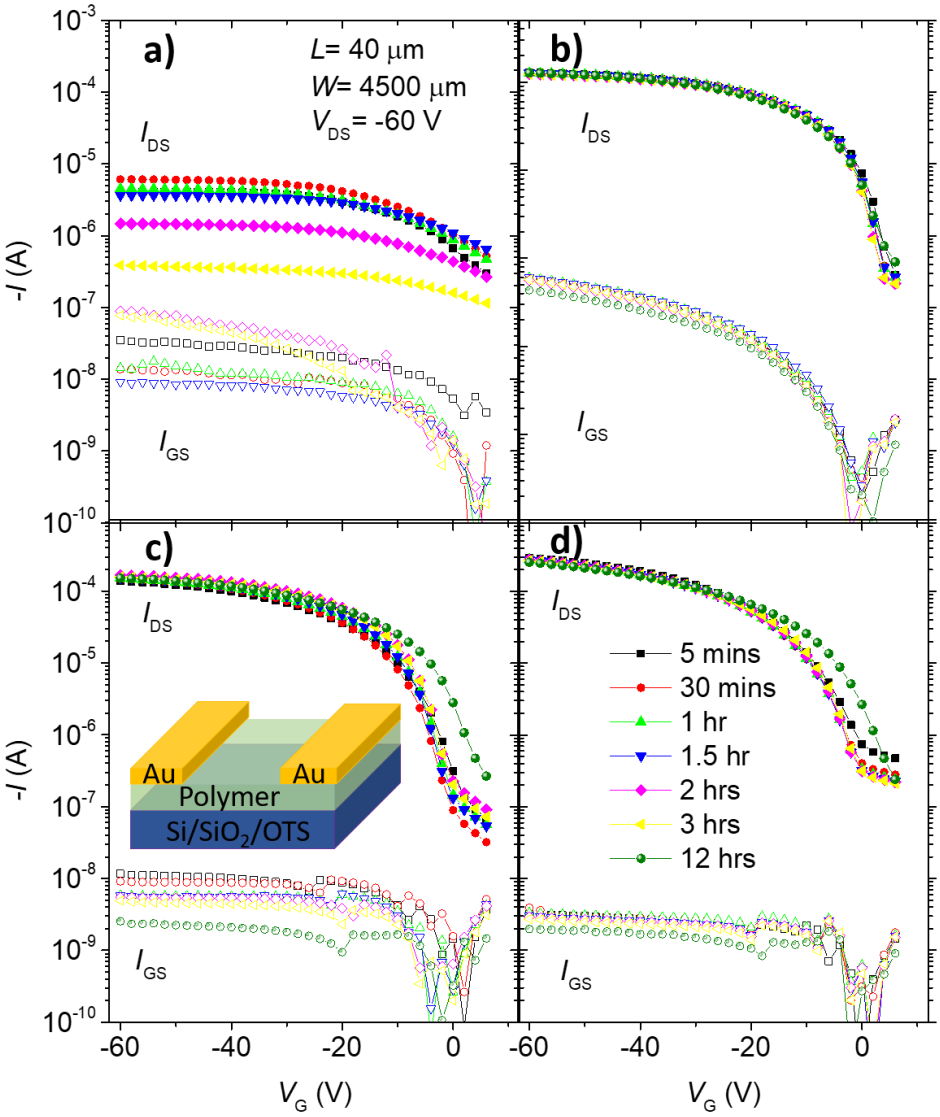


Figure 4.13. OFET performance of blend devices based on PVK blends with a) P1, b) P2, c) P3 and d) P4 when baked at 150°C for 12 hours under inert conditions. P1/PVK blend films showed declining performance as the baking time increased. The other pairs exhibit nicely overlapping transfer characteristics with extremely stable ON currents and relatively low gate currents. Minor fluctuations could be observed after 12 hours of measurement and could be associated with impoverished contact with the measurement probes.

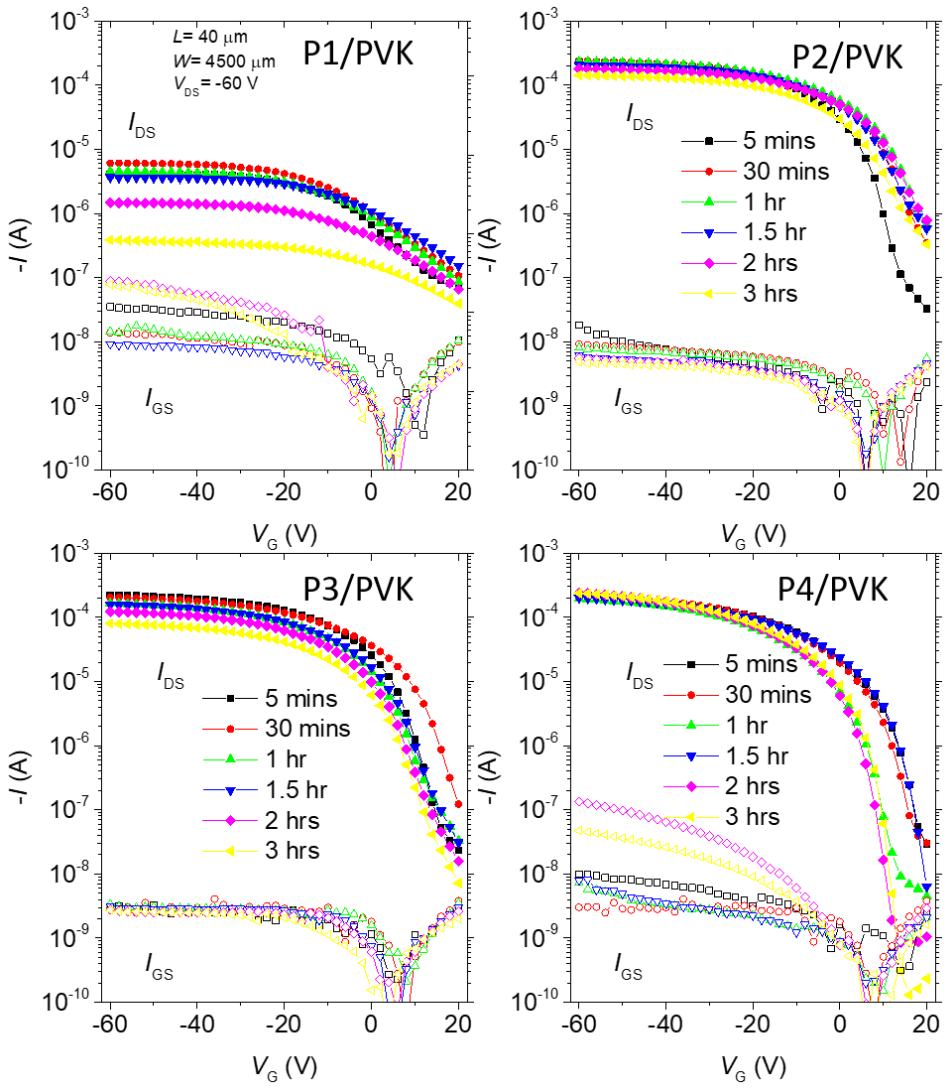


Figure 4.14. Transfer curves of the bottom gate top contact transistor devices measured when the studied blends were baked at 150°C in the open air. Notice a relative slight shift in the threshold voltages most likely due to the presence of oxygen during the measurement.

4.6 Conclusions

To conclude this chapter, we carried out a detailed analysis on the impact of molecular weight on the miscibility and thermal stability of high temperature semiconducting polymer blends. We found the following: 1) lowering the molecular weight of the conjugated component diminishes the compatibility between the blends and leads to a nucleation type of morphology. 2) Despite the presence of a large amount of the high Tg matrix polymer, the nucleation morphology

is still prone to constant domain size change and leads to unstable thin film devices. 3) The formation of spinodal-like mixed morphology leads to a permanent rigidification of the semiconducting domains amongst the matrix host and yields thermally stable transistor devices. The current study revealed that in the quest for high performance and thermally stable semiconductor-insulator combination, one ought to consider the miscibility of the system and the latter is highly dictated by the more crystalline component. The molecular of the semiconducting polymer should be intentionally selected to be higher to ensure the mixing in the physically compatibilized morphology; without this morphology, both poor starting performance and diminished thermal stability will result.

CHAPTER 5. POLY(LADDER-IMIDES): MATRIX ENGINEERING FOR EXTREME TEMPERATURE POLYMER BLENDS

5.1 Introduction

The previous chapters have outlined the materials design principles as well as the processing routes towards the realization of thermally stable operation in transistors using semiconducting polymer blends. We now ask the question of what the temperature limits of our design are. That is, how high can such polymer blends go? The answer to this question is essentially rooted in two factors: i)what the decomposition temperature of the semiconducting component is, and ii) what the confining power of the insulator is. The decomposition temperatures of most conjugated polymers are usually between 300 and 400°C.[57, 73, 145] However, it is not known how close to the decomposition temperature we can heat these materials and maintain them functional. That is, at which temperatures are the main chains still capable of transporting the charge carriers. Additionally, given the observed thermal expansion, at what temperatures would the effective π-π stacking essentially is not known. However, in accordance to our discussion, if the disordering among the semiconducting domains is mitigated, high temperature operation can be attained in extreme conditions. We thus turn our focus more on the thermal stability of the insulating host and its confining abilities. Fortunately, as mentioned above, polymers constitute one of most thermally durable class of materials.[146] For instance polyimides have been widely studied as robust plastics for various applications.[147] Several design strategies have been used to yield extremely stable polymers.[148-153] In principle, to design thermally robust polymers, the following strategies are normally utilized: 1) Increasing the polymer backbone rigidity and planarity commonly achieved by introducing *para*-substituted rings; 2) Excluding any flexible linkages and incorporating bulky side groups to decrease rotational freedom; 3) Incorporating high

energy bonds and resonance stable functional groups; 4) Increasing the molecular weight of the polymer; and 5) Crosslinking the polymer matrix.[154] In our discussion above, we utilized polyimide-based insulator which encompasses most of these design principles. We now direct our attention to how these five principles can be utilized to rationalize ways to improve the properties of our insulators.

Matrimid was discussed in both chapter two and three as a promising host matrix that is both thermally robust and readily solution processable. In terms of pushing our blending design to its thermal limit, we become limited to near 320°C which is the glass transition temperature of this polyimide. It thus become of our interest to investigate its structure in order to find or design novel alternatives. From the design criteria for a thermally robust polymer we can pinpoint two key aspects especially in terms : i) excluding any flexible linkages and incorporating bulky side groups to decrease rotational freedom; and ii) incorporating high energy bonds and resonance stable functional groups. Looking at its molecular structure with the most hydrophobic highlighted, this exemplary polyimide contains several carbon-carbon bonds in contrast to utilizing high energy bonds (Figure 5.1). Though the highlighted hydrophobic moiety is by design attached in accordance to the preferred *para* position of the phenyl ring, it still poses a considerable degree of rotational freedom relative to the imide linkage. Besides, conformational fluctuations along the cyclopentane group are also undesired.

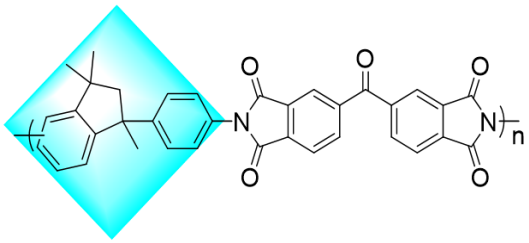


Figure 5.1. Chemical structure of Matrimid, a high Tg matrix polymer for high temperature semiconducting blends.

To improve on the thermal properties of Matrimid, this chapter explored the possibilities of substituting Matrimid with a ladder-type copolymers as reported by Abdulhamid et al.[155] By using the catalytic arene–norbornene annulation (CANAL) approach,[155-159] the authors took advantage of the polycondensation of "CANAL" ladder diamines with diphthalic anhydrides to design and synthesize a series of polyimides with different degrees of rotational freedom around the imide linkages. These polyimides exhibit extremely stable behaviors, i.e. they do not have any thermal transitions up until their decomposition temperatures which are as high as 500°C. In accordance to the design principles mentioned above, this excellent thermal stability can be credited to the incorporation on fused norbornene-based rings which reduce the degree of rotational freedom. In addition, the CANAL unit is sufficient to enable the solution processability of the resulting polyimides. The position of the alkyl groups on the CANAL block were also used a vital tool to tune the porosity on these copolymers for gas separation.

In other reports, it has been found that this increased porosity was beneficial towards lowering the dielectric properties of the polyimide membranes,[106] which for the sake of the current discussion will later become relevant as we target low capacitive insulators in our blends to conserve efficient charge transport in the resulting semiconducting blends. Recall from chapter two that the imide-based matrices exhibited the lowest electronic performances when used to form semiconducting blends. We attributed such lowered performance to potential charge trappings

introduced by the carbonyl groups, readily polarizable groups, that could render such matrices highly capacitive and detrimental to efficient charge delocalization. Abdulhamid et al. reported the polycondensation of the CANAL group with 4,4′-(hexafluoroisopropylidene)diphthalic anhydride to synthesize the copolymer herein labeled CANAL-F-PI as shown in Figure 5.2.[155] In addition to using the fused rings for the polycondensation, fluorinated units were introduced in the anhydride half. Serendipitously, the introduction of fluorine atoms remains one of the most common strategies towards lowering the dielectric properties in polyimides.[149, 153] This lowered capacitive behavior is commonly associated to the poor polarizability of fluorine atoms. In our search for low dielectric constant insulator, we thus envision the substitution of carbonyl groups with the hexafluoroisopropylidene counterparts will benefit the electronic properties of our polymer blends in two ways: i) by improving the hydrophobicity on the anhydride unit therefore rendering the matrix more compatible with the hydrophobic conjugated polymers; ii) by minimizing the charge traps density and therefore leading to more effective charge transport in the blend films. In combination with the inherent porosity mentioned above, we believe the ladder-imide copolymers will serve as improved candidates for our high temperature semiconducting blends.

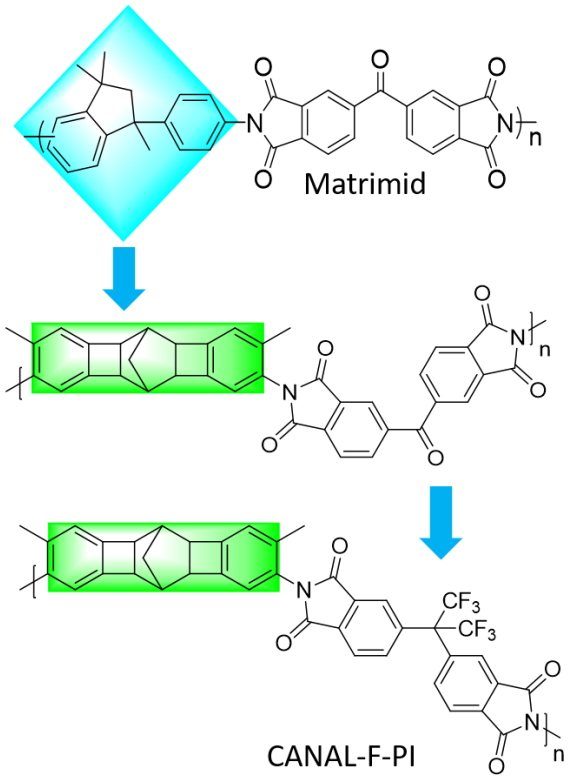


Figure 5.2. Molecular design approach towards thermally robust polyimides for high performance thermally stable semiconducting polymer blends.

In this chapter, we thus investigated the electronic performance of the semiconducting polymer blends using CANAL-F-PI as an improved version of the Matrimid parent that we covered in the previous chapters. We first measured the capacitance of the pure matrix films to compare the newly designed matrix to our previous candidates. We showed that ladder copolymer formation could halve the dielectric constant in comparison to Matrimid. We then fabricated transistor devices using the ladder matrix as the host to probe the benefit lower the dielectric properties. We also investigated the predicted compatibility in the blends gained from the use of fluorinated groups by comparing the blend morphologies to that of Matrimid blends discussed above. Finally, we tested the thermal stability of the resulting blends devices as part of the search

and design for high temperature, high performance, semiconducting polymer blends, and electronics made thereof.

5.2 Experimental

5.2.1 Materials

Matrimid® 5218 (MI) was purchased from PolyK Technologies and purified by precipitation, filtration, washing with methanol and drying before use. Is-P1 was synthesized and purified as reported in our previous works.[73, 108] High purity Au and Al pellets were purchased from Kurt J. Lesker Company and subject to high vacuum before deposition. CANAL-F-P1 was synthesized as previously reported [155] Briefly, to a flame-dried 50-mL glass pressure tube were added bromoaniline (1 eq.), $Pd(OAc)_2$ (0.01 eq.), PPh_3 (0.02 eq.), Cs_2CO_3 (1.0 eq.) and 1,4-dioxane. After the pressure tube was flushed with nitrogen for 5 min, norbornadiene (NBD , 0.5 eq.) was added. The mixture was then stirred at 150°C for 24 h. The mixture was cooled to room temperature and passed through a thin layer of Celite to remove inorganic salts. The filtered solution was concentrated and then washed with methanol to obtain a brown solid. The crude solid was purified by silica gel column using dichloromethane: petroleum ether/1:1 as an eluent to yield the CANAL diamine in a mixture of syn and anti-isomers as a white solid. Afterwards, to a dry 25-mL reaction tube equipped with a Dean-Stark trap, nitrogen inlet and outlet, and a reflux condenser were added CANAL diamine (1.0 mmol), an equimolar of the dianhydride (1.0 mmol), and isoquinoline (0.1 ml). The reaction mixture was stirred at room temperature for 1 h and the temperature was then raised gradually to 200°C and kept at that temperature for 4 h under a steady flow of nitrogen. The fibrous polyimide was obtained by the dropwise addition of the polymer solution to methanol (300 ml). The resulting solid were filtered and dried in the oven at 120°C. Purification was achieved by re-precipitation from chloroform into methanol and dried at 120°C

in the vacuum oven for 24 h. The blends were formed by mixing chloroform solutions of the conjugated polymer (Is-P1) with the polyimide in appropriate ratio and allowed to stir for a minimum of two hours.

5.2.2 Morphology characterization

The AFM height were obtained using Cypher Asylum AFM and processed through Gwyddion Software. All films were processed on cleaned silicon substrates and film morphology was imaged after annealing and/or baking of the blends. The films were annealed for 30 mins and allowed to cool to room temperature before scanning. For the thickness extraction, a notch was gently created through the polymer film on a silicon substrate and the image was scanned across the notch.

5.2.3 UV-Vis absorption

Samples were prepared by spin casting the chloroform polymer solutions onto cleaned glass substrates. All absorption spectra were collected using a UV/Visible/NIR Cary 3000i spectrophotometer. To compare aggregation behavior between films of pure polymer and corresponding blends, the films of Is-P1 and the blends of Matrimid and then CANAL-F-PI were annealed to 200ºC and slowly cooled down to room temperature inside a N_2 glovebox before each measurement.

5.2.4 Capacitance measurements

To extract the capacitance of the polyimide matrices, ITO-coated glass substrates were first cleaned and dried inside a vacuum oven. A thin layer of the polymers was processed by spin coating and annealed to 200ºC inside a N_2 filled glovebox for 30 mins. Using 1.1 mm x 1.1 mm stainless steel shadow mask, the ITO/PI/Au sandwich structure could be achieved. The capacitance

was then measured using a GW Instek LCR-6100 Precision LCR Meter in the ITO/PI/Au sandwich configuration. The frequency could be varied from 100 Hz to 100 kHz.

5.2.5 OFETs devices fabrication and characterization

For the bottom gate bottom contact devices, a heavily n-doped Si wafer with a 300 nm SiO_2 surface layer (capacitance of 11 nF/cm^2) was employed as the substrate with Si wafer serving as the gate electrode and SiO_2 as the dielectric. The gold source and drain electrodes were sputtered and patterned by photolithography technique. The device channel width and width used for all the measurements were 1000 μm and 100 μm, respectively. For the octadecyltrichlorosilane modification, the silicon wafer (with Au bottom contact) was first cleaned with hot piranha solution (H_2SO_4 (98%):H_2O_2 (30% water solution) = 7:3). It was then further subjected to sonication sequentially in water and acetone for 5 min each. After dried in an oven, the silicon wafer was then put in a Petri dish with a small drop of OTS in the center. The dish was then covered and heated in a vacuum oven at 120°C for 3 h, resulting in the formation of an OTS self-assembled monolayer on the surface. The OTS-modified substrates were rinsed successively with hexane, ethanol, and chloroform and dried by nitrogen. The semiconducting blend layer was deposited on the OTS-treated Si/SiO_2 substrates by spin-coating with speed of 3000 rpm for 30 seconds. Polymer solutions were prepared in chloroform, and the concentrations were maintained to 10 mg/mL. Corresponding blends with the same concentrations were attained by blending appropriate percentages and allow the mix to stir for at least 30 minutes for complete mixing. The devices were annealed at 200°C in a N_2 glovebox and allowed to slowly cool down prior to measurement. For the bottom gate top contact devices, cleaned silicon wafers were used as the gated substrate and the blend film was spin coated as previously described. After annealing, the coated wafers were brought to high vacuum and Au source/drain contacts were then deposited

through a prepatterned shadow mask (channel width of 1500 μm and length of 40 μm) at a rate of 0.8 Å/s to a final thickness of 30 nm.

OFET devices characterizations were carried out using a Keithley 4200 in ambient environment. The field-effect mobility was calculated in the saturation regime by using the equation $I_{DS} = (WC_i / 2L)\mu(V_G - V_T)^2$, where I_{DS} is the drain-source current, μ is the field-effect mobility, W is the channel width, L is the channel length, C_i is the capacitance per unit area of the gate dielectric layer, V_G is the gate voltage, and V_T is the threshold voltage. OFET performances were obtained by applying a gate bias from −60 V to 10V (or 20 V when the devices were heated in the presence of oxygen), with the potential gradient between the source and drain contacts kept at −60 V.

5.2.6 In-situ temperature dependent measurements

To control the thermal conditions both for FETs characterization and capacitance measurements, the HFS600E-PB4 Linkam stage was used with the heating and cooling rates maintained at 10°C/ min and the devices were allowed to reach thermal equilibrium and the electronic performance was monitored over time. For the measurement taken under inert conditions, after engaging the probe tips, the Linkam stage capped and the inside chamber was purged with nitrogen gas for at least five minutes before hermetically closing the purge valve. The devices where then brought to the appropriate temperature and the electronic properties were recorded every 30 minutes.

5.3 Poly(ladder-imides) as high temperature matrices

As mentioned in the introduction to this chapter, we are investigating the use of ladder-imide copolymers as higher performing alternatives to the conventional polyimides. As shown in

scheme 5.3 below, this chapter will investigate how each of the shown properties will translate in the behavior of transistor devices based on blend films comprising the newly designed insulating ladder-imide copolymer. The first part of design exploits the benefits of using the CANAL moiety as the solubilizing unit. Inherently, the fused nature of the moiety is expected to benefit the thermal response of the copolymer by minimizing any possible structural fluctuations. This group has also shown to lead to an inherent porosity on the resulting thin films. In our case, this porosity, therefore a reduced film compactness will lead to lower capacitance within the semiconducting blends which is beneficial to the charge transport. The second part of this design targets the fluorination on the anhydride half of the monomer. By using replacing the ketone group with a hexa-fluorinated analogue, we expect to increase the copolymer's overall hydrophobicity, reduce the inherent hydrophilic charge trapping sites, minimize the polarizability under applied electric field, and hence low the dielectric properties within the semiconducting polymer blends. The combination of these features in our blends is believed to lead to improved charge transport and thermal stability.

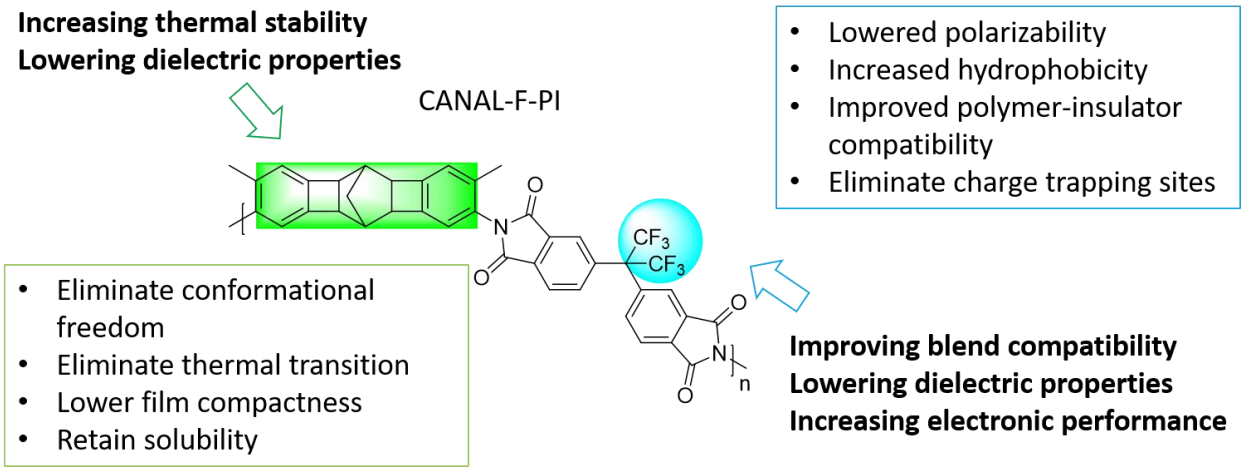


Figure 5.3. Schematic representation of the design principles for ladder-based polyimides for their use in high temperature semiconducting polymer blends.

5.3.1 Tuned blend compatibilization and morphology

5.3.1.1 Improved chain ordering and UV-Vis absorption

As we previously discussed, one of the direct indicators of the blending efficiency in our system is the ability for the matrix polymer to confine the semiconducting polymers domains and improve their ordering. As a result, the confined polymer chains exhibit improved planarity and packing which beneficial when under thermal stress. To test this effect, we utilized UV-Vis absorption and probed the changes in the signature vibronic peaks for chain ordering and packing. Here we wanted to probe the ability of the newly-designed CANAL polymer to confine the conjugated polymer domains and compare such behavior to that found in the parent Matrimid. We thus probed the absorption spectra of the annealed blend films of Is-P1 as the conjugated component and both the CANAL-F-PI polymer and Matrimid in comparison to that of the pristine polymer film. As shown in Figure 5.4, upon blending, the maximum absorption peak not only shows to *redshift* as an indication of improved aggregation, but also significantly increases in intensity indicative of improved planarization and ordering. In addition, this increased ordering

was observed in both Matrimid and the newly designed CANAL copolymer. Recall from previous chapters that this increased ordering was found to be the rationale to stabilized electronic behavior at high temperature since the chains can be maintained ordered under thermal stress.

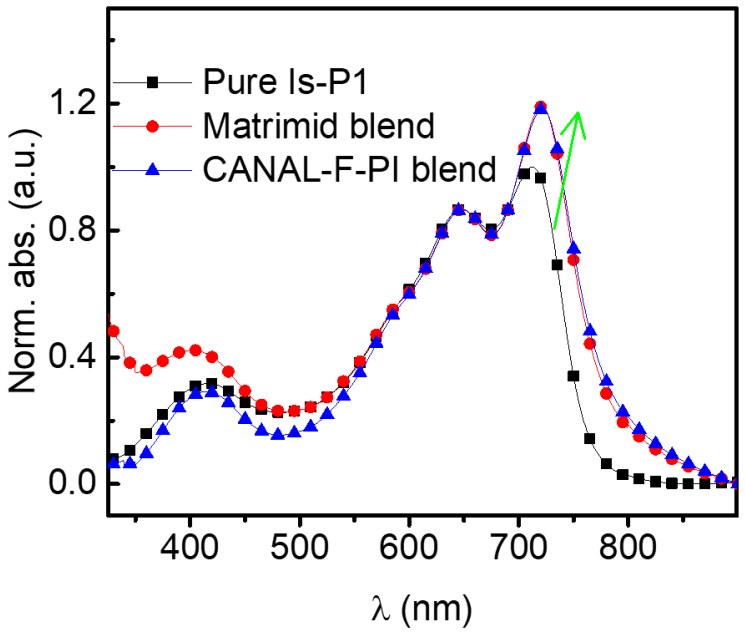


Figure 5.4. Normalized absorption spectra of Is-P1 in its pristine form compared to its Matrimid and CANAL-F-PI blends. A significant redshift accompanied with increased peak intensity in the *0-0* vibronic peak was observed.

5.3.1.2 Domains interconnectivity and topology

Besides confining the conjugated chains, the ability of the host matrix to efficiently alloy the semiconducting domains is another indicator of the blending efficiency and it can be directly probed via the resulting blend morphology. As seen in chapters above, this miscibility between the conjugated domains and the rigid matrix is key to the resulting thermal stability. Also noteworthy from previous chapters, the polyimide-based blends exhibited the formation of large domains in the films (chapters II and III) which was believed to be an indication of poor miscibility and one of the causes of poor electronic performance of the transistor devices made therefrom. To probe

the improvement in the compatibility of our blend films, we imaged the blend morphology in films processed by spin coating the conjugated polymer and the ladder copolymer. We selected the isoindigo based semiconducting polymer (Is-P1) discussed above and compared its behavior when blended with CANAL-F-PI in comparison to Matrimid. To evaluate the ability of the new matrix to form interpenetrating network with the conjugated polymer domains, we imaged the topology of the blend films with increasing content of the semiconductor. As shown in Figure 5.5, the AFM images revealed that Is-P1 could readily form a well interconnected structure within the CANAL-F-PI polymer even when low blend contents (40%) were utilized. Recall from chapter 3 that in the case of Matrimid, it required as high as 55% of the conjugated polymer to establish such a network. We believe here that the improved hydrophobicity owing to the presence of the hexafluoroisopropylidene groups renders the blend components much more compatible so that the isoindigo domains are not forced to form isolated micelles in the blend film. Instead, the domains can readily be uniformly distributed within the host matrix, and with the proper composition, a uniform and compact network is formed as evidenced by the topology AFM scans.

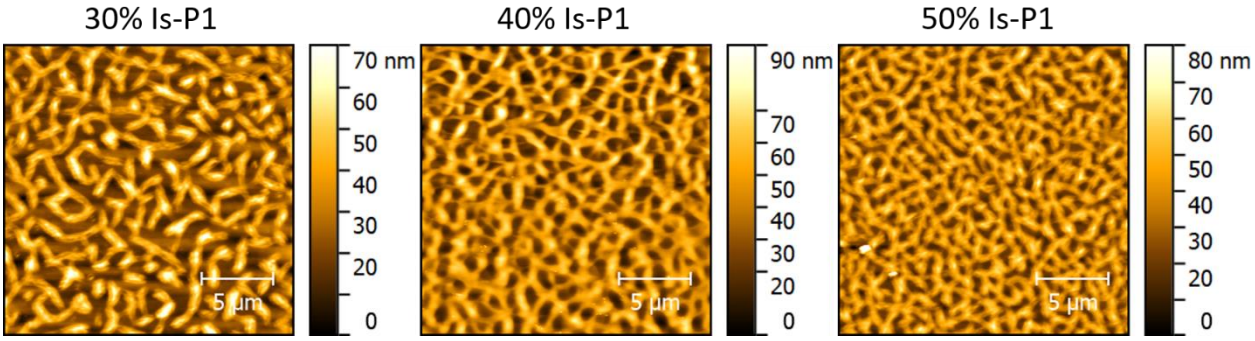


Figure 5.5. Morphology characterization of blend films of CANAL-F-PI and Is-P1. A uniformly interpenetrating network between the two polymers could obtained.

5.3.2 Improved dielectrics properties

A key aspect found in the fluorinated polyimides, is their lowered dielectric constant. For the current discussion, we are interested in how the presence of the large amount of the insulator component in the semiconducting layer will impact the capacitive behavior of film. In the case of a capacitive layer, the charges accumulated at the gate interfaces will become slower to be injected in the functional channel. i.e. the semiconducting layer will begin to act as a charge trapping region. With such blockage of charge carriers, we would expect such blends to yield poor charge mobilities. We then carried the capacitance measurements on both Matrimid and CANAL-F-PI. We processed the corresponding films in the same manner the semiconducting blends are processed. We anticipate that the capacitance measured from the pristine matrices would reasonably mirror the effect that they will have on the charge transport efficiency once used in the blends. Figure 5.6. a) illustrates the sandwich configuration used for the capacitance measurement. The thin films of the insulator were sandwiched between two conductive layers (ITO and Au) and the electric field was applied on the resulting capacitor. Figure 5.6. b) shows the measurement capacitance in such sandwich configuration. We could observe that these films are highly capacitive as they are processed to be extremely thin (around 50 nm). We can also see that in accordance to the molecular design, the copolymer with fluorine atoms is twice less capacitive than Matrimid. This result could be explained by the lower polarizability enabled by the fluorine atoms as well the lowered packing density resulting from the porosity introduced by the CANAL group.

We also back-calculated the thickness-dependent dielectric constant (k) for these matrices using the following classical equation:

$$k = C\frac{d}{A * k_o}$$

where k is the dielectric constant, C is the measured capacitance, d and A are the distance between the plates and the area of the conductive plates, respectively. k_o is the permittivity of vacuum (8.854 pF/m). We extracted the thickness of the matrix films to be 50 (±3)nm as shown in Figure 5.7. The area of the conductive contacts was measured to be 1.1 mm^2 as described in chapter 3. The corresponding dielectric constants were thus calculated to be around 4.5 for Matrimid and 2.4 in the case of CANAL-F-PI which were in good agreement with literature values.[153] We thus expect that this lowered dielectric behavior within the designed matrix, which is one again attributed to the used of fluorinated groups and lowered film compactness, will beneficial once we form blends with semiconducting polymers.

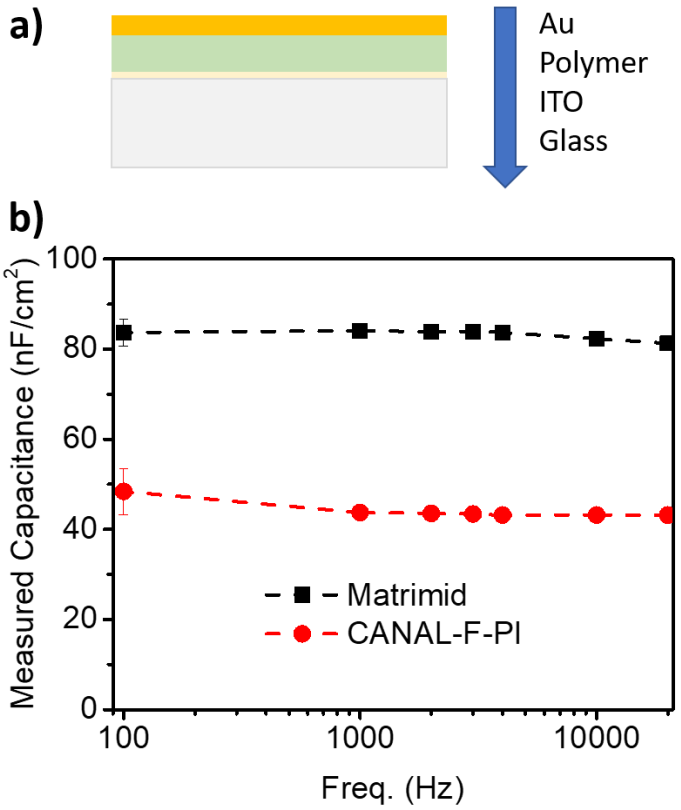


Figure 5.6. Capacitance comparison between polyimide-based matrices. a) The illustration of the sandwich structure used for the capacitance measurement. b) Measured capacitances for Matrimid and CANAL-F-PI.

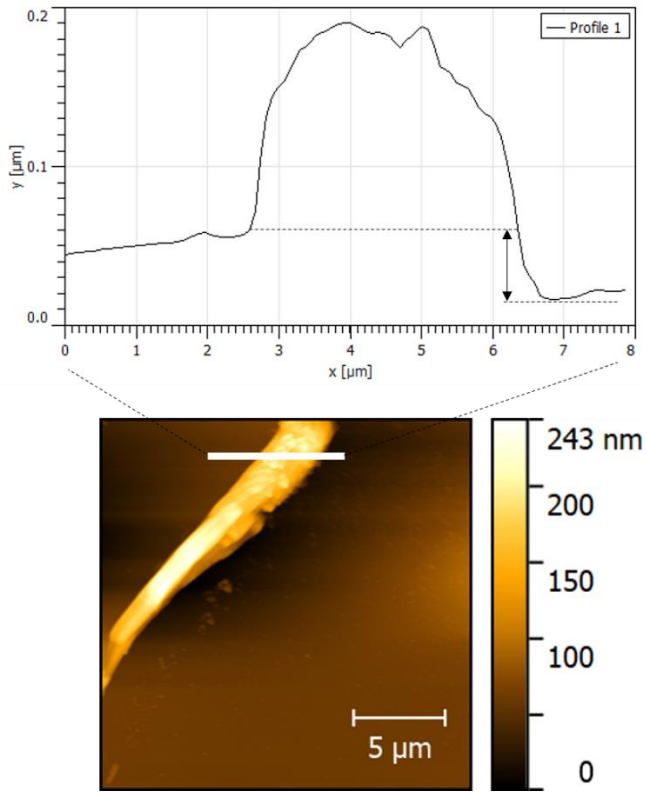


Figure 5.7. Thickness extraction for matrix polymer films for the capacitance evaluation. The thin film thickness was extracted to be near 50 nm.

5.3.3 Improved transistor performance

To test the expect electronic superiority expected in the blends of CANAL-F-PI, we fabricated transistor devices using 40% blend of Is-P1. We then tested the two blend performances and compared them to the pristine polymer film. Is-P1, as discussed in chapters above, offers modest transistor performance which had showed to barely benefit from the fiber-like morphology and aggregation induced by the presence of Matrimid in the blends. Charge mobilities no higher than 0.15 cm^2/Vs could be attained in the case of Is-P1/Matrimid. The newly designed CANAL-F-PI based blends showed to boost these mobilities on to 0.75 cm^2/Vs on average. As shown in Figure 5.8, the transfer characteristics from an average device made with each blend film with Is-P1 reveal much improved behavior in CANAL-F-PI blends in comparison to Matrimid.

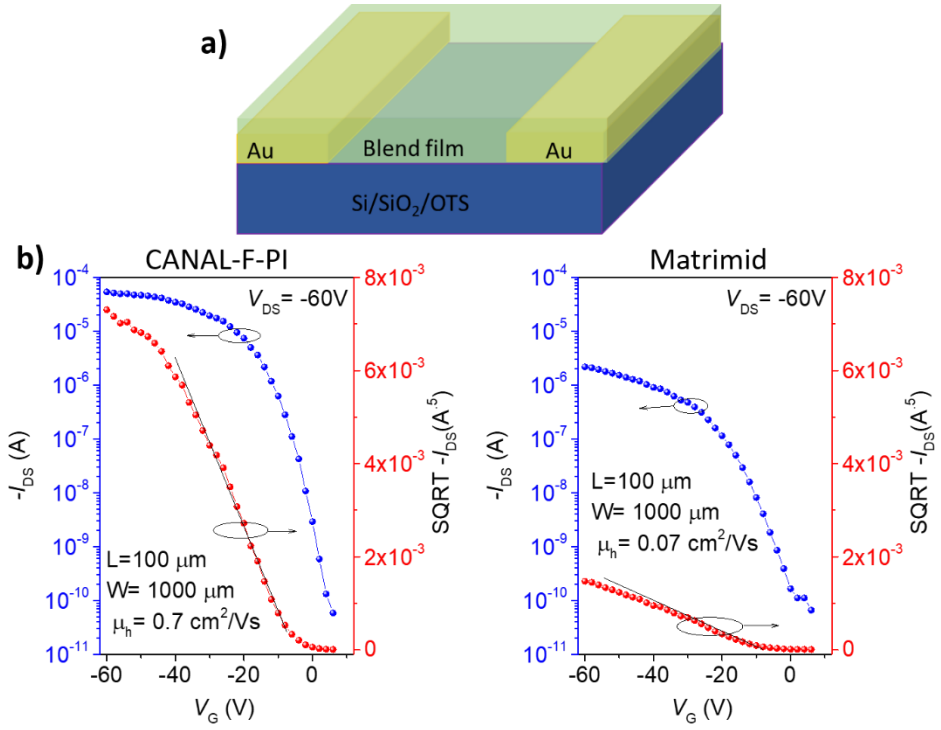


Figure 5.8. Electronic properties of CANAL-F-PI based blends compared to Matrimid based blends. a) Illustration of the transistor devices used for electronic performance comparison. b) Characteristic transfer curves from the optimized blend devices measured at ambient.

To test the reduced trap density in the case of fluorinated matrix, we used the hysteresis measurement to compare between Matrimid and CANAL-F-PI. During the hysteresis measurement, the gate bias is swept forward and backward, and the resulting current curves are overlapped for comparison. In case of little to no charge trapping, the forward and backward scans should yield overlapping current curves. This measurement is one of the commonly utilized quick indicators to probe the interface quality in terms of charge trapping defects. As seen in Figure 5.9, the transistor devices based on CANAL-F-PI blend films exhibit nicely overlapping forward and backward scans. Conversely, the Matrimid-based blends yield significantly worsened overlap indicative of higher hysteresis, i.e. higher degree of charge trapping. From most of the devices we measured, not only did the backward scan current not overlap the forward scan in the case of

Matrimid, but it was also less stable as seen in Figure 5.9 which hints that in these blends, the charge carriers are slowed down by different trapping sites. This trapping behavior could be explained by the polarizable groups in Matrimid which were found to increase its inherent capacitance.

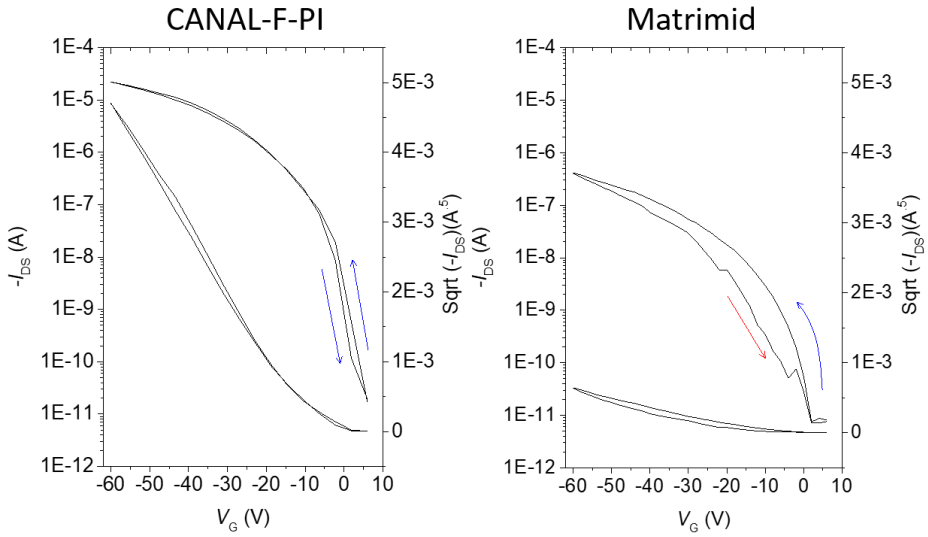


Figure 5.9. Hysteresis characterization of the transistor devices based on blend films of Matrimid and its fluorinated CANAL-based derivative.

5.3.4 Thermally stable high-performance transistors

To test the thermal stability of the newly designed semiconducting polymer blends, we fabricated transistor devices and studied their tolerance towards temperature when baked for a long period of time. As shown in Figure 5.10, the bottom gate bottom contact devices were baked at 195°C under nitrogen up to 12 hours and the thermal stress response was monitored. The CANAL-F-PI based transistor exhibited excellent thermal tolerance as seen from the overlapping transfer characteristic curves. When the ON and OFF drain current were further extracted from the baked devices, minimal changes could be observed even after 12 hours of uninterrupted heating (Figure

5.11). This excellent thermal stability observed in the devices made from the ladder polyimide blends could be credited to the thermal robustness of the matrix polymer enabling extremely stable semiconducting polymer blends. Note that these blends were intentionally measured under nitrogen environments since CANAL-based polyimides possess inherent porosity which renders their behavior to be directly influence by the moisture. In fact, this inherent is envisioned as a venue for high temperature gas sensing as the permeability of the copolymer can readily be tuned by designed functionalization of the CANAL moiety.[155, 158, 159]

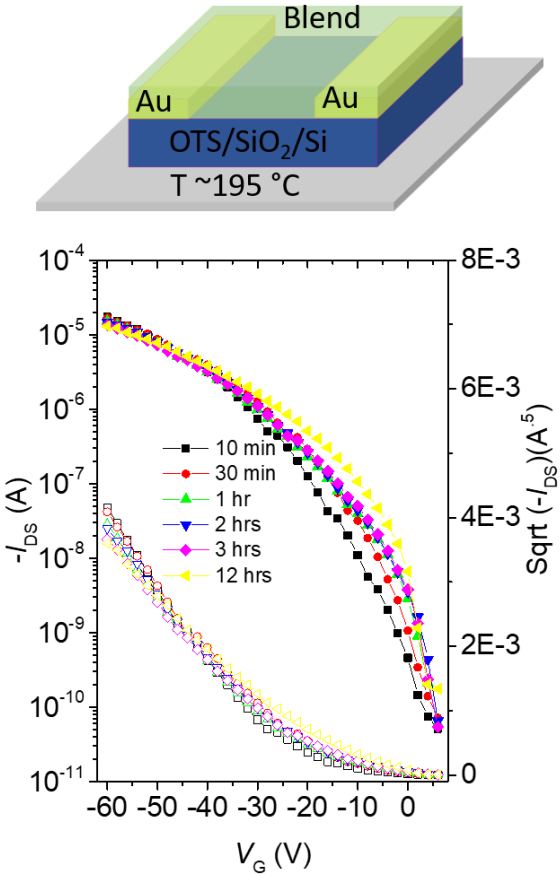


Figure 5.10. Baking characterization of transistor devices based on CANAL-F-PI blends. Overlapping current curves are observed when the devices are subjected to constant thermal stress at 195°C up to 12 hours.

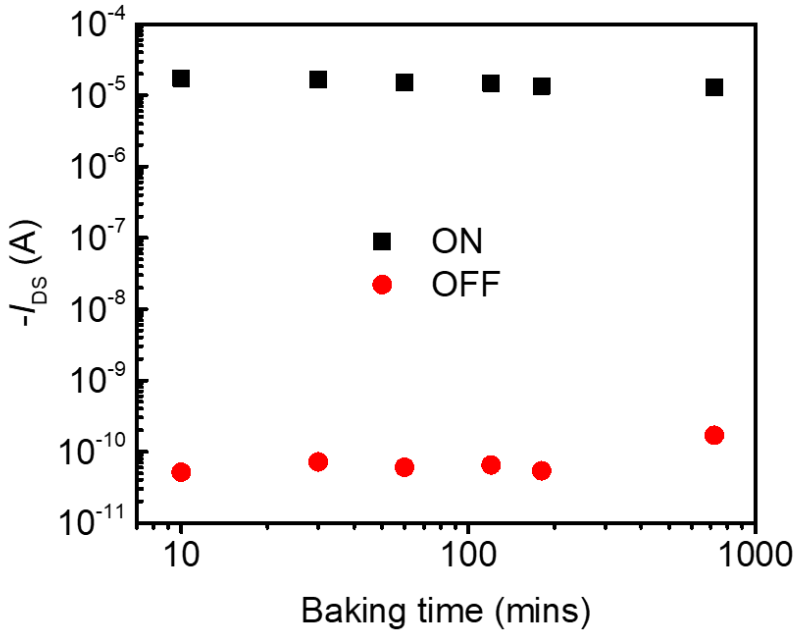


Figure 5.11. Baking analysis of the transistor devices based on Is-P1/CANAL-F-PI blends. The extracted ON/OFF currents exhibit excellent stability even after baking for 12 hours under N_2.

Lastly, we wanted to test whether the CANAL-F-PI films which exhibited minimal charge trapping behavior (minimal hysteresis behavior) at room temperature can retain such a beneficial property after prolonged thermal stress. We then carried out the hysteresis analysis as we discussed in sections above. We performed the forward and backward scans on the transistor devices that were heated for 12 uninterrupted hours at 195°C. We predicted that the presence of the fluorinated groups in the anhydride unit helps minimize charge trapping. We also expect that the thermal stability of the ladder-imide copolymer renders thermally robust morphologies through which the carriers can delocalize effectively even at very high temperature. The hysteresis curves revealed that even under oven-like conditions, overlapping forward and backward currents can be obtained in our blend films. This indicated that our designed copolymers and resulting semiconducting blends are excellent candidates for electronics that must function under extreme thermal conditions.

As shown in Figure 5.12, even after 12 hours of baking, the blend films can still yield excellent hysteresis-free transfer characteristics.

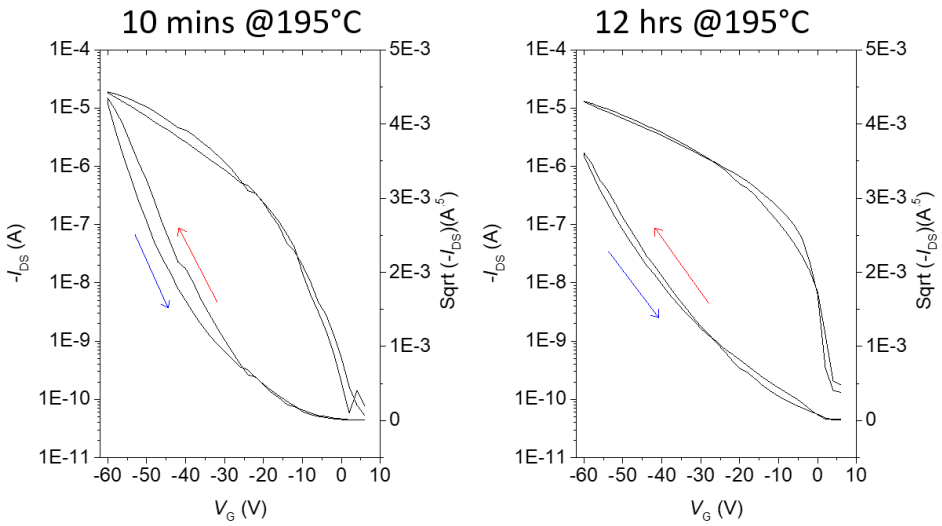


Figure 5.12. Hysteresis characterization of transistor devices based on CANAL-F-PI blends under thermal stress.

5.4 Conclusions

The blending concept for high temperature operation stability offers the opportunity of bridging the best of both worlds from the semiconducting polymers and the rigid matrix hosts. In order to answer the question of how stable our blend devices can be, two design principles are to be considered: how much heat the semiconducting conjugates can sustain, and how rigid can the host matrix remain upon heating to ensure its confining abilities. To couple these properties with high performance, it is crucial that we select matrices that do not significantly hamper the efficient transport once in the functional layer. In this chapter we demonstrated that by designing ladder-imide copolymers, the thermal stability of the matrix can be extremely enhanced. At the same time, we showed that we can improve the electronic performance of the blends by designing matrices

that while housing the semiconductor, do not trap the charge carriers. Substituting carbonyl groups by the hexafluoroisopropylidene showed to not only lower the dielectric constant of the matrix polymer in comparison the parent polyimide, but also improve the interconnectivity in the blend morphology. The increased hydrophobicity in the copolymer improved the blend compatibility and the fluorination lead to lower polarizability and therefore lowered capacitance. We then demonstrated improved electronic performances in the transistor devices using the ladder-imide copolymer in comparison to Matrimid as well as excellent thermal stability. We envision such matrices to find applications in extreme temperature applications such as gas and pressure sensing. Further molecular designs in this regard also become possible owing to the tunability of the CANAL building unit.

CHAPTER 6. CLOSING REMARKS AND OUTLOOK

We have discussed the design, processing, and characterization of semiconducting polymers and polymer blends that are stable at high temperature. The first chapter offered an overview of charge transport basics in organic semiconductor especially the impact of temperature. We showed that in most organic semiconductors, though charge transport is a typically thermally activated, the resulting disorder limits their high temperature operation stability. We provided literary examples showing that the effect of temperature of the film morphology, the packing motifs, and the chain distortions are the key causes to why organic semiconductors only exhibit stable operation in a limited temperature window.

Chapter II introduced our blending design to enable high temperature operation. We laid out the design principles of the thermally robust semiconducting blends. We showed that instead of using the common insulators used to improve environmental stability, we can use high Tg matrices, establish an interpenetrating network between the conjugated polymers and the insulator, and form thermally stable thin films. The formation of the interpenetrating morphology, in which the semiconducting chains are physically confined was shown to benefit the morphology stability at elevated temperature. We showed that the induced order via blending is key towards designing such films. Through opto-electronic characterization we proved that using rigid matrices benefits the packing among the crystalline domains of the conjugated component enabling efficient transport even under harsh temperatures. We also showed that through molecular dynamics simulations, this confinement effect can be predicted and used to rationalize the improved order in terms of dihedral torsions when the polymer films are heated. We then demonstrated generality of this blending strategy as a route towards high temperature electronic applications.

Chapter III focused on the demonstration of the all-plastic thermally stable devices utilizing the blending concept to enable the semiconducting properties at high temperature. We envision that one of the key advantages of the studied blending concept will its ability to be incorporated into light weight plastic devices. Such devices will find applications in smart textiles, as well as other industries requiring the combination of flexibility, lightweight, and thermal stability. We thus studied the use of polyimide-based substrates, dielectrics, and then semiconducting layers in order to assembly an all-plastic thermal stable transistor device array. Through the sequential layering approach, we demonstrated the fabrication of polyimide-based transistors and carefully characterized the properties of each individual layer to ensure the integrity upon assembly. We then demonstrated the stability of our newly designed transistors, especially their stability under oven-like conditions. We attributed the observed stability to the inherent thermal robustness enabled by polyimide layers, the matchup in thermal expansion amongst layers, and the low operating voltages that were needed to drive the charge carriers in our devices. As the need for electronics that can function in harsh thermal environments keeps rising as humankind strives to revolutionize modes of transportation, navigate the outer space, and upgrade ways of energy harvesting, we believe that such devices will soon find numerous applications.

In Chapter IV, we investigated the effect of molecular size choice in the behavior of blends. We demonstrated that through fine tuning of the molecular weight of a highly soluble donor-acceptor conjugated polymer, we can gain deeper insight in what governs the spinodal like morphology that is formed in our blend composites. We found that the lower molecular fractions of our polymer exhibit lower miscibility with the matrix polymer as the smaller the chains are, the easier it was found for them to simply crystallize and crash out of the mix and form isolated micelles. We found that to ensure the interpenetrating feature between the conjugated polymer and

the less crystalline host insulator, the molecular size of the conjugates needs to be increased. This becomes relevant in the design principles of blending approach as we strive to provide guidelines of how to ensure thermal stability as a universal approach. It was thus apparent that the control over polydispersity is extremely important to ensure uniform miscibility. We also proposed the morphology formation mechanism in our blend system, i.e. the crystallization behavior of the conjugated polymer dictates the blend morphology. We proved through careful opto-electronic characterizations that the smaller polymer chains which crystallize much faster, do not sense the presence of the insulator. The key aspect of the blending design being to house the conjugated polymer within the host matrix, with smaller polymer chains, this feature becomes compromised and the thermal stabilization power of the blend become lost. Through a molecular weight guided thermal stabilization, we were thus able to demonstrate, for the first time, polymer-based transistor devices that could handle constant thermal stress at high temperature for as long as 24 hours.

Lastly, Chapter V investigated on design principles towards selecting/designing optimized insulating hosts for the high temperature blends. We aimed to improve the chemical structure of Matrimid, a polyimide host matrix that we studied for its thermal durability. We identified that structural freedom could be mitigated by incorporating much more fused ring systems. The CANAL enabled polycondensation could yield polyimides with no detectable thermal transition phases up to 400°C. We also proposed and demonstrated that by incorporating fluorinated groups in the anhydride moiety, the dielectric properties of the matrix could be tuned to lower its charge trapping nature. We thus used a norbornene-based ladder-imide copolymer and demonstrated lowered capacitance in the matrix and fabricated transistor devices with improved electronic performance and remarkable thermal stability. We closed this chapter by mentioning that the inherent porosity found in the ladder copolymer opens a venue for high temperature gas sensing.

Organic semiconductors, especially polymer thin films have witnessed tremendous advancements for the past three decades owing their promising solution processability, flexibility, stretchability, and in some cases bio-compatibility. Our research identified that one of the fields that has yet to capitalize on these advantages is the field of high temperature organic electronics. This is mostly because semiconducting polymer thin films have been believed to be unstable at high temperatures. Because of this, most studies on high temperature stable operation have been limited to small molecule semiconductors. The current research, for the first time, demonstrated that semiconducting polymer thin films can indeed remain operational at high temperature given that the polymer chains can be maintained ordered. We proposed and demonstrated a blending approach in which a high glass transition temperature matrix polymer is used a rigid backbone to house a conjugated polymer in an interpenetrating blend composite. We found that this physical confinement leads to improved chain packing, minimizes morphological changes upon heat, and reduces the freed to torsions and rearrangements that are otherwise found in polymer films.

With this demonstration of high temperature semiconductor operation stability, we hope to spark new research directions especially on deeper investigation of charge transport dependence on temperature. Traditionally, such studies have been limited to low temperature regimes where morphology fluctuations are minimal. Now that ordered semiconducting domains can be attained upon blending, the impact of temperature of the hoping behavior of carrier in polymer can be further studied. Other aspects that impact charge transport such as contact resistance, channel resistant, and thermal expansion are also within fundamental analysis reach.

The blending concept is also envisioned to find a valuable role in applications using organic electronics. As emphasized throughout our discussion, polymers are attractive as they can yield lightweight and flexible circuitries. Traditionally, insulating polymers have found a role as the

packaging materials to serve as thermal shields. For instance, space shuttles utilize large amounts of polymers as lightweight, thermally insulating, and robust materials. Our research has now demonstrated that materials such as polyimides can be brought much closer to the functional layer. The packaging is now approaching the molecular level. This entails that instead of relying on heavy insulating to maintain the electronics within optimal operation temperatures, polymers can be used to fabricate the circuits and significantly reduced the overall device's weight. We believe that this approach will soon enable the manufacturing of organic high temperature electronics.

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VITA

A. Education

Wofford College, Spartanburg, SC. Chemistry, B.S., 05, 2015

Purdue University, West Lafayette, IN. Organic Chemistry, MS/PhD., 12, 2019

B. Awards

2019: Herbert C. Brown Graduate Student Research Award, Purdue University

2019: Herbert C. Brown Travel Award, Purdue University

2019: Arthur Nowick Graduate Student Award, Materials Research Society

2019: Graduate Student Gold Award, Materials Research Society

2018: Charles Viol Fellowship, Purdue University

2016: Herbert C. Brown Travel Award, Purdue University

2011-2015: Rwanda Presidential Scholarship, Wofford College

C. Work Experience

2017-Present: Graduate Research Assistant, Prof. Mei research group, Purdue University

- Lead graduate thesis research on the design, processing, and characterization of *High Temperature Organic Semiconducting Polymers and Polymer Blends*
- Lead the group's effort on ink formulation and the *Roll-to-roll Processing and Lamination of Electrochromic Polymer Thin Films*
- Helped the group pioneer the processing and characterization of *Melt-Processable Semiconducting Polymers and Polymer Blends*

2015-2017: Graduate Teaching Assistant, Purdue University

- Instructed undergraduate laboratory courses for both general and organic chemistry

- Assessed students' experimental reports and provided mentorship and feedback

06-09/2015: Undergraduate Research Assistant, Purdue University

06-09/2014: Undergraduate Research Intern, Center for Sustainable Materials Chemistry

D. Skills & Expertise

- Solution processing of polymer thin films: roll-to-roll (gravure & slot-die) coating, inkjet printing, blade shearing, nanosuspension, spray coating, doping, additives engineering
- Solvent-free processing of polymers: melt pressing, shearing, extrusion
- Solid-state characterization: atomic force microscopy (AFM), scanning electron microscopy (SEM), x-ray diffraction (XRD) analysis, UV-Vis absorption, optical polarized microscopy (OPM), dynamic scanning calorimetry (DSC), tensile modulus and crack-on-set measurements, dielectric and capacitance measurement
- Electronic devices fabrication and characterization: field effect transistors (FETs), flexible and stretchable transistors, four-point probe measurement

E. List of Publications

1. Gumyusenge, A.; Luo, X.; Zhang, H.; Pitch, G.; Zhao, Y.; Ayzner, A.; Mei, J., Isoindigo-based Binary Polymer Blends for Solution-Processing of Semiconducting Nanofiber Networks. *ACS Appl. Poly. Materials*, **2019**, 1, 1778-1786.
2. Li, X., Perera, K., He, J., Gumyusenge, A., Mei, J. Roll-to-Roll Manufacturing of Electrochromic Devices: Roadblocks and Solutions, *J. Mater. Chem.*, **2019**, 7, 12761-12789.
3. Gumyusenge, A.; Luo, X.; Ke, Z.; Tran, D. T.; Mei, J., Polyimide-based All-Plastic High Temperature Electronics. *ACS Materials Lett*., **2019**, 1, 154-157.
4. Gumyusenge, A.; McNutt, W.; Mei, J., Conjugated Polymer Thin Films for Stretchable Electronics. A Book Chapter in *Conjugated Polymers*. *CRC Press*. **2019**. 535-559.

5. Gumyusenge, A.; Tran, D. T.; Luo, X.; Pitch, G. M.; Zhao, Y.; Jenkins, K. A.; Dunn, T. J.; Ayzner, A. L.; Savoie, B. M.; Mei, J. Semiconducting polymer blends that exhibit stable charge transport at high temperatures. *Science*. **2018**, 362, 1131-1134.
6. Gumyusenge, A.; Xu, T.; Wang, X.; Mei, J., Organic-Based Transistors and Sensors. A Book Chapter in *Flexible and Stretchable Medical Devices*, Wiley-VCH & Co. **2018**; 53-81.
7. Gumyusenge, A.; Zhao, X.; Zhao, Y.; Mei, J., Attaining Melt Processing of Complementary Semiconducting Polymer Blends at 130 °C via Side-Chain Engineering. *ACS Appl. Mater. Interfaces* **2018,** *10*, 4904-4909.
8. Zhao, Y.; Gumyusenge, A.; He, J.; Qu, G.; McNutt, W. W.; Long, Y.; Zhang, H.; Huang, L.; Diao, Y.; Mei, J., Continuous Melt-Drawing of Highly Aligned Flexible and Stretchable Semiconducting Microfibers for Organic Electronics. *Adv. Funct. Mater.* **2017**, 1705584.
9. Zhao, X.; Xue, G.; Qu, G.; Singhania, V.; Zhao, Y.; Butrouna, K.; Gumyusenge, A.; Diao, Y.; Graham, K. R.; Li, H.; Mei, J., Complementary Semiconducting Polymer Blends: Influence of Side Chains of Matrix Polymers. *Macromolecules* **2017**, *50*, 6202-6209.
10. Xue, G.; Zhao, X.; Qu, G.; Xu, T.; Gumyusenge, A.; Zhang, Z.; Zhao, Y.; Diao, Y.; Li, H.; Mei, J., Symmetry Breaking in Side Chains Leading to Mixed Orientations and Improved Charge Transport in Isoindigo-alt-Bithiophene Based Polymer Thin Films. *ACS Appl. Mater. Interfaces* **2017,** *9*, 25426-25433.
11. Zhao, Y.; Zhao, X.; Roders, M.; Gumyusenge, A.; Ayzner, A. L.; Mei, J., Melt-Processing of Complementary Semiconducting Polymer Blends for High Performance Organic Transistors. *Adv. Mater.* **2017,** *29*, 1605056.

F. Activities and Presentations

1. Mentor to rising graduate and undergraduate students in the research group

2. Active member of the Diversity Transformation Award (DTA) team, a chemistry department diversity initiative to help facilitate communication between prospective minority students and current graduate students, Purdue University
3. Invited presentation at the 2019 SPIE optics and photonics conference; San Diego, CA
4. Invited graduate student awards finalist oral presentation and poster presentation at the 2019 MRS Spring Meeting and Exhibit; Phoenix, AZ
5. Selected student presentation at the 36th Annual H.C. Brown Lectures; Purdue University, West Lafayette, IN
6. Poster presentation at the SMART Films Industry Day at Birck Nanotechnology Center; Purdue University, West Lafayette, IN
7. Oral & poster presentation at the 253rd American Chemical Society National Meeting; San Francisco, CA

RESEARCH

REPORT

POLYMERS

Semiconducting polymer blends that exhibit stable charge transport at high temperatures

Aristide Gumyusenge[1], Dung T. Tran[1], Xuyi Luo[1], Gregory M. Pitch[2], Yan Zhao[1], Kaelon A. Jenkins[1], Tim J. Dunn[3], Alexander L. Ayzner[2], Brett M. Savoie[4]*, Jianguo Mei[1]*

Although high-temperature operation (i.e., beyond 150°C) is of great interest for many electronics applications, achieving stable carrier mobilities for organic semiconductors at elevated temperatures is fundamentally challenging. We report a general strategy to make thermally stable high-temperature semiconducting polymer blends, composed of interpenetrating semicrystalline conjugated polymers and high glass-transition temperature insulating matrices. When properly engineered, such polymer blends display a temperature-insensitive charge transport behavior with hole mobility exceeding 2.0 cm^2/V-s across a wide temperature range from room temperature up to 220°C in thin-film transistors.

The performance of inorganic semiconductors optimized for operation at ambient temperatures degrades at elevated temperatures. Charge carriers are thermally promoted across the band gap, which leads to increased carrier densities, junction leakages, and reduced charge carrier mobility (*1*–*3*). To improve the device performance and lifetime in these harsh thermal conditions, wide-bandgap materials have been utilized (*4*, *5*). Alternatively, active or passive cooling, thermally engineered packaging, as well as electrical isolation between multiple transistors are used to maintain the optimal electronic performance (*6*). By contrast, organic semiconductors commonly display thermally activated charge transport features (*7*, *8*). Charge transport is facilitated in organics with moderate temperature increases, leading to improved performance (*9*). However, this thermally activated charge transport becomes counteracted by unstable morphologies and disrupted molecular packing at higher temperatures, especially in polymer thin films (*10*, *11*). Although devices such as organic field-effect transistors are now common (*12*), their operation is normally at ambient conditions. High-temperature annealing effects have been explored in organic semiconductors (*13*–*15*), but in all reports, charge-carrier mobilities have been temperature dependent and start to decline at >150°C.

Blending semiconducting polymers with insulating hosts has been used as a general strategy to improve electronic performance, processability, and mechanical and environmental stability in electronic devices (*16*–*18*). Preserving close intermolecular interactions and packing motifs at elevated temperatures is the key challenge, especially for semiconducting polymers (*10*, *19*). We hypothesized that interpenetrating networks between semicrystalline conjugated polymers and high glass-transition (T_g) insulating polymers can confine conformational changes of semiconducting polymer chains at elevated temperatures. To test this concept, we first select diketopyrrolopyrrole-thiophene (DPP-T; P1), a high-performance conjugated polymer, and poly(N-vinyl carbazole) (PVK, T_g ~220°C) as the high-*T*g host (Fig. 1A) and studied blends from 40 to 90 weight % (wt %) of PVK in spin-cast films. The blends with between 55 and 65 wt % PVK formed interpenetrating channels between the conjugated polymer P1 and the rigid host PVK, as observed from atomic force microscopy (AFM) images (Fig. 1B and fig. S1).

Testing the blend films in field-effect transistors (FETs) under ambient and inert conditions, we observed thermally stable operations at high temperatures up to 220°C with hole mobilities as high as 2.5 cm^2/V·s at the blend ratios of 55 to 65 wt % PVK that created a bicontinuous morphology with interconnected P1 domains (Fig. 1C and fig. S2). With loadings outside this range, undesired vertical or large lateral phase segregation occurs, which leads to the loss of thermal stability. The mobility of the pristine semiconductor P1 decreases to 8% at 220°C. Ultraviolet-visible (UV-Vis) absorption spectra (Fig. 1D) revealed an increase in the *0-0* vibronic peak intensities upon approaching the optimal blending ratios, indicative of increasing ordering and π-π interactions between P1 chains in the confined domains (*20*–*22*). The bottom surface morphology analysis confirms that the interpenetrating structure is preserved at the gate interface in the thermally stable high-performance blends (fig. S3).

To elucidate the observed thermal stability of the 60 wt % PVK blend versus pure P1, we use in situ temperature-dependent UV-Vis spectroscopy, AFM, and grazing incidence x-ray diffraction (GIXD), as well as molecular dynamics simulations to study the effect of temperature on the intermolecular interactions of the semiconducting chains. Upon heating, the UV-Vis absorption spectra of pristine P1 films revealed a blue shift of 35 nm in the maximum absorption peak, accompanied by a decrease in both the *0-0* and the *0-1* peaks (Fig. 2A). These phenomena are consistent with the polymer chains' deaggregating and reorganizing caused by the thermal energy disrupting the crystallites. For the blend films, the chain ordering and interchain interactions were less affected upon heating, in comparison with pristine P1 films, as evidenced by the less pronounced decrease of the *0-0* vibronic peak intensity. More distinctively, the *0-0* vibronic peak that vanished in the P1 films was retained in the blended films even at temperatures up to 220°C (Fig. 2B). The temperature-dependent AFM analysis also revealed that the microscale morphology of the pristine P1 films changes upon heating, whereas the P1/PVK blend film morphology is not affected by heating (fig. S4). Together, these observations indicated that the matrix polymer effectively confined the semiconducting polymer and limited dihedral twisting and larger structural reorganizations that were responsible for the loss of the carrier mobility at high temperatures.

In situ temperature-dependent GIXD studies showed that in the 60% PVK blend film, the π-π stacking distance of P1 was reduced from 3.70 to 3.64 Å, relative to the pristine P1 (Fig. 2, C and D, and fig. S5). In both cases, the π-π stacking distance increased when the thin films were heated and reached 3.79 and 3.73 Å at 200°C for the pure P1 and the PVK blend films, respectively.

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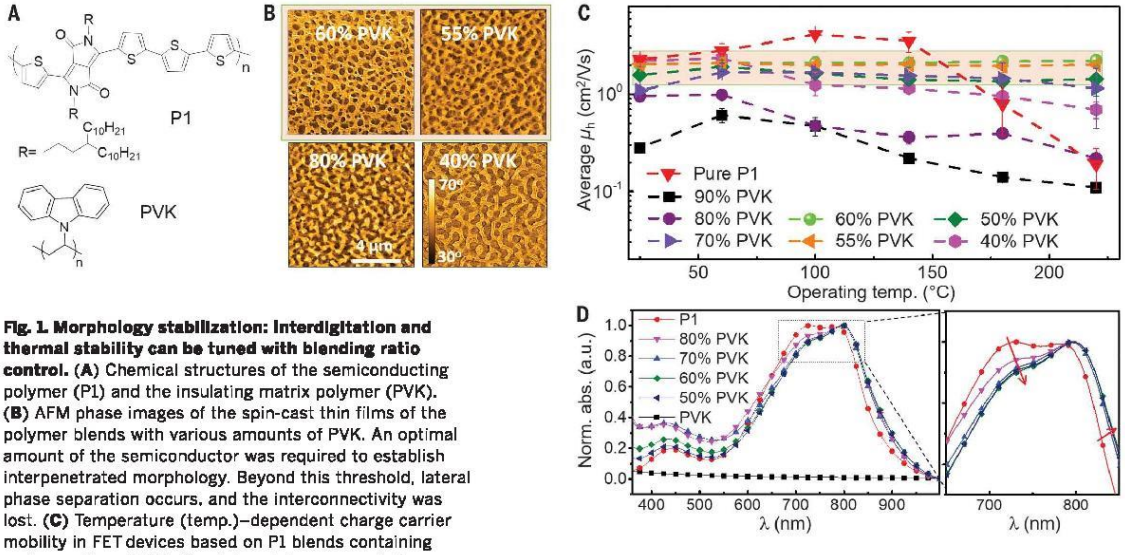

Fig. 1. Morphology stabilization: Interdigitation and thermal stability can be tuned with blending ratio control. (**A**) Chemical structures of the semiconducting polymer (P1) and the insulating matrix polymer (PVK). (**B**) AFM phase images of the spin-cast thin films of the polymer blends with various amounts of PVK. An optimal amount of the semiconductor was required to establish interpenetrated morphology. Beyond this threshold, lateral phase separation occurs, and the interconnectivity was lost. (**C**) Temperature (temp.)–dependent charge carrier mobility in FET devices based on P1 blends containing various ratios of PVK. The data points represent the average hole mobility measured from 10 different devices for each blending ratio, and the error bars represent the standard deviation from the average. The pure P1 data are also plotted. (**D**) Normalized UV-Vis absorption spectra (Norm. abs.) of P1-PVK blends with varying amounts of the matrix polymer. The confinement of the semiconductor within rigid domains of the host led to increased ordering of the conjugated polymer chains. a.u., arbitrary units.

To evaluate the effect of this π-π stacking confinement on the polymer dihedral distribution, molecular dynamics modeling was performed. In these simulations, the π-π separation of the semiconducting polymer chains was restrained to model varying levels of confinement, and the resulting dihedral distributions were compared to characterize the polymer reorganization dynamics (Fig. 2E). At π-π confinements of 3.0 Å, we observed complete conservation of the dihedral distributions at all temperatures. Notably, the CCCN dihedral, corresponding to the DPP-T conformations, exhibited interconversion between gauche conformers, but there was no evidence of gauche-to-trans interconversion (i.e., the onset of chain twisting) at any temperature. Likewise, the SCCC dihedral angle, corresponding to the thiophene-thiophene conformations, broadened with temperature but remained sharply peaked. By contrast, at π-π confinements of 5.0 Å, the SCCC dihedral distribution is broadened at all temperatures, and the CCCN dihedral exhibits gauche-to-trans interconversion at all temperatures (Fig. 2, F and G). Systematic studies of the dihedral distributions under confinements from 3 to 6 Å allowed us to conclude that large-scale DPP-T reorganizations began relatively abruptly once fluctuations in the interchain π-π separation reach ~5 Å (figs. S7 to S9). On the basis of these results, we interpret the π-π confinement exhibited by the bicontinuous P1/PVK blends to play a critical role in restricting intrachain reorganization and enabling temperature-insensitive mobility. This mechanism suggests that this confinement strategy should be general to other semiconducting polymers embedded in similarly rigid matrix polymers or potentially to other confinement strategies like channel templating. The relatively broad range of blending concentrations that exhibit temperature insensitivity (40 to 70%) implies that this effect is relatively insensitive to the width of the confined semiconducting domains.

To evaluate the stability of the blend films under prolonged thermal stress, the fabricated FET devices were subjected to constant heating at 150°C for 6 hours in air. For inorganic semiconductors, prolonged heating leads to increased charge-carrier density and uncontrolled thermal doping (*23*). For organics, prolonged heating, especially above the T_g or the melting point of the semiconductors, leads to morphology changes and device performance degradation (*10*, *11*, *15*). In contrast with the pristine P1 devices under the same conditions, the devices based on the 60% PVK blends retained excellent electronic properties (as high as 95% of the original mobility) under thermal stress (Fig. 3A). The FET devices made from pristine P1 showed a declining on-off current ratio (I_{ON}/I_{OFF}) and increased threshold voltages under constant heating, consistent with earlier observation of unstable morphologies at high temperatures. The thermally stabilized blend-based FET devices retain an on-off current ratio higher than 10^3 and threshold voltages below 3 V after thermal stressing (Fig. 3, B to D).

To demonstrate the generality of our blending strategy, we explore the FET thermal stability of P1 blended with four other high-T_g matrices i.e., polycarbonate (PC), polyacenaphthylene (PAC), polyetherimide (PEI), and Matrimid 5218 (MI) (Fig. 4A). We first optimized the blending ratios to attain interpenetrating morphologies (fig. S10A). FET devices based on these optimized blends exhibited thermally stable charge transport and the P1/PAC blend pair could reach hole mobilities as high as 2.0 $cm^2/V{\cdot}s$ that were stable up to 220°C in open air (Fig. 4B). The optimized P1/PC blend only provided thermally stable operation up to 180°C, which is near the T_g of the host. We also tested other donor-acceptor semiconductors based on high-performance DPP (P2) (*20*) and isoindigo (P3) (*24*) (Fig. 4C) and studied the thermal stability of their blend films with the champion high-Tg matrices, i.e., PVK and PAC. After optimizing the blend ratios to obtain an interpenetrating morphology (fig. S10B), FET devices with excellent thermal stability up to 220°C were also achieved

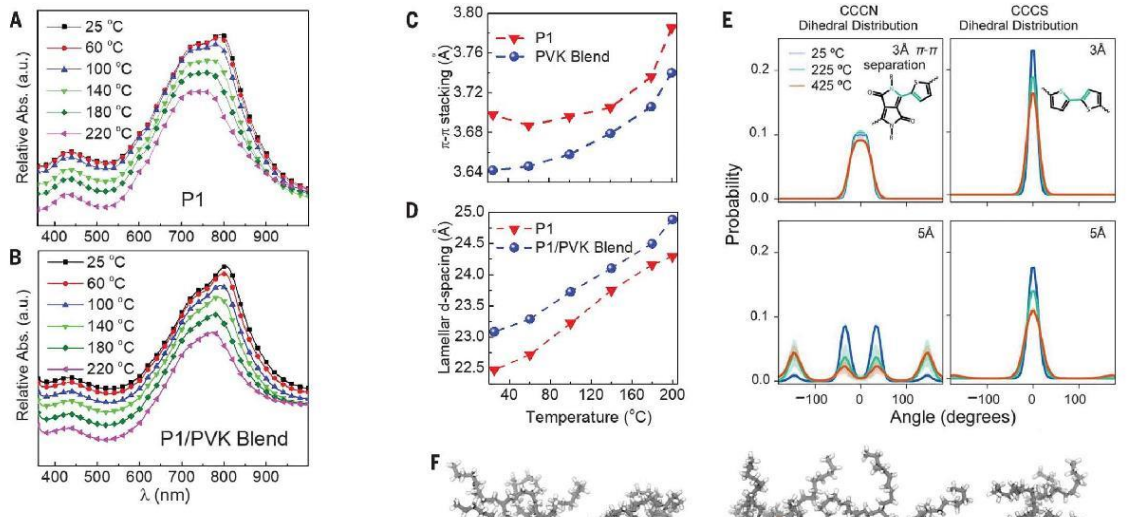

Fig. 2. Thermally stable packing behavior in PVK blends. (**A** and **B**) Temperature-dependent UV-Vis absorption spectra of pristine P1 films and the corresponding PVK blend. (**C** and **D**) Evolution of π-π d-spacing and lamellar stacking in thin films treated at different temperatures. The presence of PVK in the films not only induced closer packing of the conjugated polymer chains, but it also reduced their freedom to thermally expand and rearrange. π-π stacking distance as close as 3.72 Å can be retained at 200°C in the case of the PVK blend film. The peak position was extracted from Gaussian fits to the one-dimensional I(q) versus q plots. (**E**) Simulated dihedral distributions at different temperatures when π-π separations are confined to 3 Å and 5 Å. With the π-π restraint of 5 Å, the distribution broadens, indicative of chains twisting at all temperatures. (**F** and **G**) Packing behavior of DPP-T chains when confined to 3 Å and 5 Å, respectively.

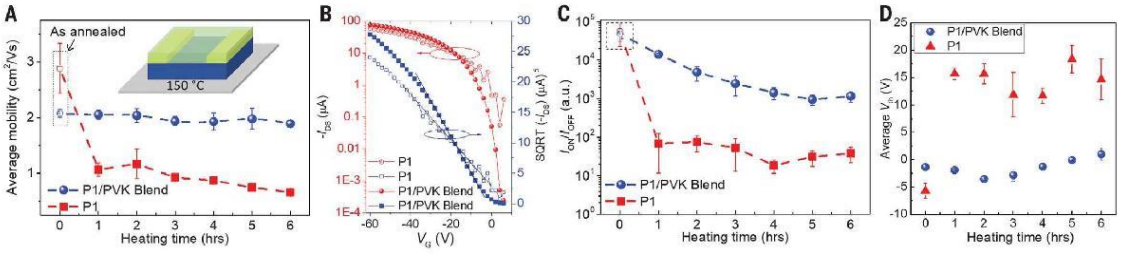

Fig. 3. Effect of thermal stress on FET devices and thermal stability of PVK blends. (**A**) Measured hole mobilities under constant thermal stress for 6 hours. A sudden decline in mobility was observed for pure P1 when the FET device is heated. The blend can retain its original mobility after 6 hours. (**B**) Characteristic transfer curves of FET devices based on P1 with and without PVK after 1 hour of heating. SQRT, square root. (**C**) Impact of heating on the I_{ON}/I_{OFF}. After 1 hour of heating, the ratio fell to nearly 10 for the devices based on P1 while remaining > 10^4 for the blend devices. (**D**) Threshold voltages (V_{th}) for FET devices based on the 60% PVK blends (below 3 V) and pure P1 (exceeding 20 V) upon prolonged heating. The data points represent the average values measured from 10 different devices, and the error bars represent the standard deviation from the average.

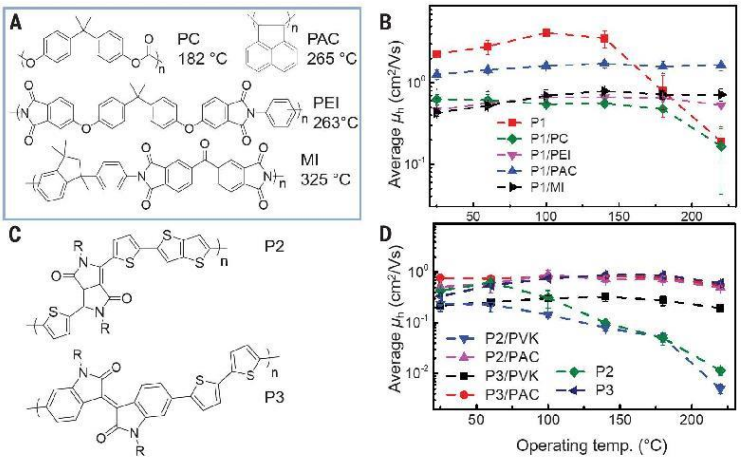

Fig. 4. Attaining universal thermal stability in semiconducting polymer blends. **(A)** Molecular structures and glass-transition temperatures of the representative matrix polymers tested for high-temperature charge transport. Matrimid 5218; PEI, polyetherimide. **(B)** Hole mobilities of FET devices based on the optimized blends of P1 in four different matrices measured in open air. **(C)** Molecular structures of additional semiconducting polymers studied for thermally stable blends. **(D)** Measured FET mobilities from the blend films of P2 and P3 with PVK and PAC used as the host matrices. The blend combinations that had stable close packing exhibited hole mobilities stable up to 220°C. The data points represent the average mobility values measured from 10 different devices, and the error bars represent the standard deviation from the average.

(Fig. 4D). Temperature-dependent UV-Vis absorption analyses on the blend films of P2 and P3 confirmed that those blend pairs with thermally insensitive charge transport properties exhibited a similar behavior as the P1/PVK blend at high temperatures (figs. S11 to S14). One exception was the P2/PVK pair, which did not present a thermally stable charge transport behavior (Fig. 4D). Likewise, this pair did not preserve the characteristic intermolecular interaction vibronic peak upon heating, indicating that this was a necessary feature in stable blends (fig. S12). We also noticed that the pristine P3 film exhibited a nearly thermally stable operation across the tested temperature range. Consistent with the thermally stable blends previously discussed, the P3 film itself also exhibited strong intermolecular interactions even at high temperatures (fig. S13), which suggested the organization of P3 is unusually robust among the studied semiconductors. Lastly, the blending strategy was tested for n-type semiconducting systems, and the blend films that form interpenetrating morphologies exhibited thermally stable operation in comparison with the pristine thin films (fig. S20).

To design high-temperature semiconducting polymer blends, a few requirements appear to be essential: (i) a host matrix with a T_g higher than the desired operating temperature; (ii) a semicrystalline semiconducting polymer; (iii) the interpenetration of the semiconducting component into the host matrix; and (iv) improved intermolecular π-π stacking within semiconducting channels that can be retained at high temperature. The use of high-T_g matrices is demonstrated to be a general strategy to attain these properties by minimizing spatial rearrangements within the polymer films at elevated temperatures. We hypothesized that the superior ordering in the confined channels enhanced charge transport by reduced activation energy and trap density.

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SUPPLEMENTARY MATERIALS

www.sciencemag.org/content/362/6419/1131/suppl/DC1
Materials and Methods
Tables S1 to S3
Figs. S1 to S20
References (*25*–*33*)

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LETTER

Polyimide-Based High-Temperature Plastic Electronics

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Supporting Information

ABSTRACT: All-plastic transistor devices with thermal stability up to 220 °C are demonstrated. We employ polyimide substrates, polyimide dielectrics, and a polyimide-based semiconducting blend to achieve flexible and thermally-robust transistors. An in situ temperature-dependent charge transport study was used to demonstrate that these devices can operate in extremely high temperatures and can sustain prolonged baking. Our devices maintained stable charge-transport characteristics with charge mobilities of 0.20 $cm^2/(V\ s)$, I_{ON}/I_{OFF} of 10^4, threshold voltage of 3 V, and operational voltage of 10 V when baked at 195 °C for 2 h.

Organic-based electronics that are conformable, flexible, low-cost, and lightweight have been studied for the past two decades as alternatives for silicon-based technologies.[1,2] Today, flexible electronics are on the verge of becoming a commodity in daily life applications, such as flexible displays and wearables. One class of application that is yet to benefit from these lightweight and cost-effective electronics is for high-temperature applications, especially in aerospace engineering and the automobile industry, as well as in gas and oil drilling industries.[3,4] These applications require lightweight materials that can sustain harsh thermal conditions for prolonged operation times without requiring additional insulation or cooling. Currently, active or passive cooling and insulation are needed for such applications, resulting in a weight and cost burden especially in aerospace engineering.[5] Carbides and wide-band gap inorganics have been studied as thermally-robust alternatives, but their cost and complicated processing limit their wide adoption.[3] With such requirements, plastic electronics based on thermally-stable plastic substrates, dielectrics, as well as semiconductors potentially become excellent candidates.

Polyimides have been used as heat-resistant materials for high-temperature applications and have been investigated as substrates for fabricating thermally stable, flexible electronics.[6−8] For instance Kuribara et. al. utilized polyimide substrates and fabricated transistor devices for sterilizable medical devices.[6,9] By using thermally-resistant organic small-molecule semiconductors, the fabricated flexible devices showed to remain functional after annealing at temperatures up to 250 °C. The use of polyimide substrates thus enables the fabrication of flexible electronics able to sustain thermal environments in which the commonly used plastic substrates such as polyethylene terephthalate (PET) would not survive.[10] In separate reports, polyimides also constitute a class of excellent dielectric materials as they exhibit excellent capacitive response to electric field, as well as high capacitive breakdown ability with low power consumption in transistor devices.[11−15] For instance, the polymerization of pyromellitic dianhydride (PMDA, $C_{10}H_2O_6$) with 4,4′-oxydianiline (ODA, $C_{12}H_{12}N_2O$), followed by a thermal curing step, has been used to process highly uniform and smooth films of polyimide dielectrics used in transistor devices.[16,17]

The long-standing challenge towards achieving thermal stability has been the design of thermally-stable semiconductors as electronic properties are temperature-dependent and degrade especially at extremely high temperatures.[18,19] Organic semiconductors, a class of materials that exhibit a thermally activated electronic behavior, were recently demonstrated by our research group to be rendered thermally-stable through strategical blending and composites formation.[20] High glass-transition temperature (T_g) matrix polymers were used as hosts in thin films to increase the thermal stability of the semiconducting blends up to 220 °C. With this approach, we demonstrated excellent high-temperature operation stability as opposed to other works that mostly investigated the effect of annealing temperatures.[6,9,21−23] The blending strategy allows for common semiconducting polymers to be processed into thermally robust thin films to fabricate transistor devices that can function under thermal stress. This strategy thus offers the

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opportunity for facile fabrication of large-scale plastic electronics functional under extreme temperatures.

In this Letter, we demonstrate all-plastic, thermally stable transistor devices fabricated through a facile sequential layering of polyimide films. We utilized Kapton substrates as the support, solution-processed polyimide as the dielectric layer, and a thermally stable Matrimid-based blend as the functional semiconducting layer. With this fabrication strategy, we aim to not only facilitate and generalize the device fabrication process but also to reduce the mismatch in thermal expansions between different layers and, therefore, improve the overall thermal stability in all-plastic device assemblies. Figure 1a

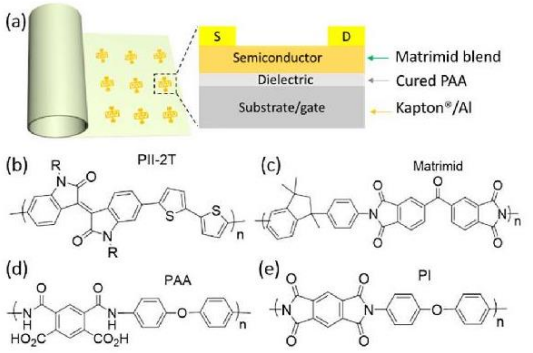

Figure 1. (a) Device architecture of an all-plastic transistor using polyimides. Molecular structure of (b) PII-2T, the conjugated polymer used in the semiconducting blends, (c) Matrimid, the high-T_g matrix, and (d) PAA used as the precursor for processing (e) the PI dielectric layer.

shows the transistor device architecture using all-polyimide components. Also shown are the molecular structures of (b) the semiconducting polymer (PII-2T), (c) Matrimid used as the host matrix in the channel layer, and (d) polyamic acid (PAA) used as the precursor solution to process polyimide (PI) as the dielectric layer (e). We selected Kapton as the plastic substrate because of its thermal durability, its flexibility, and most importantly, its compatibility with the dielectric layer. Kapton substrates were also available in different thickness gauges (25 μm for Kapton HN 100 and 125 μm for Kapton HN 500), which allows to tune the flexibility and the overall weight of the devices. We then chose polyimide as the dielectric component not only because it can be solution-processed from a readily available PAA precursor but also because it has previously demonstrated excellent thermal stability, excellent capacitive properties, and low power consumption in transistor devices.[12] We selected isoindigo, PII-2T, as the semiconducting polymer which was recently found to have heat resistant semiconducting properties on its own.[20] Finally, to improve the thermal stability of the semiconducting layer, while increasing its compatibility with the consecutive layers, we used Matrimid 5218 as the high-T_g host matrix and processed semiconducting blend films with PII-2T as demonstrated in our previous studies.[20]

We fabricated the transistor devices by, first, patterning and depositing Al gate contacts on cleaned Kapton substrates, followed by spin coating a PAA solution onto the device (Figure 2a). A smooth film (root-mean-square = 0.22 nm) of PI dielectric layer (Figure 2b) could be readily obtained after

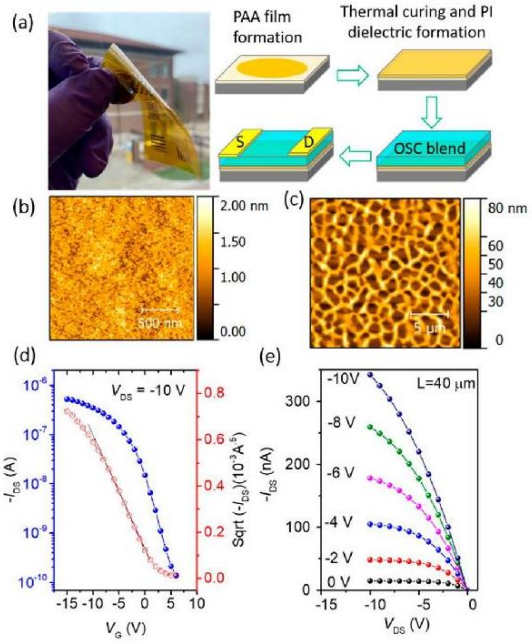

Figure 2. Proposed device fabrication route for all-plastic, polyimide-based transistor devices. (a) Micrograph of Kapton 100 substrates with patterned Al gates and the sequential layering device fabrication. AFM height image of (b) the very smooth thermally-cured dielectric layers and (c) the interpenetrating film of PII-2T/Matrimid blend processed on top of the PI dielectric. Characteristic (d) transfer curve and (e) output curve of the measured transistor devices showing ideal behavior, as well as low power consumption (V_{DS} of −10 V).

full imidization by thermal curing with a thickness of 200 nm (Figure S1) and a capacitance of 4.5 nF/cm^2 (Figure S2). The solvent resistance and robustness of the formed dielectric layer allowed to process the semiconducting layer on top. The Matrimid/PII-2T blend solution could be processed by spin coating from chloroform mixture yielding a ∼150 nm thin film (Figure S4). The blend formed a bicontinuous network in which the semiconducting polymer is surrounded by the high-T_g host (Figure 2c), a feature that has been shown to be beneficial for improving the thermal stability in thin films. After annealing the semiconducting layer, the device structure could be completed by depositing Au source/drain contacts. The fabricated transistor devices are flexible, light-weight with charge carrier mobilities as high as 0.20 cm^2/(V s), ON to OFF current ratios around 10^4, and threshold voltages of 3 V could be attained, while requiring operation voltages as low as 10 V (Figure 2d and e). Other properties, such as low hysteresis and low leakage currents, are also achieved (Figures S7 and S8).

To test the thermal stability of the fabricated plastic devices, we measured their electronic properties from room temperature up to 220 °C in ambient air. In typical electronics, such thermal stress will lead to uncontrolled increase in charge carrier density leading to excessive doping levels and carriers scattering resulting into the loss of the amplifying power of the transistor devices. Especially for conventional organic semiconductors, in this temperature regime, morphological

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fluctuations and thermal expansion normally will lead to significant decline in device performances.[8,23−25] Figure 3a

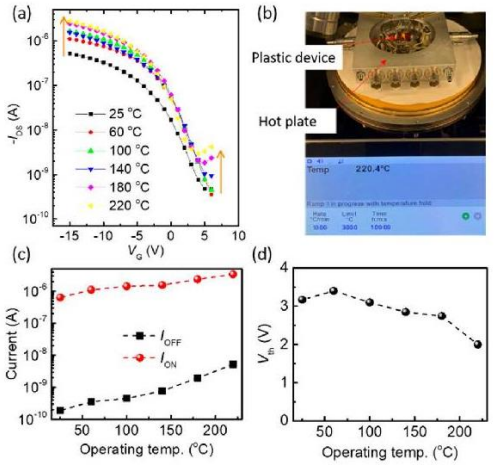

Figure 3. (a) Characteristic transfer current of the plastic device under different heating temperatures. Upon heating, the current increases indicative of a thermally activated behavior that remains stable even when the operating temperature reaches 220 °C. (b) In situ temperature-dependent device characterization set up with precise temperature control. Temperature-dependent (c) ON and OF currents and (d) threshold voltage of the transistor device measured in open air. Similar stable behavior could be observed on 10 other different devices.

shows the source/drain current with increasing temperature from our plastic transistor devices. Upon heating, the thermally-activated increase in the charge carrier density leads to increased ON and OFF currents, but our devices retain the ideal behavior and stable currents at all temperatures. These plastic devices can retain their I_{ON}/I_{OFF} even when operating at 220 °C in the open air (Figure 3c). The extracted threshold voltage also shows minimal variation as the operating temperature increases (Figure 3d). The in situ temperature-dependent capacitance study also revealed that the PI dielectric layer can retain its excellent capacitive behavior even when under baking conditions (Figure S2) in agreement with previous reports.[12] We attribute this excellent thermal stability of our plastic devices, first, to the compatibility in thermal expansion between all polyimide-based components of the transistor devices and, second, to the blending strategy, which enables the semiconducting polymer chains to remain confined by the polyimide host. This confinement in bicontinuous morphologies minimizes morphological variations and reduces carriers scattering.

To further test the thermal durability of our plastic devices, we tested the transistor properties under continuous heating at 195 °C equivalent to a baking oven environment. Upon baking, our transistors devices can retain ideal transfer and output characteristics as shown in Figure 4a and b. More importantly, these characteristics are retained after 2 h of heating in the open air. Figure 4c shows minimal to no change in the ON and OFF currents with increasing baking time. Similarly, the threshold voltage shows to remain around 3 V even after 2 h of heating (Figure 4d). In conventional

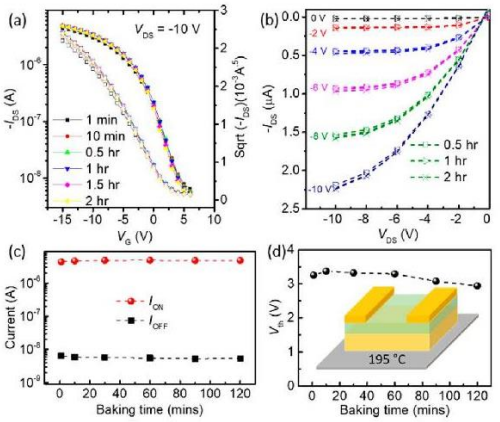

Figure 4. Characteristic (a) transfer and (b) output curves of a typical plastic transistor device measured with increasing heating time at 195 °C. The transistor devices exhibit minimal change in (c) current ratio and (d) the threshold voltage even after 2 h of constant baking. The same behavior was observed for 10 other different devices.

transistors, prolonged heating normally leads to increased charge carriers scattering and uncontrolled changes in threshold voltages resulting into increased power consumption. In our devices, the required operational voltage (V_{DS}) was kept at −10 V and the transistor devices could still exhibit excellent electronic properties. This ideality renders our approach an excellent candidate for high temperature sensing in which functional device components can sustain long-term heating with minimal power consumption.

To summarize, we have demonstrated a general, robust, and facile fabrication of all-plastic transistor devices that are thermally stable. We used polyimide components in all transistor layers and demonstrated a sequential stacking route enabling the facile fabrication of lightweight and flexible all-plastic electronics. Our devices exhibit electronic performance stable up to 220 °C and can sustain prolonged heating. We demonstrated that by utilizing semiconducting polymer blends and form thermally-robust blend composites, the amplifying power in transistor devices can be retained even under very harsh thermal conditions while requiring minimal power consumption.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsmaterialslett.9b00120.

Experimental details and supplemental figures showing thickness evaluation of the thermally-cured PI film using AFM, temperature-dependent capacitance measurements, morphology optimization in PII-2T/Matrimid blend films, thickness extraction of PII-2T film, optical micrographs of the steel shadow masks used for metal deposition and the plastic devices, statistical distribution of extracted mobility values, characteristic transfer curves, temperature-dependent source to drain and source to gate currents from the plastic device,

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characteristic transfer curves of devices measured at different operation temperatures in the open air, and characteristic output curves of devices measured at different operation temperatures in the open air (PDF)

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Notes

The authors declare no competing financial interest.

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Attaining Melt Processing of Complementary Semiconducting Polymer Blends at 130 °C via Side-Chain Engineering

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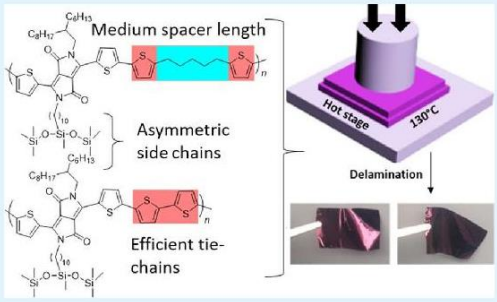
Supporting Information

ABSTRACT: Complementary semiconducting polymer blends (c-SPBs) have been proposed and tested to achieve melt-processed high-performance organic field-effect transistors (OFETs). Prior to this study, melt processing requires temperatures as high as 180 °C. To implement this technique into low-cost and large-area thin-film manufacturing for flexible organic electronics, semiconducting materials meltable at temperatures tolerable by ubiquitous plastic substrates are still needed. We report here the design and melt processing of a c-SPB consisting of a matrix polymer (DPP-CS) and its fully conjugated analogue. By utilizing a siloxane-terminated alkyl chain and a branched alkyl chain as solubilizing groups, the matrix polymer DPP-CS presents a melting temperature of 115 °C. The resulting c-SPB containing as low as 5% of the fully conjugated polymer could be melt-processed at 130 °C. The obtained OFET devices exhibit hole mobility approaching 1.0 $cm^2/(V\ s)$, threshold voltages below 5 V, and I_{ON}/I_{OFF} around 10^5. This combination of efficient charge-carrier transport and considerably low processing temperatures bode well for melt processing of semiconducting polymer-based organic electronics.



KEYWORDS: *melt processing, semiconducting polymers, side-chain engineering, organic field-effect transistors, low processing temperature*

INTRODUCTION

Organic field-effect transistors (OFETs) represent a promising alternative in designing integrated circuits for various applications in flexible electronics.[1−5] Solution-processable organic semiconductor materials have been used to achieve high performance required for practical applications.[6,7] OFETs have seen tremendous improvement in the past several years, surpassing the required mobilities for many device applications and even approaching the performance of amorphous silicon-based counterparts.[8,9] Solution processing has thus been an appealing route for thin-film formation in device fabrication as it can be easily achieved with high speed under ambient conditions; it has been envisioned to be a presumptive method for roll-to-roll printing. However, this approach is still plagued with some practical issues, such as the environmental issue, as most high-performing semiconductor polymers are mostly soluble in chlorinated solvents,[10,11] and poor morphology control, as the solvent evaporation rates dominate the film formation.[12,13]

To obviate these complications raised by the use of solvents, one of the proposed fabrication routes is solvent-free processing. For instance, methods such as melt processing, friction-transfer technique, and high-temperature rubbing have been demonstrated to be feasible in thin-film transistor fabrication.[14−16] Melt processing approach remains less appealing because most high-performing materials used in OFETs can only be melted at rather high temperatures.[16,17] In efforts to circumvent high-temperature ramping, polymer systems, such as regioregular polythiophenes, have been demonstrated to be blended with insulating matrices and achieve high-performance devices at considerably low processing temperatures.[18,19] In the first scenario, vertical phase segregation is often observed and utilized as a mean to increase the overall device performance by inducing crystallization of the semiconducting polymer within insulating matrices.[9,20−23] By blending low-performance semiconducting polymers (e.g., P3HT with insulating polymer matrices), in the second scenario, the induced crystallization can allow the formation of highly aligned nanowires, which leads to an increase in charge-carrier transport by several orders of magnitude, thereby achieving lowered processing temperatures.[19,23,24] These blending systems show promising device performances to serve as a material platform for melt processing; however, achieving the morphological stability and high charge-carrier mobility are challenging. For instance, melt crystallization will lead to undesired phase segregation.[16,25−27] There thus seems

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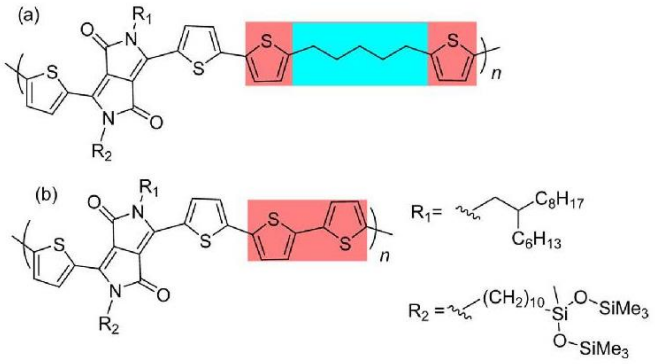

Figure 1. Molecular structures of (a) the matrix polymer: Si-C1C6C8-DPP-C5 and (b) the tie chain polymer: Si-C1C6C8-DPP-C0.

to be a lack of a semiconducting system that is both intrinsically high-performing and readily melt-processable.

Our research group has recently demonstrated a different approach to avoid phase segregation in melt processing by employing complementary semiconducting polymer blends (c-SPBs).[28] Zhao et al. reported a matrix polymer with a pentamethylene (C5) conjugation-break spacer utilized to be blended with a small portion of its fully conjugated analogue. This binary system showed no phase separation and excellent morphology stability due to structural complementarity between the tie polymer and the host matrix. However, the melt processing of this pair could only be realized at elevated temperatures (160 °C and above) as the matrix polymer alone melts around 140 °C. Such a high temperature makes it difficult to integrate these blends to low-cost, large-scale printing techniques, where low processing temperatures[4] (typically lower than 150 °C) are desired. For instance, Zardetto et al. demonstrated that the physical and electrical properties of most commonly used substrates (as well as their indium tin oxide (ITO)-modified analogues) can be greatly impeded at temperatures above 150 °C.[29] Both poly(ethylene terephthalate) and poly(ethylene naphthalate), two of the most commonly used substrates, showed to start bending upon thermal treatment higher than 150 °C. More importantly, the ITO-modified sheets of these polymer substrates showed an exponential increase in electrical resistance concomitant to the bending.[29] To attain this substrate–semiconductor compatibility, lower processing temperatures, lower than 150 °C, would be ideal. Besides, lowering the processing temperatures would translate to reducing the inherent energy consumption associated with the use of high-temperature ramping for large-scale manufacturing. To make melt processing a promising and potential candidate for organic electronics and to fulfill an easier, greener, and low-cost processing, lower-melting-point and high-performance semiconducting polymer systems are still urgently needed. Achieving such a semiconducting system would obviate the need for post-processing treatment steps and allow for the practical use of melting in electronic thin-film manufacturing.

One way to lower the melting temperatures of the matrix polymers would be to increase the spacer length, but semiconducting properties would then be compromised.[30] Alternatively, side-chain engineering has been demonstrated by our group as a tool to tune the melting point of matrix polymers.[31] Notably, the use of asymmetric side chains showed to yield lower melting temperature for a DPP matrix polymer with five methylene units. Here, we report the design and melt processing of c-SPBs consisting of a DPP-C5 matrix bearing asymmetric side chains as solubilizing groups and its fully conjugated analogue. With a siloxane-terminated alkyl chain on one side and a branched alkyl chain on the other side, the matrix polymer showed a melting temperature as low as 115 °C. Melt-processed OFET devices of the resulting c-SPBs with charge-carrier mobilities approaching 1.0 $cm^2/(V\ s)$, I_{ON}/I_{OFF} greater than 10^5, and threshold voltage below 5 V could be fabricated at 130 °C with no post-treatment steps required. To our knowledge, this is the first intrinsically semiconducting polymer system to be melt-processed at such low temperatures with such electrical and film stability behavior. By combining the ability to be melt-processed at significantly low temperatures and the potential to yield high-performance OFET devices, this system opens the door for robust and sustainable processing routes in organic electronic thin-film manufacturing.

■ RESULTS AND DISCUSSION

Materials Design, Synthesis, and Characterization. As previously demonstrated, conjugation break spacers can be used to tune polymer backbone flexibility as well as their melting temperatures. Zhao et al. demonstrated that π-conjugation in semiconducting polymers can be intentionally interrupted by placing an alkyl chain along the polymer backbone, yielding melt-processable semiconducting polymer thin films and fibers.[30,32] In a subsequent study, we demonstrated that asymmetric side chains could yield lowered melting transitions for the same polymer backbones.[31] In this study, a DPP-based matrix polymer with a five-carbon (five methylene units) flexible spacer affording sufficient backbone flexibility was selected.[30,31,33] A branched alkyl chain placed two carbons away from the backbone (C1C6C8–) and an elongated alkyl chain with a siloxane terminal group (Si–) were then used as the solubilizing chains. This breaking of symmetry in side chains has been also recently found to be beneficial for yielding mixed orientations and improved charge transport in isoindigo-based donor–acceptor systems.[34] The molecular structure of the matrix polymer, Si-C1C6C8-DPP-C5, is shown in Figure 1a. The same solubilizing side chains were then utilized for the fully conjugated (tie-chain) polymer, which was subsequently chosen to make the corresponding melt-processable blends. The complementary tie-chain polymer, Si-C1C6C8-DPP-C0, is shown in Figure 1b. Both polymers were prepared as previously reported[30,35] and were fully characterized using NMR, UV–vis

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Table 1. Physical Characterization of Si-C1C6C8-DPP-C5, Si-C1C6C8-DPP-C0, and Their 5% c-SPB

material	M_n (kDa)/$Đ$	T_d (°C)	T_m (°C)	λ_{max} (nm) solution[b]	λ_{max} (nm) film[c]	energy levels (eV) E_{HOMO}[d]	energy levels (eV) E_{LUMO}[e]
Si-C1C6C8-DPP-C5	19.1/1.2[a]	411	125	589, 626	591, 628	−5.19	−3.81
Si-C1C6C8-DPP-C0	5.8/1.2[f]	417		733, 799	749, 822	−4.95	−3.55
5% c-SPB	NA	417	132	618, 671	622, 674		

[a]Tetrahydrofuran is used as the eluent at room temperature. [b]Chloroform used as the solvent. [c]Drop-casted films on glass substrates. [d]Obtained from ultraviolet photoelectron spectroscopy, uncertainty ±0.05 eV. [e]Calculated using the equation $E_{LUMO} = E_{HOMO} + E_g^{opt}$. [f]Trichlorobenzene used as the eluent at 150 °C.

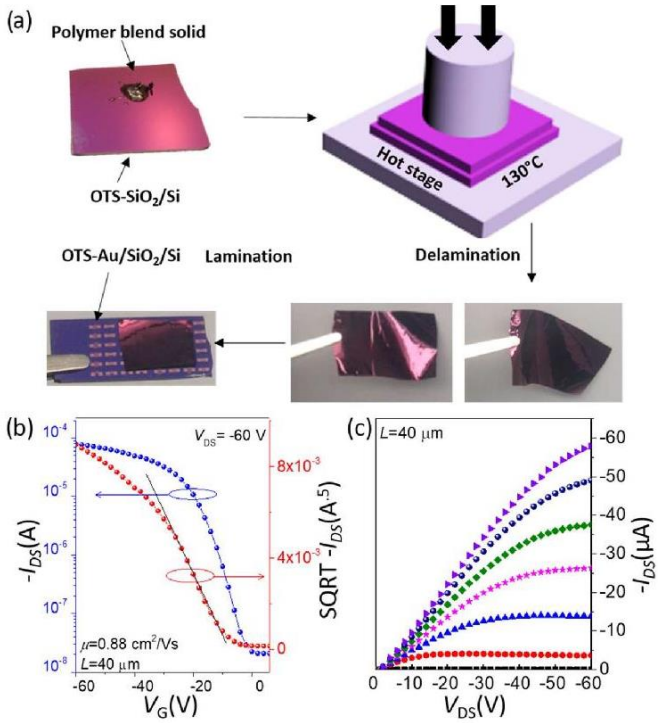

Figure 2. (a) Illustration of the thin film formation by melt pressing and OFET fabrication by delamination−lamination method. Characteristic transfer (b) and output (c) curves of the best-fabricated OFET device based on the polymer c-SPB.

absorption, and gel permeation chromatography. The characterization results can be found in the Supporting Information, and the physical properties are summarized in Table 1.

Physical blends of Si-C1C6C8-DPP-C5 and Si-C1C6C8-DPP-C0 were used to demonstrate the melt processing of OFET devices. From differential scanning calorimetry (DSC) (the second cycle) results (Figure S5), Si-C1C6C8-DPP-C5 showed a melting transition with the peak maximum around 125 °C. By blending 5% of the tie chains into the matrix polymer, the designed blend system showed a melting point slightly higher than that of the pure matrix with a peak maximum shift of ~7 °C. The fully conjugated polymer did not show any notable thermal transitions before 350 °C. Thermogravimetric analysis showed that Si-C1C6C8-DPP-C0 is thermally stable up to 417 °C (Figure S4). This thermal behavior of 5% c-SPB different from that of the pure matrix polymer is an indication of the lack of polymer phase separation, which is in good agreement with previously reported DPP-based blends. The 5% c-SPB was further utilized to investigate the melt processing of OFET devices at temperatures near the melting point of the blend system.

OFET Characterization. Melt-processed devices were fabricated as follows.[28] Briefly, Si/SiO_2 substrates with Au electrodes were first cleaned using piranha solution (2 vol 18 M sulfuric acid: 1 vol 30% hydrogen peroxide), followed by copious rinsing with water and then sonicated in isopropanol and acetone each for 5 min. The cleaned and dried substrates were then modified with a self-assembled monolayer of octadodecyltrichlorosilane (OTS). Bottom gate, bottom contact OFET devices were then fabricated by melt processing inside a N_2 glovebox, as illustrated in Figure 2a. The polymer blends were first allowed to mix in their solutions. Approximately 5 mg of the dried blended solid was used to form a thin film of a polymer blend by melting at 130 °C inside the N_2 glovebox.

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Table 2. Representative OFET Parameters for Devices Based on the Pure Matrix Polymer (Si-C1C6C8-DPP-C5), the Tie-Chain Polymer (Si-C1C6C8-DPP-C0), and the Resulting c-SPB when 5, 10, and 50 wt % of Si-C1C6C8-DPP-C0 are Used

material	μ_{max} ($cm^2/(V\ s)$)	μ_{avg} ($cm^2/(V\ s)$)	V_{th} (V)	I_{ON}/I_{OFF}
Si-C1C6C8-DPP-C5	6.50×10^{-3}	3.01×10^{-3}	-8.1 ± 2.0	$\sim 10^6$
5% c-SPB	0.57	0.20	-5.7 ± 2.4	$\sim 10^5$
10% c-SPB	0.75	0.48	-4.4 ± 1.6	$\sim 10^5$
50% c-SPB	0.88	0.62	-3.3 ± 1.8	$\sim 10^4$
Si-C1C6C8-DPP-C0[a]	2.89	1.35	-2.6 ± 1.0	$\sim 10^4$

[a]Drop-casted films.

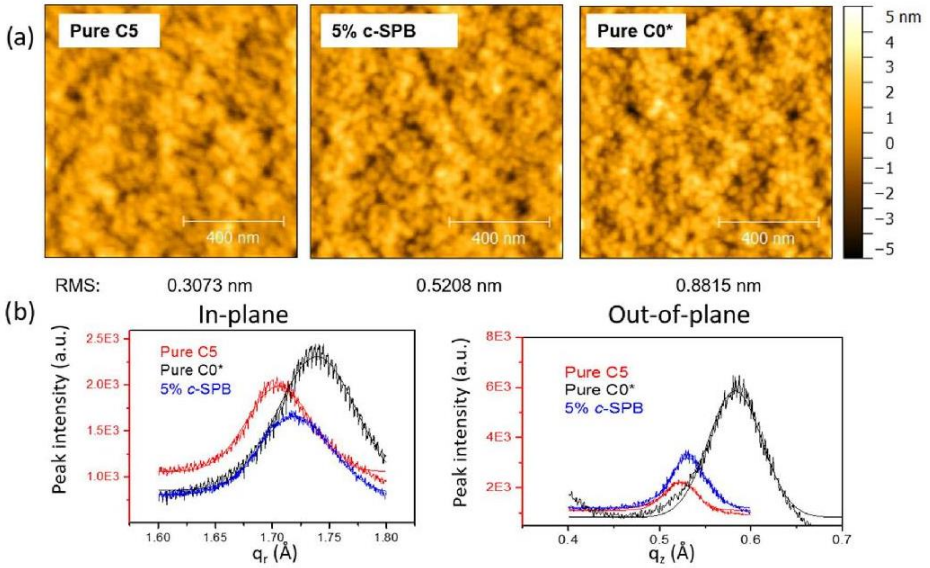

Figure 3. (a) AFM height images of the melt-processed thin films. (b) Selected peak line cuts of 2D diffraction patterns for comparison of in-plane π-stacking peaks and out-of-plane lamellar stacking peaks for pure Si-C1C6C8-DPP-C5, 5% c-SPB, and Si-C1C6C8-DPP-C0 (* indicates drop-casted film).

To yield a thin film, the dry polymer blend pellets were deposited on a cleaned and OTS-modified Si/SiO_2 and then sandwiched using a secondary clean substrate. The assembly was then allowed to fully melt at 130 °C while being pressed using a heavy object (10 kN/cm^2) for 2 h. Upon delamination, the thin film was transferred onto a cleaned and OTS-modified Si/SiO_2 substrate with Au electrodes to fabricate OFET device. To establish intimate contact between the substrate and the laminated films and eliminate any surfaces defects, the devices were placed on a hot plate (at 100 °C for an extra 15 min). For the devices based on the pure fully conjugated polymer, because the polymer could not be melted, the OFET devices were fabricated by drop casting, followed by a hot-pressing step at 130 °C for comparison. All OFET devices were then allowed to cool to ambient prior to electrical properties measurements. In the same manner, thin films used for atomic force microscopy (AFM) and grazing incidence X-ray diffraction (GIXRD) were prepared for further analysis.

The blending efficiency was studied using the 5, 10, and 50% c-SPB-based OFET devices. The representative OFET performance parameters are summarized in Table 2. Due the persistent dual-slope commonly observed for the DPP-based polymers,[12,28] the mobility values were evaluated in both low- and high-gate-voltage regimes; the calculated mobilities for higher-gate-voltage regimes are summarized in Table S1. The corresponding characteristic transfer and output curves are provided in Figure S6 along with dual sweep hysteresis analysis. Pure Si-C1C6C8-DPP-C5 showed a maximum mobility of 6.5×10^{-3} $cm^2/(V\ s)$, whereas Si-C1C6C8-DPP-C0 could reach mobilities up to 2.89 $cm^2/(V\ s)$ for a drop-casted film.

The charge-carrier mobility could be boosted by 2 orders of magnitude when as low as 5% of Si-C1C6C8-DPP-C0 was added. The mobility values then plateaued upon further increase of the amount of the added tie chains, as shown in Table 2. The c-SPB containing 50% of DPP-C0 showed hole mobility values reaching as high as 0.88 $cm^2/(V\ s)$ when melt-pressed at 130 °C. Other parameters, including the threshold and the I_{ON}/I_{OFF} current ratios, were also moderate, as shown in Table 2. The addition of a small portion of the rigid tie-chain polymer in the blend showed to be sufficient to increase the electronic properties of the matrix polymer, as seen in other DPP-based blends.[28,35]

Morphology Studies. To elucidate the charge-transport efficiency in the melt-processed devices and investigate the miscibility of polymers upon melt crystallization, morphology studies as well as molecular packing analysis in thin films were conducted using AFM and GIXRD. The topographic images showed that the melted films were smooth upon delamination

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(Figure 3a). No detectable phase separation between the two polymers could be observed, which is in a good agreement with the DSC data. These morphology behaviors were not surprising, as from Figure 2a, all of the thin films showed a metallic luster after melt pressing. This film smoothness was desired for the transfer and lamination step to ensure intimate contact between the film and the substrate. The free-standing films (Figure 2a) could thus be easily used in the lamination step as opposed to noncomplementary systems, where the dual-layer formation would require extra steps to access the semiconducting layer.[24] The in-plane and out-of-plane two-dimensional (2D) GIXRD diffraction patterns as well as the corresponding one-dimensional (1D) curves are shown in Figure S7. Key peaks extracted from the 1D curves comparing the crystallinity of the pure matrix, the 5% c-SPB, as well as the pure tie polymer are shown in Figure 3b. Even though spin casting is normally preferred for polymer diffraction studies, thicker (~1.5 μm) melt-processed films were chosen here to gain insights into the packing mechanism upon melting and cooling. For the same reason, drop-casted and hot-pressed Si-C1C6C8-DPP-C0-based films were used for a comparison. The melt-processed and thus thicker films based on Si-C1C6C8-DPP-C5 and 5% c-SPB gave ringlike diffraction patterns that indicated a broad distribution of out-of-plane orientation of crystalline aggregates. However, lower degree of out-of-plane alignment is not intrinsic to melt-processed films but is instead attributed to lack of confinement in thicker films. Therefore, much thinner spin-cast films were utilized for comparison and used to validate the extracted peak positions (Figure S7). From the 2D patterns of the melt-processed thin films, representative crystallography parameters were carefully extracted and summarized in Table 3.

Table 3. Crystallography Parameters for Melt-Processed Thin Films of Si-C1C6C8-DPP-C5, 5% c-SPB, and Si-C1C6C8-DPP-C0

material	$\pi-\pi$ spacing (Å)	in-plane FWHM ($Å^{-1}$)	lamellar spacing (Å)	out-of-plane FWHM ($Å^{-1}$)
Si-C1C6C8-DPP-C5	3.68	0.065	24.7	0.042
5% c-SPB	3.65	0.074	23.7	0.046
Si-C1C6C8-DPP-C0[a]	3.61	0.080	21.5	0.070

[a]Drop-casted thin film.

Si-C1C6C8-DPP-C5 showed an in-plane $\pi-\pi$ stacking peak appearing at 1.70 $Å^{-1}$ corresponding to a packing distance of 3.68 Å. A $\pi-\pi$ stacking could also be observed in the out-of-plane direction at 1.70 $Å^{-1}$ due to the large thickness of the film, as previously mentioned. Also along q_z, a (100) lamellar stacking peak could be found at 0.258 $Å^{-1}$ corresponding to a *d*-spacing of 24.70 Å. This large lamellar spacing was expected because the spacer group along the polymer chain was intentionally made long, and bulky side chains were used.[32] Hot-pressed Si-C1C6C8-DPP-C0 showed a clear edge-on orientation with a well-defined $\pi-\pi$ stacking peak at 1.74 $Å^{-1}$, corresponding to a shorter *d*-spacing of 3.61 Å. The lamellar stacking peak appeared around 0.291 $Å^{-1}$ corresponding to a *d*-spacing of 21.52 Å. Upon blending the two polymers in a 5% c-SPB, the GIXRD patterns showed a weak edge-on orientation with the in-plane $\pi-\pi$ stacking peak around 1.72 $Å^{-1}$ corresponding to a packing distance of 3.65 Å. The out-of-plane lamellar peak moved to 0.266 $Å^{-1}$ with a *d*-spacing of 23.69 Å. The presence of the small fraction of Si-C1C6C8-DPP-C0 in the blend thus shortened the $\pi-\pi$ stacking distance as well as the lamellar spacing by 0.04 and 1.01 Å, respectively. This close packing in c-SPB contributed to the increase in hole mobility by 2 orders magnitude in the 5% c-SPB in addition to the formation of tie chains. It could be concluded that not only does the tie-chain polymer serve as a connecting bridge between crystalline domains of the matrix polymer,[36] but also it also seems to play a crucial role in the melt crystallization of the blend. This behavior had previously been observed in a similar DPP-based system using in situ temperature-dependent GIXRD analysis[28] and could thus rationalize the increase in charge-carrier mobility.

CONCLUSIONS

We demonstrated the melt processing of complementary semiconducting polymer blends at 130 °C. The blend gave hole mobilities as high as 0.88 $cm^2/(V\ s)$ with low threshold voltages and high I_{ON}/I_{OFF} ratios in hot-processed and laminated OFET devices. The low melting temperatures were achieved by utilizing asymmetrical solubilizing side chains in combination with an elongated conjugation break spacer. Morphology studies were used to elucidate the observed high charge-carrier mobility in the polymer blends. This processing of organic semiconductors at unprecedented low temperature renders this method adaptable to ubiquitous plastic substrates and significantly lowers the energy consumption. This design thus opens up opportunities in solvent-free processing as a more suitable route for low-cost and large-area formation of semiconducting thin film and organic electronic manufacturing.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b19847.

Detailed physical characterization experiments (PDF)

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Notes

The authors declare no competing financial interest.

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