APPLICATIONS OF TWO-DIMENSIONAL LAYERED MATERIALS IN INTERCONNECT TECHNOLOGY

by

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Dedicated to my family

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ABSTRACT

Copper (Cu) has been used as the main conductor in interconnects due to its low resistivity. However, because of its high diffusivity, diffusion barriers/liners (tantalum nitride/tantalum; TaN/Ta) must be incorporated to surround Cu wires. Otherwise, Cu ions/atoms will drift/diffuse through the inter-metal dielectric (IMD) that separates two distinct interconnects, resulting in circuit shorting and chip failures. The scaling limit of conventional Cu diffusion barriers/liners has become the bottleneck for interconnect technology, which in turn limits the IC performance. The interconnect half-pitch size will reach ~20 nm in the coming sub-5 nm technology nodes. Meanwhile, the TaN/Ta (barrier/liner) bilayer stack has to be > 4 nm to ensure acceptable liner and diffusion barrier properties. Since TaN/Ta occupy a significant portion of the interconnect cross-section and they are much more resistive than Cu, the effective conductance of an ultra-scaled interconnect will be compromised by the thick bilayer. Therefore, two dimensional (2D) layered materials have been explored as diffusion barrier alternatives owing to their atomically thin body thicknesses. However, many of the proposed 2D barriers are prepared at too high temperatures to be compatible with the back-end-of-line (BEOL) technology. In addition, as important as the diffusion barrier properties, the liner properties of 2D materials must be evaluated, which has not yet been pursued.

The objective of the thesis is to develop a 2D barrier/liner that overcomes the issues mentioned. Therefore, we first visit various 2D layered materials to understand their fundamental capability as barrier candidates through theoretical calculations. Among the candidates, hexagonal-boron-nitride (h-BN) and molybdenum disulfide (MoS_2) are selected for experimental studies. In addition to studying their fundamental properties to know their potential, we have also developed techniques that can realize low-temperature-grown 2D layered materials. Metal-organic chemical vapor deposition (MOCVD) is adopted for the synthesis of BEOL-compatible MoS_2. The electrical test results demonstrate the promises of integrating 2D layered materials to the state-of-the-art interconnect technology. Furthermore, by considering not only diffusion barrier properties but also liner properties, we develop another 2D layered material, tantalum sulfide (TaS_x), using plasma-

enhanced chemical vapor deposition (PECVD). The TaS_x is promising in both barrier and liner aspects and is BEOL-compatible. Therefore, we believed that the conventional TaN/Ta bilayer stack can be replaced with an ultra-thin TaS_x layer to maximize the Cu volume for ultra-scaled interconnects and improve the performance. Furthermore, Since via resistance has become the bottleneck for overall interconnect performance, we study the vertical conduction of TaS_x. Both the intrinsic and extrinsic properties of this material are investigated and engineering approaches to improve the vertical conduction are also tested. Finally, we explore the possibilities of benefiting from 2D materials in other applications and propose directions for future studies.

1. INRODUCTION

1.1 State-of-the-art Cu Interconnect Technology and its Challenges

Ever since the inventions of transistors and integrated circuits (ICs), the computational capability has been escalating in a remarkable way, which tremendously changes human beings' lives. This is attributed the well-known Moores' Law, which predicts the number of transistors doubles approximately every eighteen months. Originally, the success of keeping the growth rate was realized by continuing scaling down transistors' dimensions. However, the increased challenges of transistor scaling as well as the scaling of other parts of an IC have slowed down the growth rate. In an IC chip, the regions consisting of transistors is also known as the front-end-of-line (FEOL). However, different transistors must be connected to each other to perform certain computational functions. The connecting bridges between transistors are called "interconnects." Interconnects are metal wires with various lengths, widths, and thicknesses, depending on the vertical levels they are located in an IC chip. Copper (Cu) has been the material of choice for interconnects in today's IC chips for more than 20 years. Before the integration scheme for Cu interconnects was available, aluminum (Al) was the main conductor for interconnects. However, with increasing demands of lower resistivity and better electromigration endurance, Al was eventually replaced with Cu in late 1990s, after many challenges of integration had been overcome. The regions consisting of interconnects is known as the back-end-of-line (BEOL). The top-view and cross-section of an IC chip are shown in Fig. 1.1. It clearly shows that transistors are in the very bottom level while there are many levels of interconnects above transistors. It can also be observed that these interconnects are buried in trenches surrounded by dielectrics, which is also known as the "Damascene Structure". The standard Damascene process is depicted in Fig. 1.2(a), which begins with the formation of trenches by etching the inter-metal dielectrics (IMDs). Next, barrier/liner (TaN/Ta) layers are deposited in these trenches followed by the deposition of a thin copper seeding layer. With the assistance of the seeding layer, the trenches are then filled with copper through electroplating. Finally, chemical mechanical polishing (CMP) is used to remove the excess Cu from the top of the trenches. The cross-section of a single interconnect is illustrated in Fig. 1.2(b). On the top of Cu, a capping layer (typically, SiN_x, Co, CoWP, etc.) is deposited to alleviate the damages from the CMP process. The purpose of barrier and liner layers will be

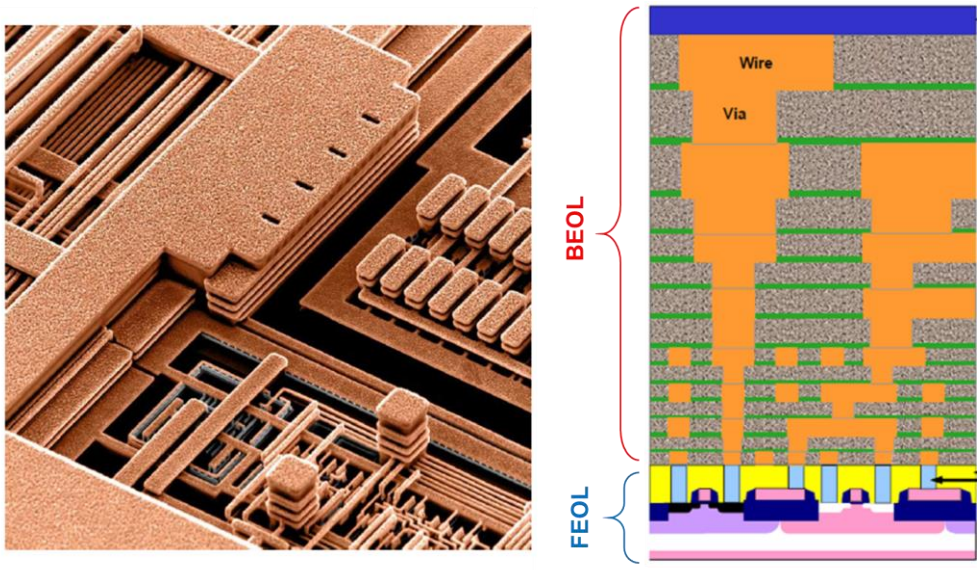


Fig. 1.1 (left) Scanning electron microscope (SEM) image of the multi-level Cu interconnects fabricated using the damascene process (courtesy: IBM Corp.). (right) Cross section of an IC chip, where multiple layers of interconnects can be observed on top of the transistor level [1] (courtesy: International Technology Roadmap for Semiconductors, ITRS).

introduced in the following paragraph. Note: although Cu electroplating is considered in the thesis, the current technology is using "Cu reflow" as the new approach for Cu formation [2].

Although transistor scaling contributed to the continued scaling of an IC chip, the scaling of interconnects has become the bottleneck in recent years. Because of the high diffusivity of Cu, diffusion barriers must be incorporated to surround Cu wires. Otherwise, Cu ions/atoms will drift/diffuse through the IMDs that separates two distinct interconnects, resulting in circuit shorting. Conventionally, tantalum nitride (TaN) has been adopted as the diffusion barrier owing to its superior capability of blocking Cu diffusion [3], [4]. However, the adhesion of Cu to TaN is not ideal. To address this issue, tantalum (Ta) has been integrated in-between TaN and Cu to improve the adhesion. The optimized stack consists of a TaN layer deposited on low-*k* dielectrics, followed by a Ta layer before the Cu deposition, as depicted in Fig. 1.2(b). The barrier/liner (TaN/Ta) bilayer has been demonstrated to fulfill several requirements of the interconnect technology [3]. With the advent of sub-5 nm technology nodes, the interconnect half-pitch size will reach ~20 nm and below [1]. Meanwhile, the thickness of the conventional TaN/Ta bilayer cannot be reduced below ~4 nm just to maintain its capability of blocking Cu diffusion into the IMDs [5]. However, the TaN/Ta bilayer is much more resistive than Cu. In ultra-scaled Cu interconnects, TaN/Ta will occupy a large

portion of the cross-section area, which tremendously increases the line resistance, as shown in Fig. 1.3. The main challenge of scaling conventional TaN/Ta lies in their three-dimensional (3D) nature, which makes atomically thin and continuous TaN/Ta stack difficult to achieved fundamentally. Throughout this dissertation, I will discuss how 2D layered material can overcome this bottleneck.

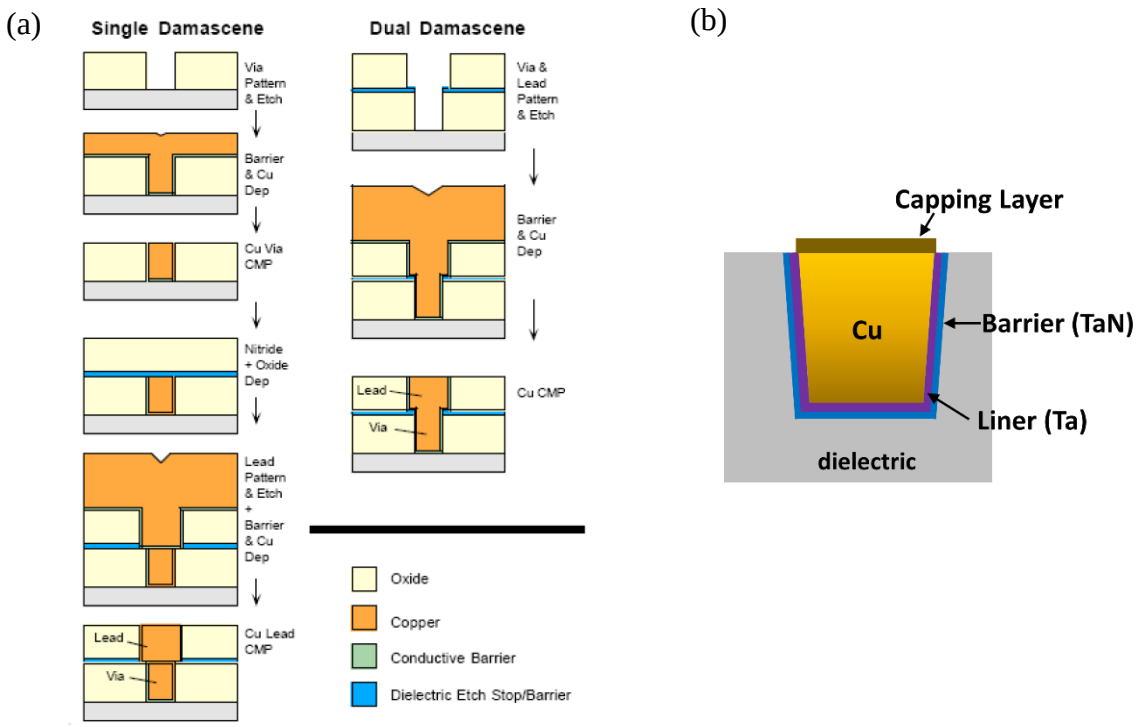


Fig. 1.2 (a) Process flows of the formation of the Damascene Structure. (b) Schematic of the cross-section of a Cu interconnect. A resistive barrier/liner bilayer surrounds Cu and occupies a certain portion of the interconnect.

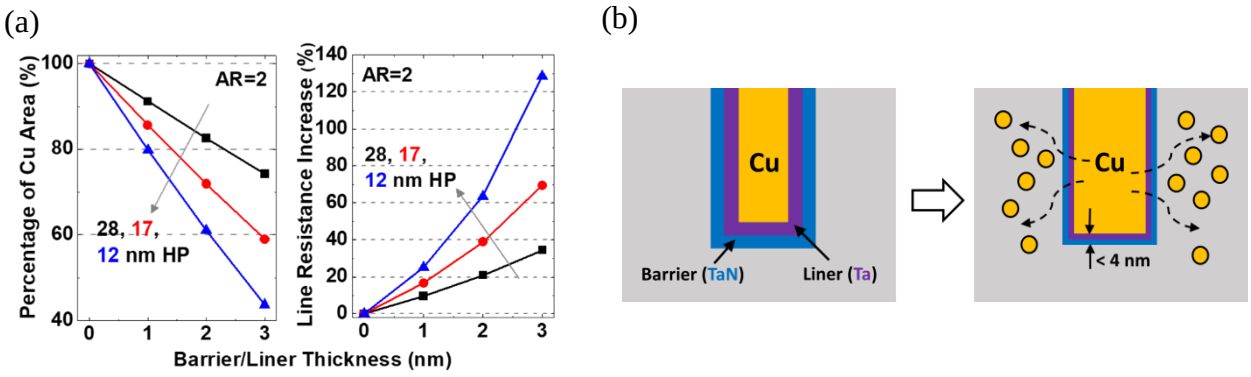


Fig. 1.3 (a) Percentage of Cu area (left) and increase in line resistance (right) in a single interconnect Damascene trench with various barrier/liner thicknesses and half-pitch (HP) sizes. Aspect ratio (AR) of the trench is fixed at 2. Line resistance drastically increases in extremely scaled interconnects with thicker barrier/liner. (b) Schematic of severe Cu diffusion as the thickness of a conventional TaN/Ta diffusion barrier/liner is scaled.

1.2 Introduction to Two-dimensional Layered Materials

Two-dimensional (2D) layered materials, such as graphene [6], hexagonal-boron nitride (h-BN) [7] and transition metal dichalcogenides (TMDs) [8], [9], possess atomically thin body thicknesses. A few examples of these materials are shown in Fig. 1.4, even though tens of 2D materials have been discovered. The underlying reason that these materials can achieve the thicknesses is the van der Waals force interaction between layers. Unlike three-dimensional (3D) materials, where different atoms are normally bonded by covalence or ionic bonds, the van der Waals force interaction between 2D layers makes it possible and easier to separate layers from each other. The original interest of this atomically thin layer arose from the demand of a superior gate electrostatic control for extremely scaled transistors. A great number of achievements of decent transistor characteristics using 2D materials as the channel materials have been demonstrated over the past few years [10], [11]. To demonstrate field-effect transistors (FETs) with high performance, the 2D layers are normally exfoliated from chemical vapor transport (CVT) prepared bulks to ensure highest possible film quality. The sizes of these 2D "flakes" are normally in micrometer scale.

In addition to the applications for FETs, the 2D nature of these materials inspires people of using them as Cu diffusion barriers to solve the obstacle mentioned in the previous section. Early demonstrations of using graphene as Cu diffusion barrier demonstrates the materials' potential [12]–[14]. However, to evaluate the feasibility of integrating these novel 2D layered materials with the existing Cu interconnect technology, a wide variety of aspects needed to be evaluated, which is the focus of this dissertation.

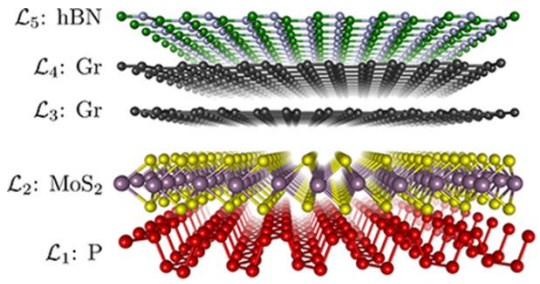


Fig. 1.4 Examples of 2D layered materials. The van der Waals force interaction between layers makes it possible to separate layers from each other and realize atomically thin films. Reprinted with permission from Cancès *et al.* J. Math. Phys. **58** (2017) Copyright @ 2017 American institute of Physics.

1.3 Motivation of Integrating 2D Layered Materials with Cu Interconnects

As pointed out in Section 1.1, the fundamental obstacles of using conventional barrier/liner lie in their 3D nature. Given their atomically thin nature, it is intuitive to consider 2D layered materials as diffusion barrier alternatives. Our early work has demonstrated that graphene has a superior capability of blocking Cu diffusion despite its atomic thickness [15]. Figure 1.5(a) illustrates the test structure and method, where a constant electric field is applied across the capacitor structure to drive Cu ions into the dielectric. The presence of positively charged Cu ions results in a flat-band voltage (V_{FB}) shift that can be observed in a capacitance-voltage (C-V) measurement, as shown in Fig. 1.5(b). It is observed that with graphene being inserted in-between Cu and the dielectric, V_{FB} shift can be largely suppressed, indicating graphene blocks Cu diffusion. In addition, by encapsulating Cu with graphene, it has been shown that the electrical and thermal conductivity of Cu are enhanced due to suppression of the surface scattering between Cu and the barrier/liner [16], as the resulted briefly summarized in Fig. 1.6.

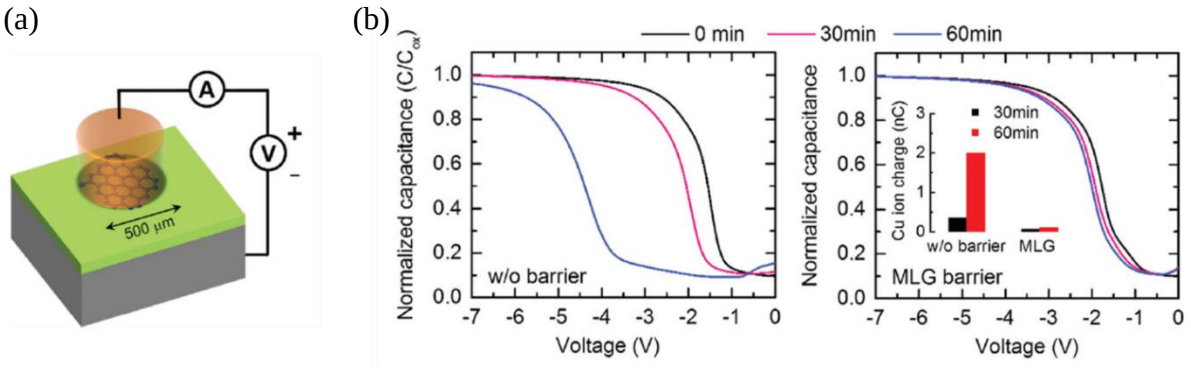


Fig. 1.5 (a) Metal-oxide-semiconductor (MOS) capacitor structures used for Cu diffusion tests. Graphene is inserted in-between Cu and SiO_2 for the devices with barrier while the control devices have no graphene. (b) After the electrical stressing, devices without graphene show obvious flat-band voltage (V_{FB}) shift, indicating significant Cu diffusion. Devices with graphene barrier show negligible V_{FB} shift due to suppression of Cu diffusion. Reprinted with permission from Mehta *et al.* Nanoscale **9** (2017) Copyright @ 2017 Royal Society of Chemistry.

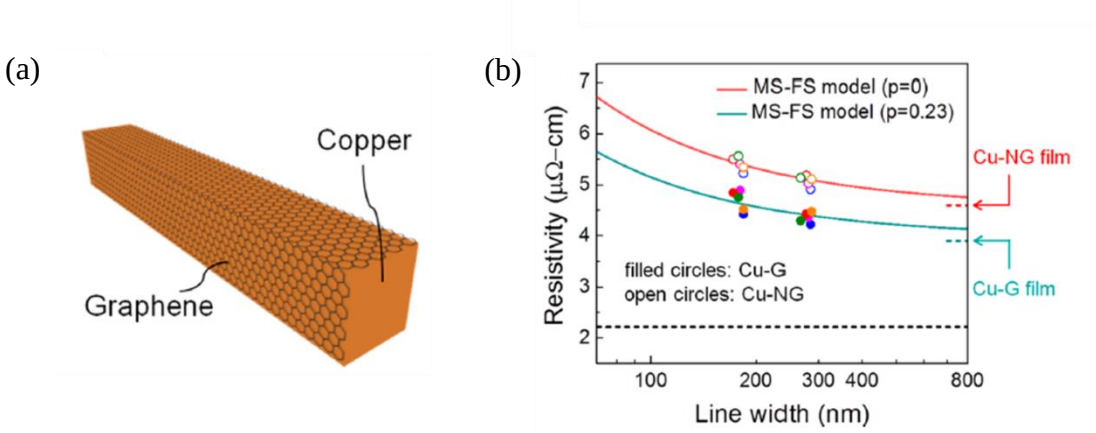


Fig. 1.6 (a) Cu nanowire encapsulated by graphene. (b) With the encapsulation of graphene, the resistivity of Cu nanowires decreases due to the suppression of surface scattering. Reprinted with permission from Mehta *et al.* Nano Lett. **15** (2015) Copyright @ 2015 American Chemical Society.

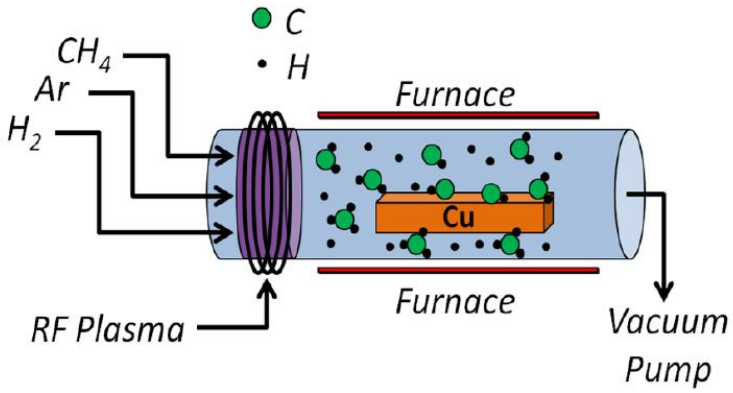


Fig. 1.7 Schematic of the plasma-enhanced chemical vapor deposition (PECVD) system for graphene growth. Cu substrate is illustrated here only as an example. Growth on other substrates is also possible. Reprinted with permission from Mehta *et al.* Nano Lett. **15** (2015) Copyright @ 2015 American Chemical Society.

Despite the abovementioned advantages of graphene, in the meantime, a group of 2D layered materials exists, whose properties are complementary yet distinct from those of graphene. Theoretical calculations predict high-energy barriers in some of these materials to prevent molecule diffusion [17], [18]. Inspired by the graphene works, in this dissertation, the discussions will focus on diffusion barrier properties as well as other properties of different 2D layered materials. In addition, the syntheses of BEOL-compatible 2D materials is also one of the main focuses in this thesis. Our previous work has demonstrated that low-temperature grown graphene can be realized by utilizing the energy of plasma since plasma can dissociate carbon bonds so that high temperatures are not required to provide thermal energy [19]. The plasma-enhanced chemical vapor deposition (PECVD) system is depicted in Fig. 1.7. Similar approaches are adopted for the low-temperature syntheses of other 2D materials. In short, this thesis covers aspects of material synthesis, material/electrical characterizations, and various techniques of evaluating 2D materials' properties, such as diffusion barrier and liner properties.

1.4 Synopsis of the Thesis

The description of my work starts from Chapter 2, where the intrinsic diffusion barrier properties of 2D layered material other than graphene are evaluated. First principle density functional theory (DFT) calculations are utilized to estimate the potential of various 2D layered materials. The results demonstrate promising diffusion barrier properties of many of the candidates. The materials selected for experimental studies include hexagonal-boron-nitride (h-BN) and molybdenum disulfide (MoS_2). Intrinsic diffusion barrier properties of these films are investigated by conducting the standard reliability test vehicle, time-dependent dielectric breakdown (TDDB) measurements on high-quality films. The results show superior diffusion barrier properties of these two materials. Moreover, STEM (scanning transmission electron microscopy) in conjunction with EDS (energy dispersive X-ray spectroscopy) and EELS (electron energy loss spectroscopy) are used for structural analysis and compositional/chemical mapping of the interface and inter-diffusion processes. This work was carried out in collaboration with Prof. Strachan and his group at Purdue University, Prof. Eric Pop and his group at Stanford University, and Prof. Moon Kim and his group at the University of Texas at Dallas.

Next, in Chapter 3, MoS_2 barrier grown at low temperature (400 °C) compatible to the technology is demonstrated. Unlike Chapter 2, where the fundamental properties of 2D are studied using highest-possible-quality films grown at high temperatures, this chapter focuses on realizing a BEOL-compatible 2D barrier. The growth method, material characterizations, and barrier property tests are discussed. In addition, this low-temperature grown MoS_2 is compared with the high-temperature grown one in Chapter 2 for their diffusion barrier properties. This work was carried out in collaboration with Prof. Joshua Robinson and his group at Pennsylvania State University, as well as Dr. Ryan Scott Smith and Ketan Shah at Globalfoundries.

In Chapter 4, another 2D layered material, tantalum sulfide (TaS_x) is discussed. The reason of choosing TaS_x is not only because of its superior diffusion barrier property, but also of its liner properties, which are not discussed in previous chapters. In fact, none of the works using 2D layered materials for Cu interconnects have study the liner properties, which are essential to the technology integration. This chapter first introduces the low-temperature growth of TaS_x by our PECVD system. The material characterizations are also systematically conducted. Finally, electrical and other tests show the superior barrier and liner properties of this material. This work was carried out in collaboration with Prof. Moon Kim and Prof. Robert Wallace and their groups at the University of Texas at Dallas. It was also in collaboration with Dr. Kevin L. Lin, Dr. Carl H. Naylor, and Dr. Han Li at Intel Corporation.

In Chapter 5, vertical conduction of 2D layered materials is studied since it is directly related to "via resistance", which has become a bottleneck of interconnect performance. Due to the several advantages of TaS_x demonstrated in Chapter 4, the material is chosen for the analyses. We first confirm the existence of oxides on TaS_x and their serious impacts on vertical conduction. Then, we develop two approaches in the hope to avoid the oxides from being formed at the interface of metal and 2D barrier/liner. Finally, the intrinsic vertical conduction across high-quality TaS_2 is assessed, and a projection of its advantage in ultra-scaled interconnects is performed. This work was carried out partially in collaboration with Dr. Dimitry Zemlyanov at Purdue University.

Finally, Chapter 6 describes other possible applications that could benefit from 2D materials. One of them is the application in radio-frequency (RF) transmission lines. The reduction of the surface

scattering (hence the resistivity) at Cu/2D interface discussed in Chapter 4 could indicate the possibility of reducing the power loss in RF transmission lines. We show that TaS_x can lower RF power loss in transmission lines. The work was carried out in collaboration with Prof. Dana Weinstein and her group at Purdue University. In addition, TaS_x is further integrated with cobalt (Co) interconnects. The results show that Co diffusion is suppressed and Co resistivity is reduced with TaS_x being used as the barrier/liner. Finally, directions for future development is suggested.

2. TWO-DIMENSIONAL LAYERED MATERIALS BEYOND GRAPHENE AS CU DIFFUSION BARRIERS

2.1 Introduction

Although graphene has been demonstrated to have superior capability of blocking Cu diffusion despite its atomic thickness, in the meantime, a group of other two-dimensional (2D) layered materials exists, whose properties are complementary yet distinct from those of graphene. For instance, hexagonal boron nitride (h-BN) is an atomically thin 2D insulator (band gap ~6 eV) [7] and molybdenum disulfide (MoS_2) is a 2D semiconductor with a band gap ~2 eV [20] . Theoretical calculations predict high-energy barriers in some of these materials to prevent molecule diffusion [17], [18]. In the development of conventional diffusion barrier materials, various material types including both metals and insulators have been investigated, judged by the interface requirements of different applications [21], [22]. While it is still a rather unexplored field with many unknowns in these 2D materials such as Cu wetting and adhesion, interface scattering, and CMOS compatibility, it is important to evaluate the potential of these atomically thin 2D materials as ultra-thin barriers and make thorough comparisons.

In this chapter, we provide an overview on both theoretical and experimental studies of intrinsic diffusion barrier properties of various 2D materials. First principle density functional theory (DFT) calculations are employed to investigate barrier energies of various 2D materials for Cu diffusion. Although many of the candidates possess potential, we choose h-BN and MoS_2 for experimental analyses since high-quality, large-area, and continuous films of these two materials are available, which is not the case for many of the candidates. Their diffusion barrier properties are investigated by time-dependent dielectric breakdown (TDDB) measurements. We observe that the lifetime of intra- and inter-layer dielectrics can be significantly extended with the presence of the tested 2D

barriers. In addition, using scanning transmission electron microscopy (STEM), energy dispersive X-ray spectroscopy (EDS), and electron energy loss spectroscopy (EELS), we confirm that the examined ultra-thin 2D barriers can efficiently mitigate Cu diffusion and are promising alternative barrier solutions for interconnect technology. For the purpose of studying the fundamental/intrinsic properties, the materials chosen in the chapter are grown at high temperatures to achieve the highest possible quality. Practical considerations of the integrability to the technologies will be discussed in the following two chapters.

2.2 Simulation and Experimental Procedures

2.2.1 Density Functional Theory (DFT) Calculations

The geometry optimization minimum potential energy surfaces for Cu diffusion across TMDs were carried out using DFT as implemented in the Vienna ab-initio simulation package (VASP) [23], [24]. Projector-augmented-wave (PAW) potentials [25], [26] were used to account for the electron-ion interactions, and the electron exchange-correlation potential was calculated using the generalized gradient approximation (GGA) within the Perdew-Burke-Ernzerhof (PBE) [27] scheme using real-space projections. Since long-range dispersion interactions are not captured by the GGA functional, we employed Grimme's DFT-D3 energy correction scheme to account for these interactions [28]. In the DFT-D3 scheme, the Kohn-Sham DFT energy is corrected by adding a pairwise term that depends on the local environment of each atom. The kinetic energy cutoff for all calculations was set to 500 eV and, due to the relatively large simulation size, a gamma-centered $4 \times 4 \times 1$ mesh was used for the k-space sampling. A Gaussian smearing of 0.05 eV and an electronic relaxation tolerance of 1×10^{-5} eV was used for all calculations.

We used the climbing image nudged elastic band (NEB) method as implemented in VASP [29] to determine minimum potential energy surface and diffusion paths between known initial and final geometries with the Cu atom at local minima (on top of a metal atom for the 2H structures and opposite a chalcogen atom for the 1T structures) on either side of a 4×4 monolayer TMD with approximately 19-20 Å of vacuum between out-of-plane periodic images. The minima were obtained by structural relaxations using a conjugate gradient (CG) algorithm with a force tolerance of 0.01 eV/Å. The NEB calculations were initialized from a set of geometries interpolating

between initial and final structures; then, the ionic positions of the different geometries are iteratively optimized using only the ionic-force components perpendicular to the hypertangent. The energy along the diffusion path was determined by spline interpolation based on the total energy of the individual geometries.

The NEB structural relaxations were carried out using either the damped molecular dynamics or quasi-Newton algorithms. If the NEB forces could not be converged to 0.01 eV/Å under "normal" precision (the VASP input specification PREC = Normal), the precision was increased (PREC = Accurate). If convergence could still not be achieved, the density of the FFT grid was increased (ADDGRID = True). Only 2H-TaS_2 could not be converged to 0.01 eV/Å and was instead converged to 0.05 eV/Å.

2.2.2 Preparation of 2D Materials

Cu foils with h-BN grown on both sides by CVD at 1000 ℃ were first coated with polymethyl methacrylate (PMMA) on one side. The side with/without PMMA is identified as the top/bottom side throughout the descriptions. h-BN on the bottom side was completely etched away by Ar plasma. Then, the sample was placed in 1 M iron chloride ($FeCl_3$) solution, with the bottom side facing down, to etch away the exposed Cu. After Cu was completely etched, the sample was immersed in DI water for 10 minutes, followed by 1 M HCl solution for 10 minutes, and another 10 minutes in DI water. The PMMA/h-BN film was then picked up with a 20 nm SiO_2 on Si substrate and PMMA was finally dissolved by acetone. The STEM cross-section in Fig. 2.2(a) reveals there may be small thickness variations in our h-BN sample, ranging between 3-4 layers.
MoS_2 films were directly grown on 30 nm SiO_2 on Si substrates by CVD at 850 ℃. Details of the CVD growth can be found elsewhere [30]. 1L MoS_2 was identified by Raman spectroscopy, with characteristic E' peak at 384.5 cm^{-1} and A_1 at 405 cm^{-1}, respectively, as shown in Fig. 2.2(c). In addition, although 1L MoS_2 was dominant, characteristic Raman peaks associated with 2L MoS_2 were also found occasionally (~10% coverage). To transfer the MoS_2 film off the growth substrate, the sample was spin-coated with PMMA and immersed in DI water. A diamond scribe was used to create some scratches at the edges, which allows water to penetrate into the interface of the MoS_2 film and the substrate. The PMMA/MoS_2 was then detached from the substrate in DI water and transferred to the target substrate. Finally, PMMA was dissolved by acetone.

Both h-BN and MoS_2 samples have continuous film coverage with areas larger than 1 cm^2, such that large arrays of devices can be fabricated to perform statistical electrical measurements. We would like to emphasize that, the use of transfer method or high-temperature growth in this chapter is intended to study the fundamental diffusion barrier properties of large-area, high quality 2D layered materials, rather than providing a direct solution to interconnect technologies.

2.2.3 Fabrication of MOS Capacitor Structure

To perform electrical measurements, a metal-oxide-semiconductor (MOS) capacitor structure was fabricated, as depicted in Fig. 2.3. Devices with 2D barrier layers inserted between Cu and SiO_2 were evaluated for the diffusion barrier properties, while devices without any 2D barriers were prepared as control samples. Heavily-doped Si (resistivity < 5 mΩ-cm) substrates with 20 nm or 30 nm SiO_2 were used for the MOS capacitor sample fabrication. After transferring or growing a 2D film, Cu/Al (~30 nm/20 nm) electrodes with diameters of 100 μm were deposited using e-beam evaporation through a shadow mask, with Cu in contact with the 2D material and Al on top. The sample was then coated with photoresist and placed into 6:1 buffered oxide etch (BOE) to etch away the SiO_2 on the bottom side of the substrate, followed by 50 nm Al deposition to form an ohmic contact to the Si substrate bottom. Finally, the top photoresist was removed by acetone.

Three types of barrier samples were compared: i) One to two layer (1-2L) h-BN grown by chemical vapor deposition (CVD) on a Cu foil was transferred onto a 20 nm SiO_2/Si substrate twice to form a 3-4L h-BN barrier; ii) Single-layer (1L) MoS_2 with some small two-layer (2L) regions was directly grown on a 30 nm SiO_2/Si substrate by CVD [30] at 850 ^oC; iii) 1L MoS_2 from the same CVD growth was transferred to a 20 nm SiO_2/Si substrate for a direct process comparison that will be discussed. Note that, it will be shown possible in the next chapters to lower the growth temperature to be back-end-of-line (BEOL) compatible, which is not the focus of this chapter. This chapter aims to demonstrate the intrinsic barrier properties of various 2D materials by using high quality films from high temperature growth.

2.2.4 TEM/EDS/EELS Analysis

STEM cross-sectional samples were prepared with a FEI Nova 200 dual-beam FIB/SEM by using the lift-out method. The region of interest above the Al metal pad was protected during the focused

ion beam milling, by depositing SiO_2 and Pt layers on top of the sample. Both high resolution transmission electron microscopy (HREM) images, atomic STEM HAADF and bright field (BF) images were obtained in a JEOL ARM200F microscope equipped with a spherical aberration (Cs) corrector (CEOS GmbH, Heidelberg, Germany) and operated at 200 kV. The corrector was carefully tuned by the Zemlin-tableau method with Cs = 0.5 µm and the resolution was demonstrated to be around 1 Å. EDS was performed with an Aztec Energy Advanced Microanalysis System with X-MaxN 100N TLE Windowless 100 mm^2 analytical silicon drift detector. Line scan profiles were obtained by scanning the electron probe perpendicularly to the interface of interest. EELS was also performed by using a Gatan parallel electron energy loss spectrometer with better than 1 eV energy resolution.

2.3 Results of DFT Calculations

Although the 2D layered materials used for the experimental studies in this chapter have larger grain sizes, making diffusion through perfect crystal sites dominant, grain boundaries diffusion is also calculated here to provide general insight for many practical situations. Figures 2.1(a) and 2.1(b) show the lowest potential energy surfaces for Cu diffusing across various single-layer, perfect crystals of MX_2 TMDs with M=Mo, W, Ta and X=S, Se, Te. We show results for the two most stable phases 2H (space group P-6m2) and 1T (space group P-3m1). These calculations are performed on defect-free, perfect crystals that are hardly produced in real growth effort. In fact, most 2D materials in literature and those available in the market show rather high defect and impurity densities as well as limited grain sizes. Grain boundaries have been established as the dominant diffusion paths in the case of TaN/Ta [31]–[33], and they can certainly play important roles in the 2D materials of interest [34]. Nevertheless, exploring performance in ideal materials by calculations is essential for comparing intrinsic properties among different materials and identifying diffusion mechanisms. Our DFT results show that sulfides impose the highest barriers to diffusion with a reduction as we move to selenides and tellurides. In fact, quite surprisingly, Cu prefers interstitial sites over surface sites for 2H tellurides [35]. Due to the great interest in TaS_2 for reasons to be addressed in Chapter 4, the material will be discussed in further detail to fully evaluate its potential. Figures 2.1(a) and 2.1(b) show that 2H-TaS_2 is preferable over 1T-TaS_2 because of its higher energy barrier. In addition, 2H-TaS_2 is easier to be produced by low-temperature syntheses [36]. It is important to compare these new 2D materials with the

conventional TaN barrier that has been thoroughly studied both theoretically and experimentally. Although the comparison of calculated energy barriers for 2D materials and experimentally extracted values for TaN is rather crude, it is helpful to gain some initial insights in order to quickly identify promising candidates. Experimental barrier energy extraction of 3.27eV in single crystalline TaN by Wang et al. [31] and the calculated energies for 2D materials are included in the left panel of Fig. 2.1(c). Based on these comparisons, we conclude that graphene, h-BN and some sulfides can be as good as or even better than single crystallin TaN in terms of barrier energy and can be considered for Cu diffusion barrier applications. As mentioned earlier, materials used in practice are normally polycrystalline with grain boundaries. The right panel of Fig. 2.1(c) displays experimental extraction of reduced barrier energy range from 0.14-1.4 eV in TaN due to diffusion through grain boundaries [32], [37], [38]. The barrier energy for 1T-TaS_2 is calculated to be 1.5 eV [39], higher than that of TaN. It would be interesting to have the same to be calculated for 2H-TaS_2 as well. Surprisingly, the value for graphene obtained from the same work by Zhao et al. [34] reduced significantly. It is worth pointing out that even though 2D materials are not obviously superior than TaN in terms of grain boundary diffusion, it is theoretically possible to realize a single atomic layer of a 2D material with very large grain size. On the contrary, due to the 3D nature of TaN, achieving the same type of TaN film is not possible.

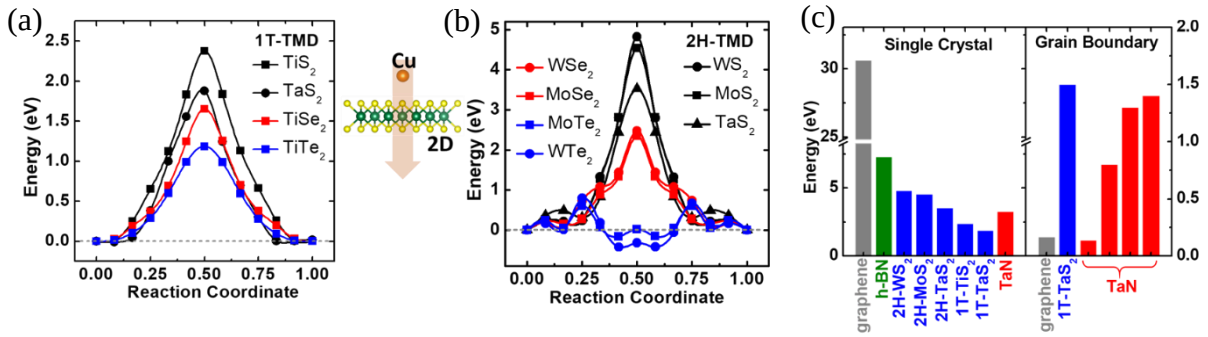


Fig. 2.1 (a) DFT-calculated barrier energy for Cu diffusion across various single-layer, perfect crystals of (a) 1T and (b) 2H TMDs. (c) Summary of barrier energies of various single crystal materials and materials with grain boundaries, both from this work (h-BN and materials in (a) and (b)) and literature (graphene, grain boundary diffusion of 1T-TaS_2, and TaN). It can be clearly observed that the energies for diffusion across single crystals are much higher than those across grain boundaries. Some 2D materials show comparable or superior performance than TaN.

2.4 TDDB Measurements and Lifetime Prediction

Although DFT calculations in the previous section provide prediction of the potential of various 2D materials as the diffusion barrier, experimental verification can only be conducted on large-area and continuous films, which is not available for many 2D materials yet. Therefore, in this section, we choose h-BN and MoS_2 for experimental analyses since films that meet the requirement are available. To rule out the variations generated by defects and grain boundaries in CVD-grown 2D films, or other imperfections from the not-yet-optimized CVD recipes, TDDB was adopted to evaluate the diffusion barrier properties of these 2D materials since it provides a statistical approach for a fair analysis. In addition, TDDB has been widely accepted as a test vehicle for assessment of Cu interconnect reliability [40]–[47]. Hundreds of devices (diameter=100 μm; spacing between two devices ~ 350 μm) were fabricated across large-area, continuous films for statistical assessments. In our TDDB setup, a positive constant electric field (E-field) was applied at room temperature to the top Cu electrode of the device-under-test, with the bottom p^{++} Si being grounded, as shown in Fig. 2.3. If the positive E-field drives Cu ions into SiO_2, these ions can accumulate and form a conductive path in the dielectric and/or assist in Poole-Frenkel tunneling [43], which leads to device breakdown. Time-to-breakdown (t_{BD}) of each device was recorded when the device broke down and the leakage current density reached 1.3×10^{-2} μA/μm^2 (equivalent to 100 μA from a circular metal pad with 100 μm diameter). Once t_{BD} of more than 10 devices (more than 15 in most cases) was obtained, an evaluation of the dielectric quality that takes the variability into account was finally achieved. If significant Cu diffusion is present, t_{BD} will be reduced due to Cu-induced breakdown, as illustrated in the left part of Fig. 2.3. If a 2D barrier can mitigate the Cu ion diffusion, t_{BD} is expected to be extended due to the lower probability of conduction path formation, which is depicted in the right part of Fig. 2.3. We would like to further emphasize that, the capacitor structure used here facilitates the study on intrinsic material properties [41], compared to the conventional inter-digitated electrode structures [43], [45], whose breakdown mechanisms are often affected by chemical-mechanical polishing (CMP) processes. Furthermore, the large area of the capacitor provides a fair imitation of real interconnects considering the large diffusion area due to the extended wire length.

Fig. 2.4(a) shows the current evolution with time for devices with and without h-BN under a stress of 7 MV/cm. We observe that devices without h-BN barriers reached breakdown earlier in general.

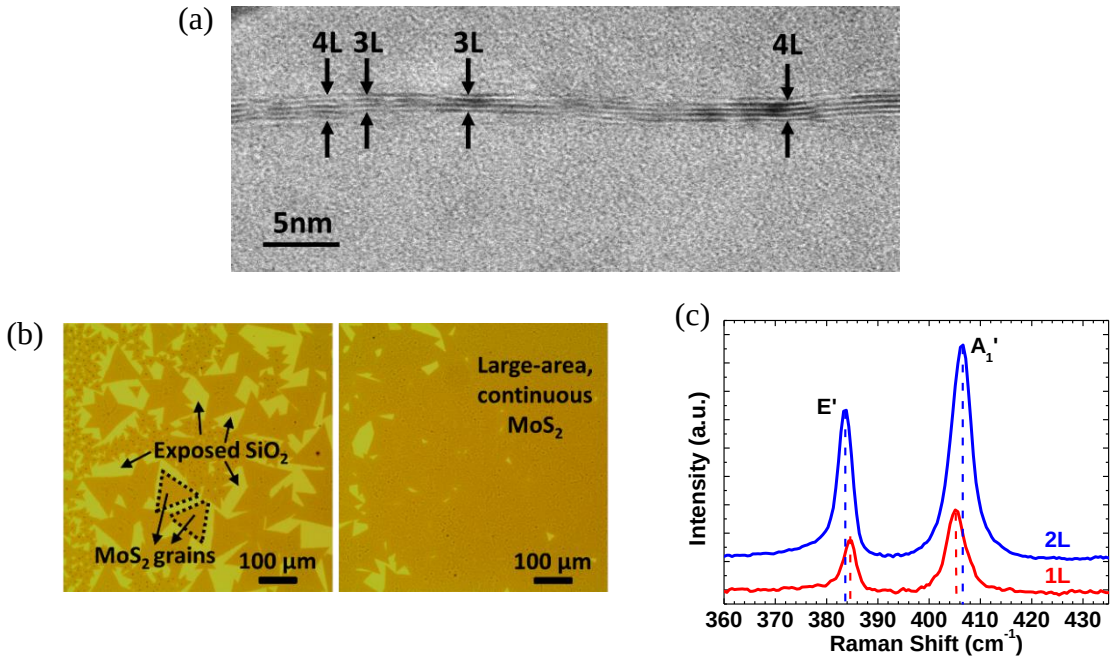


Fig. 2.2 (a) STEM cross-sectional image of transferred h-BN. (b) Optical images of directly-grown CVD MoS_2 films on SiO_2. Large MoS_2 grains are triangular shapes. The film consists of mostly 1L MoS_2 with some 2L regions. The empty areas are exposed SiO_2. (c) Raman spectra of MoS_2 on 30 nm SiO_2 on Si substrate. Characteristic peaks of 1L and 2L MoS_2 can both be identified, with 1L being dominant. The wavelength of the laser used for Raman measurements was 532 nm. All measurements on both h-BN and MoS_2 were conducted in regions with large-area (> 1 cm^2), continuous film coverage.

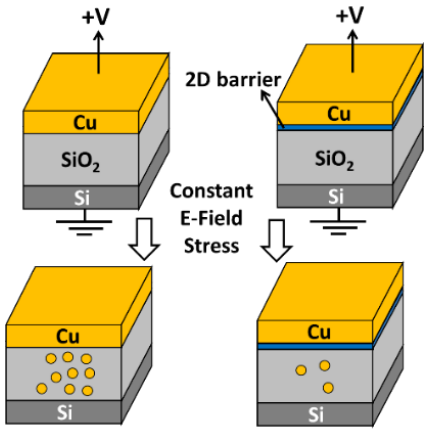


Fig. 2.3 MOS capacitors used for barrier property evaluation. Cu diffusion into SiO_2 with and without 2D barriers in place under constant-electric-field stress is illustrated. Note that an Al layer (not shown) was deposited both above Cu and beneath Si.

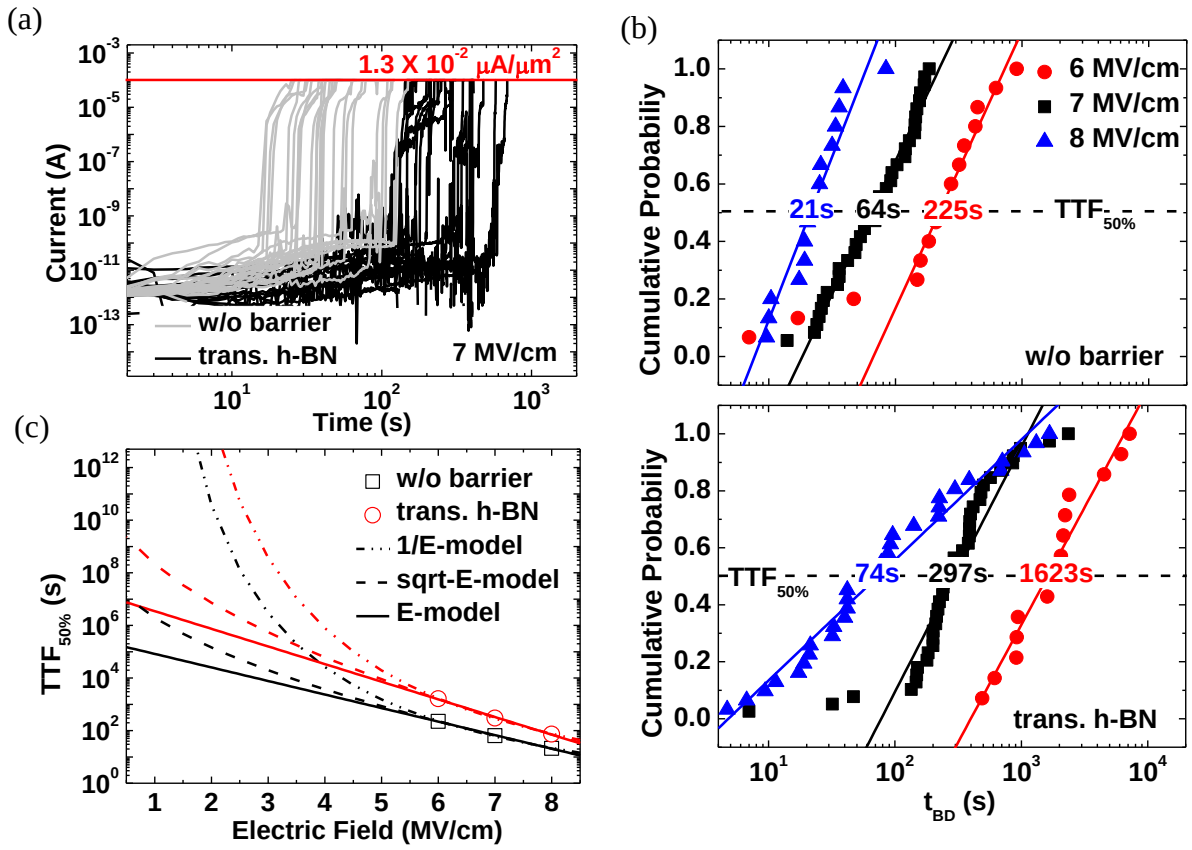


Fig. 2.4 (a) Current evolution with time for multiple devices with and without h-BN under the stress condition of 7 MV/cm. Devices without barriers break down earlier in general. (b) TDDB results at various E-fields for devices with and without the h-BN barrier. Time-to-breakdown (t_{BD}) of the h-BN devices is significantly increased. (c) Lifetime predictions based on three analytical models. With the presence of h-BN, device lifetime at low fields can be enhanced from 10^5 s to 7.5×10^6 s, based on the E-model.

Moreover, before the breakdown occurred, the currents of the devices without h-BN were generally higher. Defining the breakdown current at 1.3×10^{-2} μA/μm^2, t_{BD} of different devices can be obtained from Fig. 2.4(a). TDDB results of devices with and without h-BN at various E-fields of 6, 7, and 8 MV/cm are compared in Fig. 2.4(b). Each data point represents t_{BD} of a single device. At a certain E-field, the device with the shortest/longest t_{BD} was assigned to have the lowest/highest value of the cumulative probability. Therefore, the slope of the fitted line for any given E-field is always positive. With the presence of the h-BN barrier, t_{BD} of devices has clearly increased, indicating the suppression of Cu diffusion. The less-steep slope of the 8 MV/cm line of the h-BN devices is attributed to device variations, which occasionally is inevitable for transferred-CVD films. Despite this, the median-time-to-failure ($TTF_{50\%}$) defined at probability of 0.5 is still a fair indication of the average device reliability since it was statistically obtained from a large number of devices. The purpose of performing TDDB measurements at various E-fields is to allow extrapolation of the device lifetime under normal operating conditions (much lower E-fields) by fitting with some analytic models [40]–[44]. Otherwise, directly conducting TDDB at low E-fields can be extremely time consuming. Among numerous proposed models, E-model [40], 1/E-model [41], [42], and sqrt-E-model [43], [44] are chosen for low field lifetime predictions, as shown in Fig. 2.4(c). The equations of these models with only the E-field dependent terms shown can be expressed as:

E-model: $\ln(TTF_{50\%}) \sim -\gamma E$ (2.1)

1/E-model: $\ln(TTF_{50\%}) \sim (G/E)$ (2.2)

sqrt-E-model: $\ln(TTF_{50\%}) \sim -2\beta_S\sqrt{E}$ (2.3)

where γ, G, and β_S are regarded as constants in this study. While various models emphasizing different breakdown mechanisms have been investigated extensively for decades, it is well understood that they can vary significantly with different materials, processes, and structures. Since detailed breakdown mechanisms are not yet explored in these diffusion barrier materials, a lot more research is required to develop sufficient understanding and build models that can eventually provide precise predictions in the future. The models adopted in this study include the most conservative one (E-model) and a relatively optimistic one (1/E-model), based on which qualitative comparisons without detailed mechanism analyses have been accomplished. Our

results demonstrate a general enhancement of dielectric lifetime regardless of the model used. In Fig. 2.4(c), under the normal operating condition, devices with h-BN have ~50 times longer lifetime (from ~10^5 to 7.5 × 10^6 s) than devices without barriers, based on the prediction of the E-model.

We now turn to the MoS_2 barriers. Field dependent TDDB measurement results are plotted in Figs. 2.5(a)-(c). Based on $TTF_{50\%}$ of the directly-grown MoS_2 (Fig. 2.5(b)) devices and the control samples (Fig. 2.5(a)) at different E-fields, comparison of the lifetime prediction is provided in Fig. 2.5(d). We observe that, with the presence of the MoS_2 barrier, the reliability of the dielectric underneath Cu under normal operating conditions is significantly enhanced, from ~10^5 to 3.7 × 10^8 s, showing more than three orders of magnitude improvement in device lifetime. It is worth noting that, despite the longer $TTF_{50\%}$ of the devices with transferred h-BN at high E-fields, the predicted lifetime of the devices with directly-grown MoS_2 is superior at low E-fields. This discrepancy can be attributed to SiO_2 quality degradation due to thermal stress during the CVD growth, which is confirmed in Fig. 2.5(e). The sulfur-thermal annealed SiO_2/Si sample (labeled as "after 850 ^oC growth") went through the same CVD process but intentionally received no MoS_2 growth. During the CVD growth, the high-temperature facilitated decomposition of SiO_2 and/or thermal stress-induced diffusion of precursor residues into SiO_2 can generate defects in the dielectric [48]–[50]. As a result, the sulfur-thermal annealed SiO_2/Si sample has lower t_{BD} and higher leakage current before the breakdown. This can be minimized once the growth recipe is optimized. It is acknowledged that low temperature growth processes need to be developed to meet the BEOL requirements and prevent thermal damage to the dielectrics. Interestingly, at low E-fields, the extrapolated lifetime of both SiO_2/Si control substrates are very similar, as shown by the black curves in Fig. 2.4(c) vs. Fig. 2.5(d). This suggests that the aforementioned CVD-induced SiO_2 defects do not contribute much to the reduction of $TTF_{50\%}$ at low E-fields. In contrast, $TTF_{50\%}$ degrades more at high E-fields when the energy barrier for Cu ions to overcome to transport through these defect states is lowered by the E-fields. Therefore, at low E-fields, the lifetime of devices with the transferred h-BN and directly-grown MoS_2 can still be compared even though they have gone through different processes. To further verify the proposed mechanism, MoS_2 is removed from its original growth substrate and transferred onto the same 20 nm SiO_2/Si substrate used for the h-BN samples. As shown in Fig. 2.5(c), $TTF_{50\%}$ at high E-fields is higher than that of

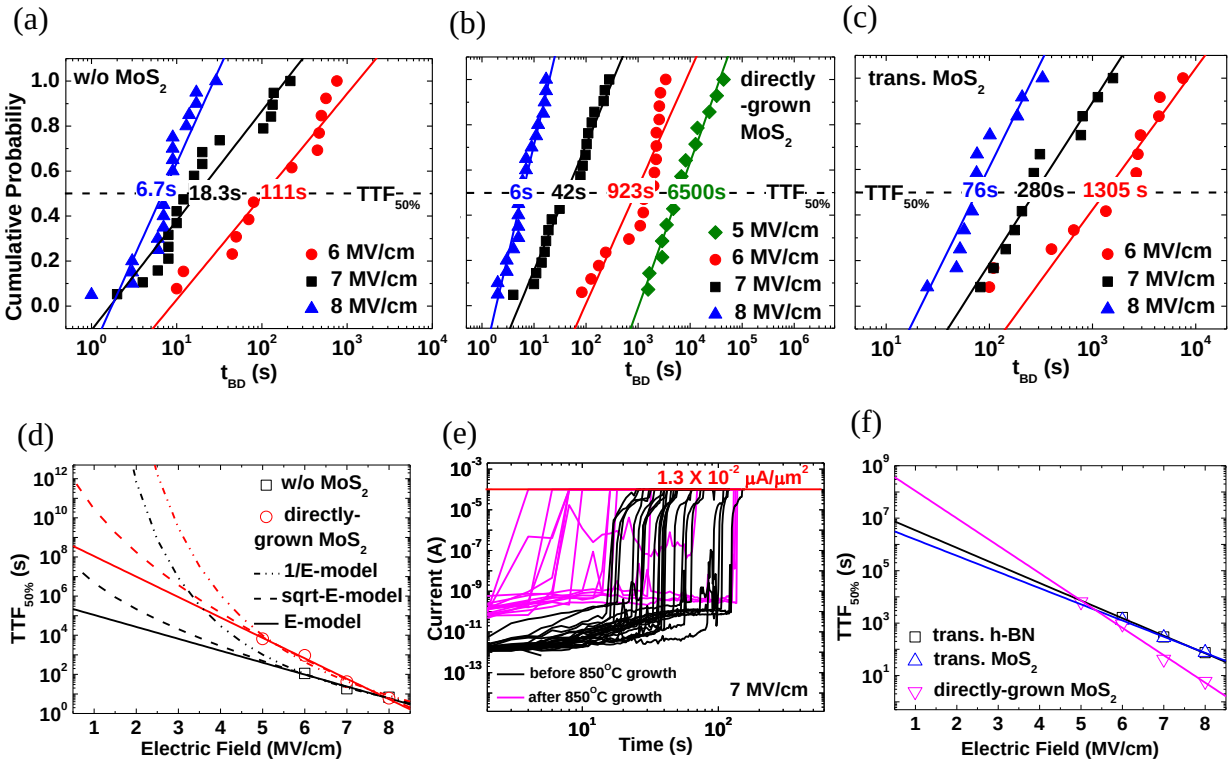


Fig. 2.5 (a)(b)(c) TDDB results at various E-fields of devices (a) without MoS_2, (b) with directly-grown MoS_2, and (c) with transferred MoS_2 as the diffusion barrier. (d) Lifetime prediction of directly-grown MoS_2, compared to that of the control sample using various models. With the presence of MoS_2, device lifetime can be enhanced from 10^5 s to 3.7×10^8 s, based on the E-model. (e) Current evolution with time of multiple devices before and after the thermal stress from the CVD growth. The sulfur-thermal annealed devices (labeled as "after 850 °C growth") went through the same CVD process but intentionally received no MoS_2 growth. These devices had higher leakage currents and shorter breakdown time. (f) Comparison of the predicted lifetime for devices with different 2D barriers and from different preparation processes, based on the E-model. Directly-grown MoS_2 performs the best as a diffusion barrier.

the directly-grown MoS_2 and rather close to the h-BN samples shown in Fig. 2.4(b), which can be attributed to the superior SiO_2 quality. However, when extrapolated to the normal operating conditions, the transferred MoS_2 sample shows worse performance than the directly-grown MoS_2, as discussed in next paragraph.

The comparison of the device lifetime with different materials and from different processes is shown in Fig. 2.5(f). With the presence of transferred h-BN, transferred MoS_2, and directly-grown MoS_2, the device lifetime at low E-fields can be enhanced from ~10^5 s (without barrier) to 7.5 × 10^6 s, 3.1 × 10^6, and 3.7 × 10^8 s, respectively, based on the most conservative expectation from the E-model. The summary of the material information and the lifetime improvement is listed in Table 2.1. Since the grain size of the h-BN and MoS_2 films used in this work is rather similar (~micrometer), we conclude that grain boundary density is not the dominant factor in device lifetime. In fact, we conclude that directly-grown MoS_2 gives the best performance in mitigating Cu ion diffusion. Interestingly, devices with transferred h-BN and transferred MoS_2 show similar E-field dependent behaviors, indicating the lifetime of these devices is limited by the film transfer process instead of individual material properties. Defects, cracks and impurities introduced by the mechanical transfer process limit the barrier quality to a large extent. Although optimization of the transfer methods can certainly bring improvement [51], it will remain challenging to realize large-scale transfer of 2D barrier materials with consistent reliability in VLSI technology. We therefore conclude that, directly-grown 2D materials are highly preferred to improve the reliability and device lifetime.

While this chapter focuses on testing diffusion barrier properties of 2D materials, we acknowledge there might be additional advantages and functionalities these materials can bring to the interconnect technology, which will require further investigations. For example, it has been shown that single layer MoS_2 with a body thickness of ~0.7 nm can be rather conductive despite its semiconductor nature [11]. The conventional diffusion barrier, TaNx, generally has a bulk resistivity of a few hundred μΩ-cm. When being scaled down to 2-3nm, the deposited TaNx layer becomes TaONx in most areas where it is in direct contact with the interlayer dielectric, resulting in a largely increased resistivity (~few thousand μΩ-cm). In some circumstances where conductive diffusion barriers are requested (e.g. shunting the current through tiny voids in Cu formed in the

Table 2.1 Material information and lifetime improvement in samples with different barriers.

Material	Layer number	Thickness	Lifetime improvement at 0.5 MV/cm (E-model)
Transferred h-BN	3 - 4	~1 – 1.3 nm	~50×
Transferred MoS_2	1 - 2	~0.6 – 1.3 nm	~20×
Directly-grown MoS_2	1 - 2	~0.6 – 1.3 nm	~1000×

early stage of electromigration) [52], MoS_2 can actually outperform ultra-scaled conventional barriers. In addition, phase engineering [53] can also convert semiconducting 2H-phase MoS_2 into metallic 1T-phase MoS_2 to carry out a high conductivity.

Another major concern is that electromigration lifetime generally decreases for every interconnect generation. When interconnect dimensions continue to scale down, the interfacial mass transport becomes the dominant factor responsible for the reduction of the lifetime. In a standard damascene structure, the bottom and sides of the Cu line are covered by the diffusion barrier/liner layer where the bonding strength is rather strong, while the top surface is covered by a capping layer to strengthen the bonding at the interface. While graphene has been recently demonstrated to improve Cu electromigration lifetime [54], the bonding strength between Cu and 2D materials has not been widely studied yet. Thorough studies should be carried out on MoS_2 and h-BN to examine their impacts on electromigration lifetime in addition to their diffusion barrier properties.

2.5 STEM/EDS/EELS Analysis

Besides electrical measurements, STEM in conjunction with EDS and EELS were used for structural analysis and compositional/chemical mapping of the interface and inter-diffusion processes. Devices without a barrier, with transferred h-BN barrier, and with directly- grown MoS_2 were analyzed. Each device had an Al cap on top to prevent Cu oxidation and was electrically stressed at 6 MV/cm for 250 s. Under this stress condition, only the control device without a barrier broke down, whereas devices with 2D barriers maintained their initial current values and no breakdown was observed. Fig. 2.6(a) shows the HAADF (high-angle annular dark-field) STEM cross-sectional image of the MoS_2 sample. As the heaviest element, Cu gives the brightest contrast while SiO_2/Si and Al appear relatively darker, as expected. Between Al and Cu, there appears to

be a uniform layer with a light contrast. EDS suggests that this layer was formed by intermixing of Al with diffused Cu. In both STEM image and EDS line scans, the Cu/SiO_2 interface appears sharp with a MoS_2 layer clearly detected in between, and Cu diffusion into SiO_2 is greatly suppressed.

In the device with the transferred h-BN barrier, the Al and Cu regions were hardly distinguishable, as observed from both the STEM and EDS line scan profile in Fig. 2.6(b). This strong inter-diffusion of Al and Cu could be a result of poor Cu adhesion on h-BN. At the Cu/SiO_2 interface, a very weak N signal (not shown) can be identified for the h-BN layers, while the B signal is too small to be detected in EDS. To further verify the existence and position of the h-BN layer, EELS was conducted given its superior resolution for lighter elements. As shown in Fig. 2.6(c), B and N signals were detected between the Cu and SiO_2 layer. Similar to the MoS_2 sample, Cu diffusion into SiO_2 is prevented.

In contrast, the MOS capacitor structure of the control device without any barrier was severely altered by the electrical stress, with Figs. 2.6(d) and 2.6(e) as two examples. In Fig. 2.6(d), a ball-like feature displaying strong Cu signals was formed. In Fig. 2.6(e), a large amount of Cu diffused through SiO_2 and reached the Si substrate. This phenomenon has been observed and identified as copper silicide formation by others [12]–[14], where Cu ions reacted with Si after the diffusion. Note that the devices in previous reports were thermally stressed; while electrical field stress was used in this work, with all measurements at room temperature. This can explain why crystalline copper silicide was not clearly observed here, possibly due to the lack of thermal energy.

Comparing the TEM cross-sections in Figs. 2.6(a) and 2.6(b), we conclude that Cu started to diffuse into SiO_2 in the transferred h-BN device even though no breakdown was measured and the device structure was not changed; whereas no such diffusion was observed at all in the device with directly-grown MoS_2 barrier. Similar results were observed in STEM cross-sections of six other positions (three for h-BN and three for MoS_2). Therefore, we conclude that directly-grownMoS_2 performs better as a diffusion barrier, which is consistent with the TDDB results.

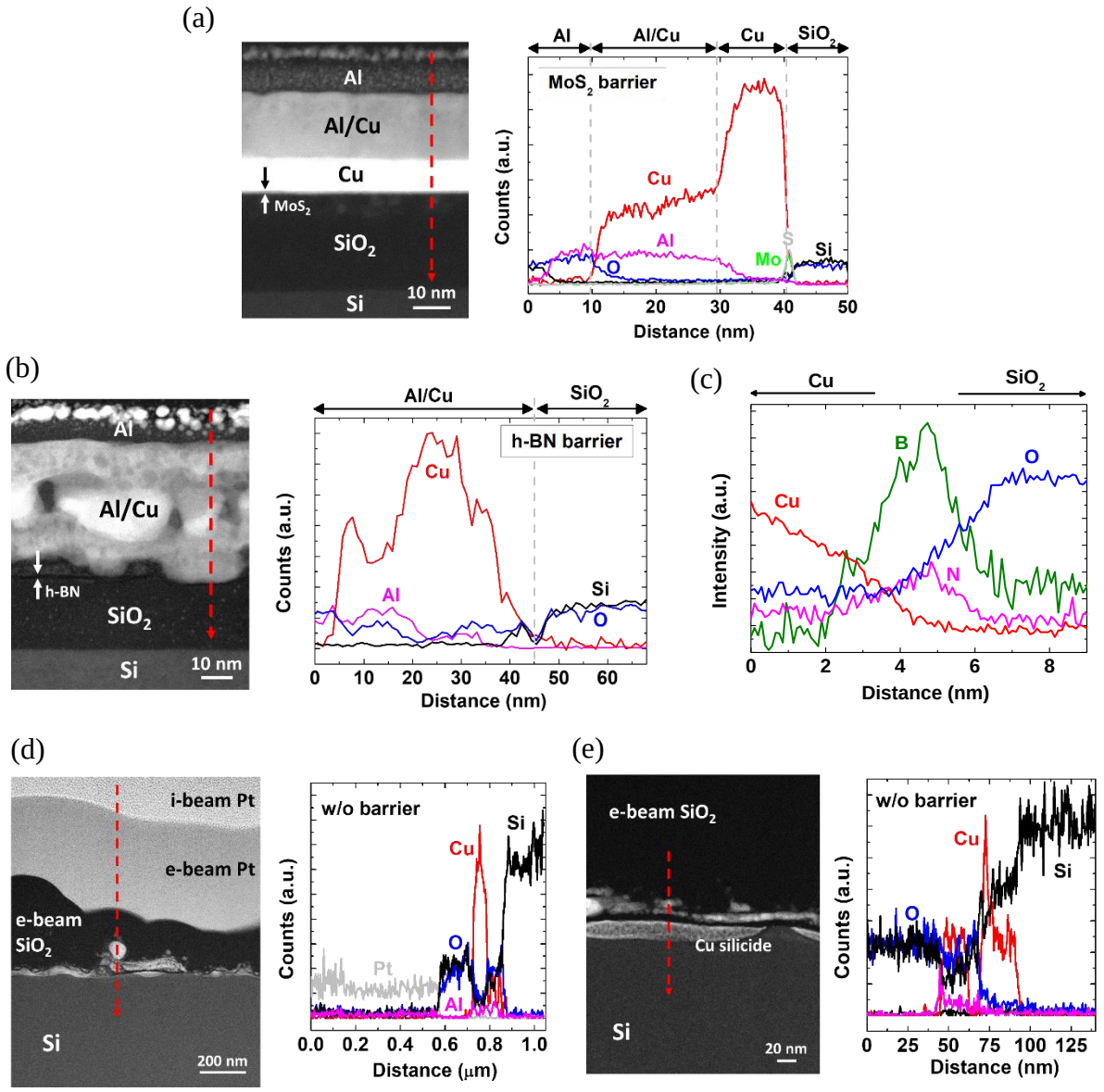


Fig. 2.6 Structural, compositional, and chemical analyses. STEM cross-sections and EDS line scan profiles of devices (a) with directly-grown MoS_2, (b) with transferred h-BN, and (d)(e) without any barriers. The structures of control devices without barriers were completely damaged after the electrical stress (6 MV/cm; 250 s). The device with either h-BN or MoS_2 barrier remained unaltered and Cu signals were barely found in the SiO_2 region. (c) EELS line scan profile of the device with h-BN barrier. B and N signals can be detected in-between Cu and SiO_2 layers. Cu diffusion into SiO_2 was suppressed by h-BN barrier.

2.6 Conclusion

In this chapter, the barrier energies for Cu diffusion of multiple 2D materials are predicted using DFT calculations, with the results showing potential of many 2D materials. Experimentally, the diffusion barrier properties of two types of 2D materials, h-BN and MoS_2 have been evaluated using TDDB measurements and with STEM, EDS, and EELS analysis. Predictions of substantial device lifetime improvement are made by analytical models based on experimentally measured times-to-breakdown. The work in this chapter provides strong evidence that these atomically thin 2D materials are capable of suppressing Cu diffusion into surrounding dielectrics, identifying them as potential sub-nanometer thin barrier solutions for interconnect technology. We further conclude that direct growth of 2D barriers on dielectric substrates is favored over that of transferred 2D barriers, at least with the present state of the art in both processes. Future studies must focus on a more detailed understanding of the diffusion and breakdown mechanisms through 2D materials, and an optimization of the 2D material deposition to be BEOL compatible.

3. DEVELOPMENT AND EVALUATIONS OF BACK-END-OF-LINE COMPATIBLE TWO-DIMENSIONAL DIFFUSION BARRIERS

3.1 Introduction

In the previous chapter, we have shown the promising diffusion barrier properties of 2D layered materials, h-BN and MoS_2 specifically. Together with other graphene barrier works, it is convincing that 2D layered materials are great candidates of diffusion barrier alternatives. However, despite the abovementioned benefits of 2D layered materials, a BEOL compatible growth process that can directly deposit ultrathin 2D barriers on dielectrics has not yet been realized. The obstacle lies in the requirement of high temperature and the substrate dependent growth [55], [56]. Diffusion barriers need to be directly deposited on the dielectrics of the Damascene Structures. However, for some materials, such as graphene, growth on dielectrics is more challenging than on Cu [16], [54], especially at low temperatures. An approach of growing 2D materials on catalytic substrates followed by a transfer process to substrate of interest is usually adopted for planar structures [13], [57], which often introduces defects to the barrier material and raises concerns of conformal coverage for Damascene structures. Table 2.1 summarizes works using 2D material as diffusion barriers. It is obviously that each method has its own issue for the BEOL integration. In this chapter, a single-layer (1L) MoS_2 (~0.62 nm) directly grown on dielectrics at 400 ℃ is achieved by metal-organic chemical vapor deposition (MOCVD). We will show that these barriers can effectively prevent Cu diffusion and enhance the dielectric reliability. In addition, diffusion barrier property of this BEOL-compatible MoS_2 and that of the high-temperature-grown MoS_2 in the previous chapter will be compared.

Table 3.1 Comparison of different works using 2D layered materials as Cu diffusion barriers

Material	**Thickness**	**Growth Temperature**	**Accomplishment**	**Method**
Graphene [16]	1 nm	650 ℃	Reduce surface scattering/resistivity	Grown on Cu
Graphene [54]	> 10nm (1-2 layers of Gr + 10 nm a-carbon)	400 ℃	Improve electromigration lifetime	Grown on Cu
MoS_2 (Chap. 2)	< 1 nm	850 ℃	Mitigate Cu diffusion	Direct-grown on SiO_2
Graphene [57]	< 1 nm	1000 ℃	Mitigate Cu diffusion	Transfer from Cu foil
Graphene/graphene oxide [14]	< 1 nm / ~ 1 nm	750 ℃	Mitigate Cu diffusion	Transfer from Cu substrate
Graphene [12][13]	< 1 nm	High temperature	Mitigate Cu diffusion	Transfer from Cu sheet /substrate

3.2 Material Preparation and Characterizations

The material preparation was carried out by Dr. Kehao Zhang at Prof. Joshua Robinson's group at Pennsylvania State University. Large-area (> 1 cm^2), uniform MoS_2 films were grown by MOCVD in a hot-zone reactor, as illustrated in Fig. 3.1(a). Molybdenum hexacarbonyl ($Mo(CO)_6$) (Sigma, > 99.9%) and diethyl sulfide (DES) (Sigma, 98%) were used as the precursors for Mo and S, respectively. The growth was set at 400 ℃ for 60 minutes. During the growth, $Mo(CO)_6$ was kept at 24 ℃ with 2 sccm of H_2 as the carrier gas; meanwhile, the DES was kept at 22 ℃ with 45 sccm of H_2 as the carrier gas. In the main chamber, 565 sccm of Ar was continuously flowing as the carrier gas. Raman spectrum with 488 nm laser wavelength in Fig. 3.1(b) reveals the characteristic peaks, namely $E_{2g}{}^1$ and A_{1g}, of MoS_2, suggesting the formation of the material. The thickness of MoS_2 was measured to be sub-nm by atomic-force microscope (AFM) line scan, shown in the top panel Fig. 3.1(c). The bottom panel of Fig. 3.1(c) indicates that the MoS_2 film is nanocrystalline with a grain size around tens of nanometers. The impact of the crystal structure on diffusion barrier property will be discussed in this chapter.

3.3 Diffusion Barrier Property Tests

The testing methodology is briefly described in this section. Details of the preparation and the structure of the device, as well as the measurement setups can be found in Chapter 2. Capacitor structures illustrated in Fig. 3.2(a) were used for time-dependent dielectric breakdown (TDDB) measurements [41], [43], [45], [47], [58]–[60] conducted at room temperature since it is well accepted that capacitor structures provide the information of the intrinsic dielectric reliability [41], [45], [58], [59]. In TDDB measurements, a constant electric field is applied across the capacitor structure to drive Cu ions into SiO_2, which can cause Cu-induced breakdown. If the 1L MoS_2 barrier is able to mitigate the Cu diffusion, time-to-breakdown (t_{BD}) of device with the barrier is expected to be enhanced since fewer the Cu ions would be present in SiO_2, as depicted in Fig. 3.2(a). Current evolution at a constant electric field stress of 5 MV/cm is shown in Fig. 3.2(b). Each line represents the breakdown behavior of a device. When breakdown occurs, the device current reaches the compliance, which was set to be 100 μA, equal to1.3×10^{-2} $\mu A/\mu m^2$ based on the capacitor area. In general, devices with MoS_2 barriers break down later than those without any

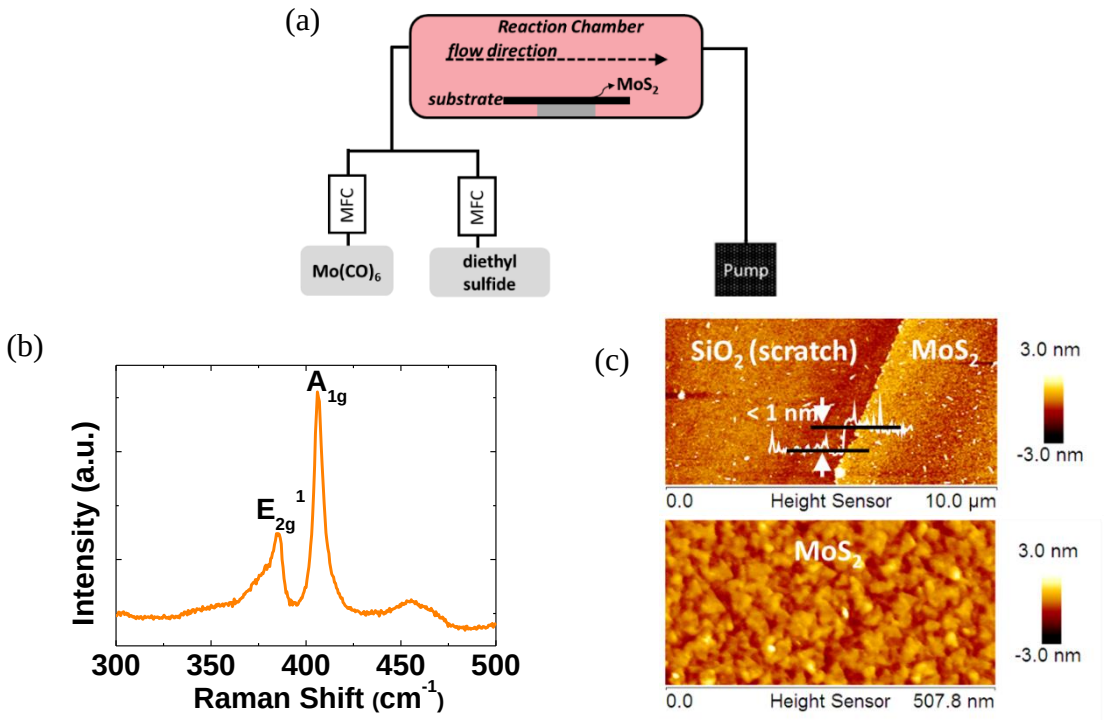


Fig. 3.1 (a) Schematic of the MOCVD system for MoS_2 grown at 400 °C. (b) Raman spectrum of 400 °C MoS_2 grown on 90 nm SiO_2. The laser wavelength used is 488 nm. Characteristic peaks of MoS_2 are revealed. (c) AFM images and line scan profile of the MoS_2 film. The thickness is below 1 nm. The grain size is around tens of nanometers.

barrier. Note that some of the devices with MoS_2 have higher leakage currents before breakdown. This is attributed to the conductance through MoS_2 [61] surrounding the capacitors with high voltages applied. Nevertheless, a general trend of increase in t_{BD} is observed. TDDB measurements at various electric fields were also conducted and the values of t_{BD} of multiple devices were recorded and represented in the cumulative distribution plot shown in Fig. 3.2(c). With the MoS_2 barrier, the trend of increase in t_{BD} is obvious regardless of the electric field applied. The increase in medium-time-to-failure ($TTF_{50\%}$) is also revealed in Fig. 3.2(c). The low-temperature growth is

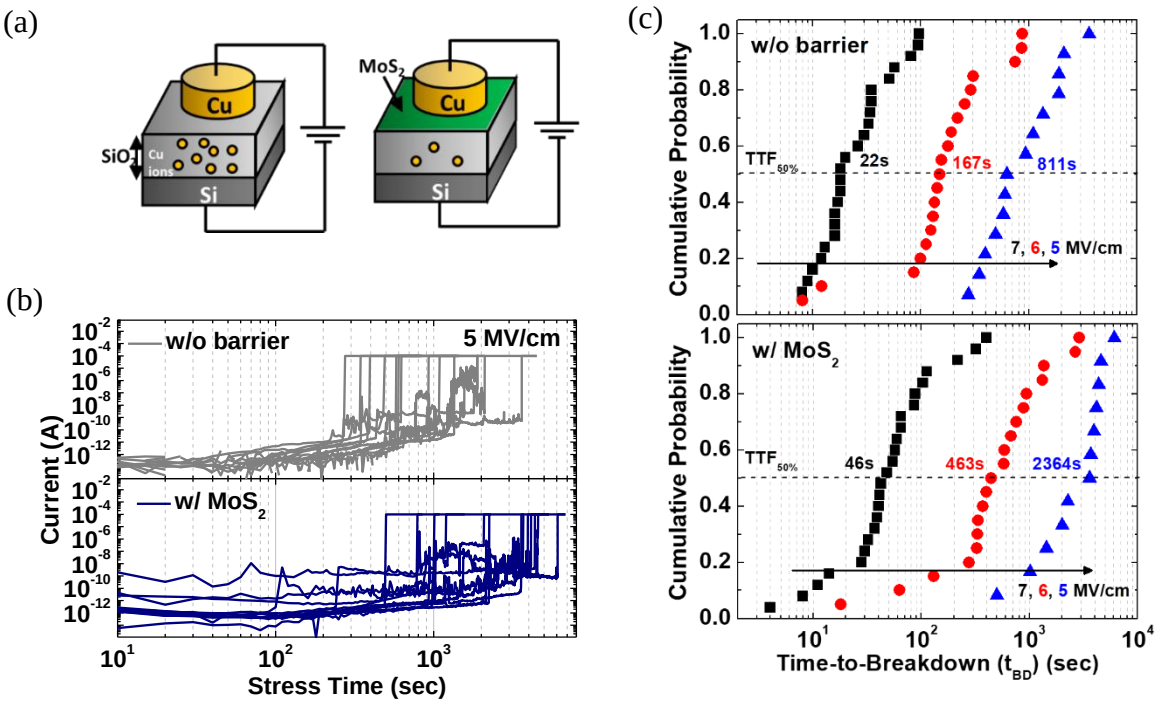


Fig. 3.2 (a) Capacitor structures used for TDDB measurements to evaluate Cu diffusion. If MoS_2 barrier can mitigate Cu ion diffusion, time-to-breakdown (t_{BD}) will increase due to the suppression of Cu induced breakdown (b) Current evolution with stress time of devices with and without a barrier at 5MV/cm. (c) Cumulative distribution of t_{BD} under various electric field stress for devices with and without MoS_2 barrier. From (b) and (c), it is observed that t_{BD} increases in general with the presence of MoS_2 barrier.

advantageous in reducing the damage to SiO_2, as observed by comparing the top panel of Fig. 3.2(c) with Fig. 2.5(a) (SiO_2 after 850 ℃ treatment). However, the grain size of low-temperature grown MoS_2 is smaller compared to that from the high-temperature growth, resulting in an inferior Cu blocking capability. Efforts must be made to enlarge the grain size to further mitigate Cu diffusion. Detailed discussions on the effects of growth temperature and grain sizes will be included in the next section.

In addition to using SiO_2 as the dielectric for the test, the industrial standard low-*k* dielectrics (*k*=2.55; 150 nm) was also adopted for the evaluation. To reduce the total *RC* (resistance-capacitance) delay, dielectrics with lower (compared to SiO_2) relative permittivity (*k* value) have been incorporated as the dielectric in-between two interconnects to reduce the capacitance. The same growth condition was used to deposit MoS_2 on low-*k* substrates. Since low-*k* dielectrics have weaker dielectric strength, the tests were done at a much lower electric field. Figure 3.3(a) shows the current evolution of devices with and without MoS_2 at a stress field of 2.5 MV/cm. Devices with MoS_2 barrier break down later, as in the case of SiO_2. The general improvement with MoS_2 can also be observed in distribution in Fig. 3.3(b).

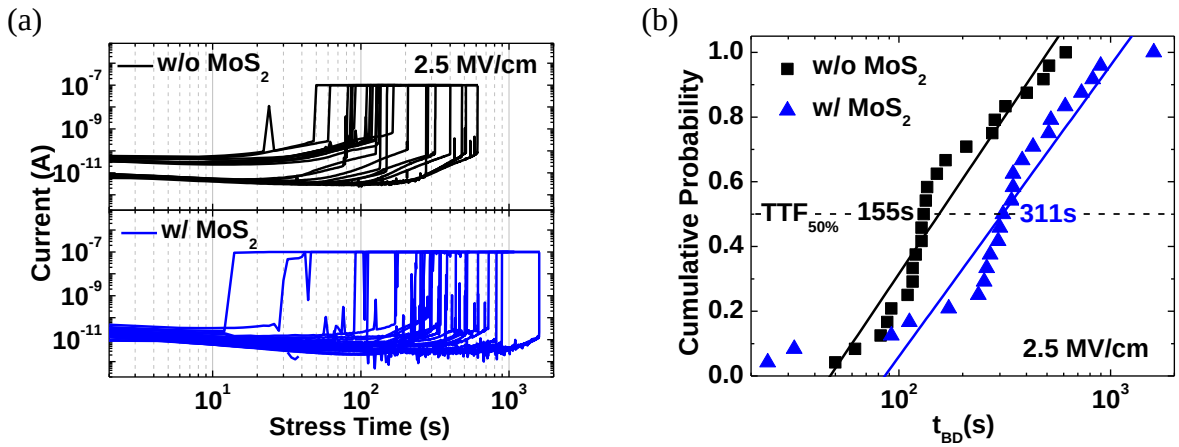


Fig. 3.3 (a) Current evolution with stress time of devices with and without a barrier at 2.5MV/cm on low-*k* dielectrics. (b) Cumulative distribution of t_{BD} under 2.5 MV/cm stress for devices with and without MoS_2 barrier on low-*k* dielectrics.

3.4 Comparison of MoS_2 Grown at Different Temperatures

We have shown the diffusion barrier properties of MoS_2 grown at higher temperature in Chapter 2 and at lower temperature in this chapter. Now we will make the comparison in this section. Time-to-breakdown (t_{BD}) values obtained from multiple devices on MoS_2 films prepared at different temperatures and by different methods are plotted in Fig. 3.4. The importance of lower growth temperatures, as mentioned in Chapter 2, can be observed by comparing the green and the red boxes. The green box represents the statistics of t_{BD} from devices with directly-deposited MoS_2 barriers at 850 ℃. When the same MoS_2 is transferred to a substrate that has not gone through the high temperature process, t_{BD} of devices increases obviously, as shown in the red box. Since the qualities of two MoS_2 films should be nearly identical, the enhanced t_{BD} indicates a better qualify of the latter dielectric, as a more defective dielectric will facilitate more Cu diffusion.

Although BEOL-compatible synthesis can be realized by the abovementioned MOCVD approaches, growth at lower temperatures normally results in films with smaller grain sizes, as observed in Fig. 3.1(c). Since grain boundaries are the main diffusion paths for Cu, barriers with smaller grain sizes will have inferior performance. On the other hand, with high-temperature CVD growth, the grain size is normally on the order of a few to tens of micrometers, as shown in Fig. 2.2(b). The compromised diffusion barrier property of low-temperature MoS_2 barrier can be noticed by comparing the red and the blue boxes. Since the dielectric is hardly damaged by the low-temperature growth, the degraded performance is attributed to the smaller grain sizes or more grain boundaries, which facilitate more Cu diffusion.

Even with the current bottleneck of low-temperature growth, the grain size of the BEOL-compatible MoS_2 is still comparable to those of sputtered TaN and Ta, whose grain sizes are also in the range of tens of nanometers [32]. In fact, the columnar structure in TaN/Ta [32], [62], [63] can possibly make grain boundary diffusion more severe than in 2D materials. In addition, although the grain size is limited by current CVD techniques, achieving single-layer 2D materials with large grain size is fundamentally possible due to the material nature. This should be one of the future research focuses in this area. On the other hand, TaN/Ta would become discontinuous at the same atomic thickness due to their 3D natures.

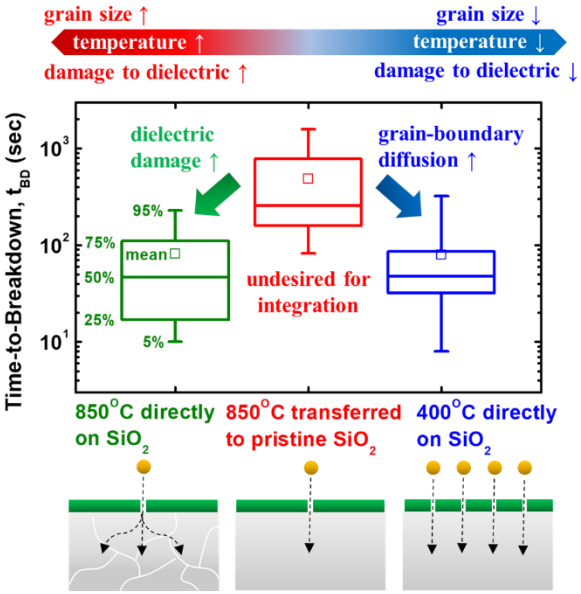


Fig. 3.4 Comparison of diffusion barrier properties of 2D materials grown at different temperatures, with MoS_2 as the example. Green box represents t_{BD} of multiple devices with directly deposited MoS_2 at 850 °C, while red box is from t_{BD} values of devices with the same MoS_2 but transferred onto a pristine SiO_2. Although high-temperature synthesis leads to a better film quality, the dielectric would be severely damaged, as can be observed by comparing the green and red boxes. Blue box represents t_{BD} values of devices with a 400 °C-grown MoS_2. The inferior barrier property of low-temperature-synthesized barrier can be noticed by comparing the red and blue boxes, which is attributed to the smaller grain size.

3.5 Conclusion

In this chapter, we demonstrate the possibility of realizing a BEOL-compatible, sub-nm MoS_2 diffusion barrier directly deposited on dielectrics, which has not been realized in other work using 2D layered materials as Cu diffusion barriers. The assessment is based on the material's immunity to Cu diffusion using TDDB measurements. The suppression of Cu diffusion with 2D barriers is demonstrated on both SiO_2 and low-*k* dielectric substrates. Furthermore, we have compared the BEOL-compatible MoS_2 with the high-quality MoS_2 grown at higher temperature. To further improve diffusion barrier property, low-temperature growth that can deliver large-grain-size-2D barriers is required.

4. TWO-DIMENSIONAL TANTALUM SULFIDE AS BEOL-COMPATIBLE DIFFUSION BARRIER AND LINER

4.1 Introduction

In previous two chapters, the fundamental diffusion barrier properties of 2D layered materials were first investigated. Then, the development of a BEOL-compatible 2D barrier was carried out. However, even with the demonstrated superior diffusion barrier properties of h-BN, MoS_2 or even graphene, integrating these completely new materials to the current technology might require a long-term development. According to ITRS [1], a sub-nm diffusion barrier/liner will be needed by 2021. Therefore, developing a 2D barrier/liner that can be directly integrated in a short term must be pursued urgently. Fortunately, with the demonstrated promising properties and with the large variety of material options in the 2D family, it is encouraging to look for a more industry-friendly 2D material. In the meantime, the industry can also put efforts to integrate the materials that have been tested (e.g. MoS_2 and graphene).

Therefore, in this chapter, we provide an approach that converts Ta, the standard liner material, to a 2D layered material, namely tantalum sulfide (TaS_x), which serves as an ultra-thin barrier and a liner at the same time. The ~1.5 nm thick TaS_x film is prepared on dielectrics (to demonstrate it can be deposited on IMDs) at a BEOL-compatible temperature. Our studies mainly focus on the comparison between (i) Ta and TaS_x for liner properties and (ii) TaN and TaS_x for diffusion barrier properties. This is the first time that adhesion properties of 2D layered materials are thoroughly explored for the liner application. The results show that TaS_x possesses superior liner and barrier properties simultaneously. In contrast, conventional TaN/Ta bilayer requires two types of thicker films to meet the requirements of both a barrier and a liner. By replacing the TaN/Ta bilayer with a 2D TaS_x layer, the percentage of Cu volume in an ultra-scaled interconnect can be significantly increased to achieve low line resistance. Showing the promising barrier/liner properties of TaS_x,

this work may encourage future development of high quality, single-layer tantalum sulfide films for BEOL applications.

4.2 Material Preparation and Characterization

2D materials are normally grown at high temperatures (> 800 °C), which does not satisfy the requirement of BEOL-compatibility. Therefore, as introduced in Chapter 1, plasma-enhanced chemical vapor deposition (PECVD) [19], [64], [65] was chosen to lower the growth temperature by utilizing the energy of remote plasma. Here, centimeter-scale, uniform TaS_x was prepared by converting a polycrystalline Ta film in a hot-zone furnace illustrated in Fig. 4.1(a). The Ta film was pre-deposited on a Si/SiO_2 substrate by an e-beam evaporator. After loading the Ta sample into the PECVD system, the tube furnace was pumped down. Nitrogen purging/chamber pumping were conducted repeatedly for ten times to remove moisture and other possible contamination sources from the ambient during the sample loading step. Meanwhile, the temperature was set at 400 °C, which was reached after 5-10 minutes. After reaching the base pressure of ~10 mTorr, Ar with a flow rate of 10 sccm was introduced. The pressure at this time was ~180 mTorr. Then, H_2S with a flow rate of 10 sccm was introduced and the pressure reached ~320 mTorr. After waiting for 5 minutes to stabilize the temperature and flow rate, plasma power was turned on and slowly increased to 70-80 W. At this power, the pressure changed to ~420 mTorr. After 20 minutes of growth, the plasma was turned off, followed by turning off the gases and the furnace heater. Here, hydrogen sulfide (H_2S) was used as the precursor while Ar was used as the carrier gas. During the growth, the remote plasma dissociated H_2S into H and S radicals. S radicals reacted with Ta and converted Ta to TaS_x. The mechanism of conversion is illustrated in Fig. 4.1(b), with 1T-tantalum disulfide (TaS_2) as an example. This method was modified from the method for low-temperature MoS_2 growth [64], [65]. Detailed material analyses will be discussed in the following paragraphs. In addition to the BEOL-compatible growth temperature, preparation of large-area films is also crucial to the integration with the interconnect technology. However, some of the 2D material synthesis recipes can only produce 2D flakes with micrometer-scale areas. Figure 4.1(c) confirms a large-scale, uniform polycrystalline Ta to TaS_x conversion was realized using our PECVD

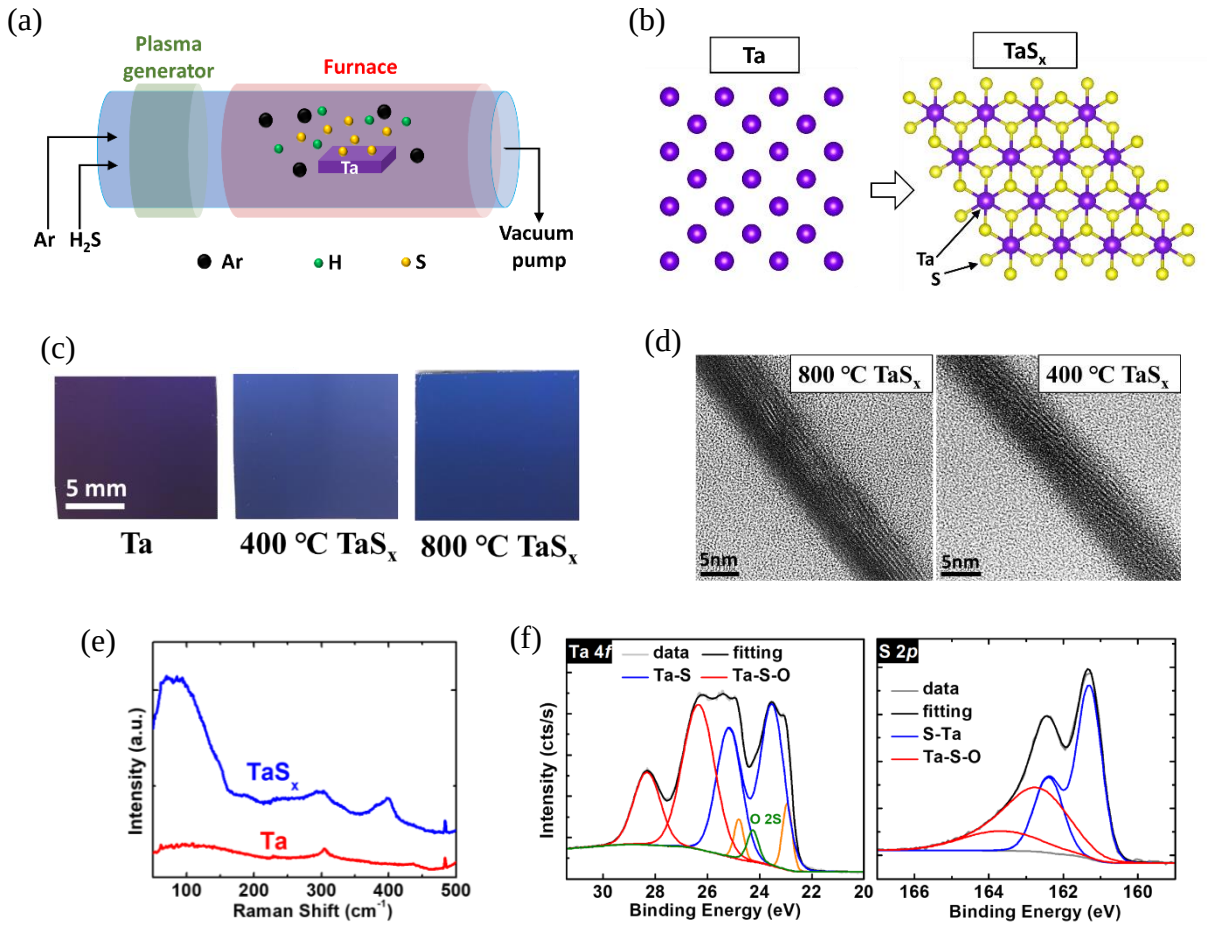


Fig. 4.1 (a) Schematic of the PECVD system for TaS_x growth. Plasma assists in dissociating H_2S and hence reduces the growth temperature. Sulfur radicals react with Ta and convert Ta to TaS_x. (b) Illustration of the conversion from Ta to TaS_x. The structure of 1T-TaS_2 is adopted for simplicity. (c) Top-view of large-area, continuous TaS_x converted from Ta. (d) TEM images showing the layer structures of thicker (~8 nm) TaS_x grown at different temperatures. (e) Raman spectra of TaS_x on Si/SiO_2 (90 nm). Characteristic peaks of 1T-TaS_2 is identified in 800 °C TaS_x. The wavelength of the laser used for Raman measurements was 532 nm. (f) XPS analysis of 400 °C TaS_x. Ta-S, Ta-S-O, and some Ta-N bonds (in orange) are detected. The ratio of Ta to S is 1: 2.5. Oxidized Ta is unavoidable due to the air-exposure before the measurement. The small amount and non-stoichiometric Ta-N cannot block Cu diffusion. An optimized TaS_x can bring even better diffusion barrier properties, while the TaS_x film demonstrated here has already shown to be able to block Cu diffusion efficiently.

method. As a demonstration, a ~3 nm Ta film was deposited on SiO_2(90 nm) grown on a Si(100) surface. After the conversion process through PECVD, a ~8 nm TaS_x film was formed at growth temperature of either 400 °C or 800 °C, as confirmed by the cross-section transmission electron microscopy (TEM) image in Fig. 4.1(d). The increased film thickness is consistent with the previously reported MoS_2 conversion [64]. The different colors between 400 °C and 800 °C conversion shown in the optical microscope images of Fig. 4.1(c) may imply different material properties, as will be discussed further. Layered structures can be observed in the TEM images. Some oxidized TaS_x can be observed on the top of the film from the TEM image due to surface oxidation. Unreacted Ta can also be found at the bottom (from TEM) of the TaS_x film grown at 400 °C, which can be attributed to the insufficient energy at the lower process temperature. Note that these thick (~8 nm) TaS_x films were intentionally selected for better imaging of the layered structures. For all electrical tests that will be discussed, TaS_x with the thickness of interest (~1.5 nm) will be used.

Raman spectra in Fig. 4.1(e) reveal that the 800 °C TaS_x is 1T-TaS_2 [36], [66], as the related peak at around 100 cm^{-1} was observed. The peak can only be resolved into multiple TaS_2 peaks at low temperatures [36]. However, this peak was not observed in the 400 °C TaS_x. The material was further investigated by X–ray photoelectron spectroscopy (XPS). Monochromatic XPS was employed in this work using a system described elsewhere [67]. The *AAnalyzer* software was used for XPS peak analysis [68]. Active Shirley background and Voigt line shape was employed for peak fitting. For all chemical states detected at Ta 4*f* core level, the binding energy separation between $4f_{7/2}$ and $4f_{5/2}$ is 1.9 eV with the same Lorentzian (0.11). Gaussian is larger for Ta-O-S chemical state due to formation of new bonds. Similar for S 2*p* core level, binding energy separation (1.1 eV) and Lorentzian (0.11) for $2p_{3/2}$ and $2p_{1/2}$ is the same for S-Ta and S-Ta-O chemical states. While Gaussian is larger and broader for S-Ta-O bonding. Corresponding to Ta-S-O chemical state at S 2*p* and Ta 4*f* core levels additional chemical state observed at O 1*s* core level at lower binding energy (~530 eV). Figure 4.1(f) shows the Ta 4f and S 2p core level spectra of the 400 °C TaS_x film obtained by XPS using a monochromatic Al Kα radiation ($h\nu$=1486.7 eV). Spectral features associated with Ta-S bond are detected at 23.5 eV and 161.3 eV in the Ta $4f_{7/2}$ and S $2p_{3/2}$ core levels, respectively. Based on XPS analyses, S to Ta ratio was estimated to be ~2.5 ($TaS_{2.5}$). An additional chemical state is detected at higher binding energy in the Ta 4*f* (26.2

eV) and S 2*p* (162.5 eV) core levels aside from that of the Ta-S bond. The binding energy of the new chemical state is lower than the reported value [66], [69] for Ta_2O_5, but higher than the Ta-S chemical state, which is assigned to the formation of Ta-S-O compound with a stoichiometry of $TaO_{1.9}S_{2.1}$. The Ta 4*f* core level shows also a chemical state at lower binding energy (22.9 eV). The binding energy of this chemical state in the Ta 4*f* core level, in conjunction with the additional chemical state detected in the N 1*s* core level at 396.4 eV, suggests the formation of a covalent Ta-N bond (labeled in orange) [70]. The intensity ratio of Ta-N to Ta-S features is 0.14. We presume that Ta-N does not play a significant role in blocking Cu diffusion, based on its relative concentration and the non-stoichiometry ($TaN_{1.3}$). It is also important to note that the Ta 4*f* core level region is convoluted with O 2*s* core level at 24.0 eV. Based on the physical characterization, the composition of the converted film appears to consist of $TaS_{2.5}$ layers mixed with naturally-oxidized $TaS_{1.9}O_{2.1}$ region. It is noted that not only TaS_2 is well-known to exhibit layered structures, but TaS_3 has also been reported to exhibit such structures [71]. In addition, the phase diagram [72] shows that TaS_3 tends to be formed at lower temperatures with H_2S as the precursor, while TaS_2 can be formed at higher temperatures. Based on these observations, we will denote this film as TaS_x to avoid any misinterpretation. The main purpose of this work is to study the liner and diffusion barrier properties of this "TaS_x" film.

Although the TaS_x film shown in the cross-section TEM image (Fig. 4.1(d)) was around 8 nm, for the electrical test structures for the barrier and liner properties, TaS_x thin films with thickness of the interest were adopted. The thickness is ~1.5 nm, close to the thickness of a two-layer (2L) TaS_2, as confirmed by atomic-force microscope (AFM) in Fig. 4.2(a). Three-layer (3L) regions were also found occasionally, with the thickness of ~2 nm. A more precise thickness control can be achieved by using other Ta deposition methods. For the simplicity, this film will be denoted as "1.5 nm TaS_x" throughout the rest of the chapter.

4.3 Tests of Liner and Diffusion Barrier Properties

4.3.1 Liner Properties

Ta has been used as the "liner" to provide good Cu adhesion, enabling survival after multiple damascene process steps [1], [3], [4]. However, it is also well known that the inelastic scattering at the Ta/Cu interface [73], [74] can increase Cu resistivity, especially when Cu wire dimensions are extremely scaled. Since the reason of utilizing an ultrathin 2D layered TaS_x barrier/liner is to address the issue of conductivity degradation in extremely scaled interconnects, it is important to understand the impact of TaS_x on the surface scattering of Cu interconnects. Here, such surface scattering at the SiO_2/Cu, Ta/Cu, and TaS_x/Cu interfaces was studied. To facilitate the analysis, ultra-thin Cu films with thicknesses of ~15 nm were deposited on the above-mentioned three different surfaces to enhance the contribution from the interface. Cu thin films were patterned into Kelvin structures for accurate resistance measurements, as illustrated in Fig. 4.2(c). Figure 4.2(d) shows the measured Cu resistivity of multiple devices on the three surfaces. Despite the fact that Cu resistivity increases as its dimension decreases [75], the thinnest Cu (13 nm) on TaS_x has the lowest resistivity among the three groups, indicating a more specular/elastic interface scattering. The enhancement of Cu conductivity by inserting/capping with a 2D layered material has also been observed and studied in other works [16], [76]–[78]. It is believed that the inferior conductivity of Ta/Cu and SiO_2/Cu can be attributed to the perturbing localized interfacial states [76], [77]. In contrast, the weaker interaction between 2D layered materials and Cu [79] is expected to result in a less perturbed interface and hence preserve the pristine Cu surface states more effectively [77]. Previous works have also shown the reduced surface scattering in Cu with exfoliated MoS_2 or WSe_2 [76], [80], or with MOCVD-grown MoS_2 at 400℃ [81], as the resultes summerized in Table 4.1. It can be observed that when Cu is deposited on a better-quality film, such as the exfoilated MoS_2, the reduction in resistivity is more than that in CVD-grown films. This could be attributed to a larger grain size (tens of micrometers) of exfoliated films, where the entire Cu wire is located on top of a single grain of the 2D film. On the other hand, there are normally mutiple grains of the CVD-grown films underneath a single Cu wire, which could introduce additional scattering effects.

In addition to the surface scattering effect of a liner on Cu resistivity, the wettability and adhesion of Cu to liners are also of great importance. The former is essential to provide a good surface for

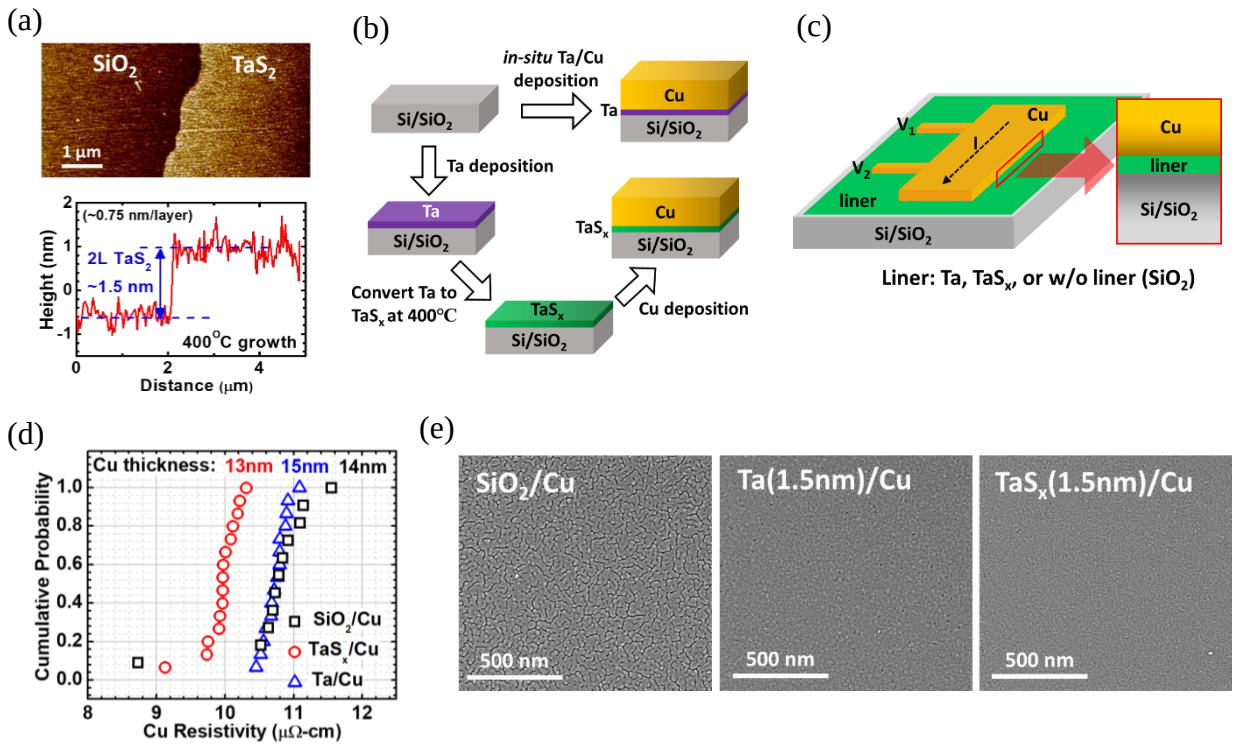


Fig. 4.2 Device structures and tests of liner properties of 400 °C TaS_x. (a) AFM profile of 1.5 nm TaS_x grown at 400 °C. This film is used for all the liner and barrier tests. (b) Sample fabrication procedure. Ta/Cu stack is deposited *in-situ*, while TaS_x has been exposed to air before Cu deposition. An *in-situ* Cu deposition on TaS_x could bring an even better performance. (c) Cu thin film patterned into Kelvin structure for resistance measurements. Ultra-thin Cu (~15 nm) film is adopted to enhance the contribution of the interface. (d) Cu resistivity on various surfaces. In general, thinner Cu is expected to have a higher resistivity. Nevertheless, the thinnest Cu (13 nm) on TaS_x has the lowest resistivity, indicating suppression of surface scattering at the TaS_x/Cu interface. (e) Wetting properties of Cu tested by depositing ultra-thin Cu (~10 nm) on different surfaces. Numbers of cracks can be observed when Cu is on SiO_2, while Cu on 1.5 nm Ta and on 1.5 nm TaS_x have smooth morphologies. The results show that TaS_x can provide a good wettibility as Ta does for Cu seeding layers, which is important for the subsequent Cu electroplating.

the Cu seeding layer and for the subsequent electroplating of Cu, while the latter is crucial for Cu to survive chemical-mechanical polishing (CMP) processes and directly impacts the electromigration lifetime of Cu wires [82]. To investigate the wettability, much thinner Cu films (~10 nm) were deposited on different surfaces. The left panel of Fig. 4.2(e) reveals lots of cracks on the Cu film deposited on SiO_2, indicating a poor wettability. In contrast, TaS_x provides a good wettability as Ta does, as can be observed in the middle and right panels of Fig. 4.2(e). The adhesion of Cu on TaS_x was verified by a tape test method [83]. After the preparation of TaS_x partially on a Si/SiO_2 substrate, ~80 nm Cu was deposited on the entire substrate followed by the attachment of a 3M Scotch® Tape for a simple adhesion test [83]. After detaching the tape, only the regions with TaS_x had Cu left; Cu on SiO_2 regions was detached by the tape, as shown in Fig. 4.3(a). The tape test method was also used to evaluate the adhesion between Cu and other 2D layered materials, as the results summarized in Table 4.1. It is observed that graphene and MoS_2 cannot pass the test, which could be attributed to the weak van der Waals force interaction between Cu and 2D layers. On the other hand, TaS_x shows superior adhesion with Cu. Possible reasons could be (i) the oxidized (Ta-S-O) regions are not bonded with Cu through the van der Waals force and (ii) TaS_x retains the adhesion property from Ta. Further studies are required for a better understanding. Furthermore, an industrial-standard four-point bending method [84] was adopted to evaluate the adhesion of TaS_x to Cu. As shown in Fig. 4.3(b), TaS_x has a slightly higher adhesion energy than Ta, suggesting a superior adhesion to Cu. All the test results above indicate that TaS_x can serve as a favorable liner for Cu. This is the first time the adhesion of a 2D layered material to Cu is verified.

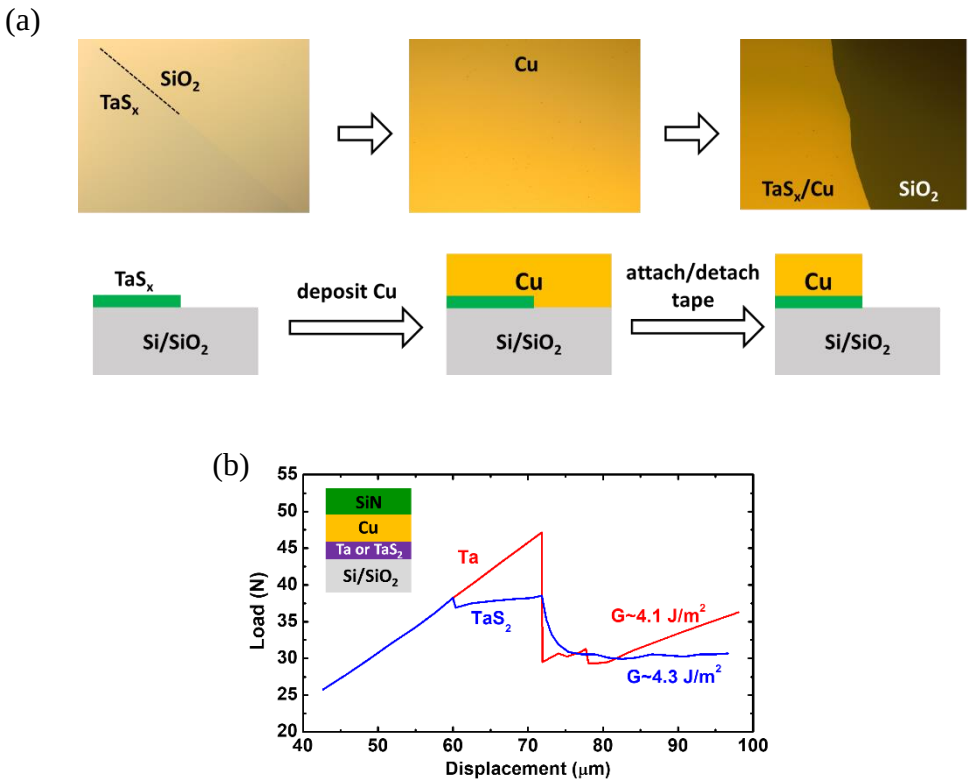


Fig. 4.3 (a) Adhesion tests using the tape method. ~80 nm Cu is deposited on both TaS_x and SiO_2 regions. After detaching the tape, only Cu on TaS_x region remains, indicating that TaS_x is a good liner for Cu to survive CMP processes. (b) Adhesion tests using industrial-standard four-point bending method. The test structure is depicted in the inset. TaS_x has a slightly higher adhesion energy than Ta, suggesting a superior adhesion to Cu.

Table 4.1 Summary of liner properties of various 2D layered materials in different aspects. The 2D materials used for the adhesion test are all CVD-grown since a large area is needed for the test.

Reduction of Cu (15-nm thick) resistivity		**Adhesion test**	
Exfoliated MoS_2	~46 %	Ta (standard liner)	pass
Exfoliated WSe_2	~23 %	TaS_2	pass
MOCVD MoS_2 (400 °C)	< 5 %	MoS_2	fail
PECVD TaS_2 (400 °C)	~10 %	graphene	fail

4.3.2 Diffusion Barrier Properties

The diffusion barrier properties of TaS_x were tested by time-dependent dielectric breakdown (TDDB) measurements [41], [43], [47], [58], as described and employed in the previous two chapters. Figure 4.4(a) shows the current evolution with the stress time at 7 MV/cm of multiple devices. Sudden current jumps indicate device breakdown. It can be observed that t_{BD} of most devices increases when Ta is converted to TaS_x, suggesting improved diffusion barrier properties. The values of t_{BD} of multiple devices were further plotted in the statistical distribution shown in Fig. 4.4(b), where each point was obtained from one device. At a certain electric field, the device with the shorter/longer t_{BD} was assigned to have the lower/higher value of the cumulative probability. Therefore, a straight line with a positive slope can be obtained. Medium-time-to-failure ($TTF_{50\%}$) was extracted from the figure for an easier comparison between different materials. From Fig. 4.4(b), it is obvious that TaS_x devices have ~6 times longer lifetime than Ta devices at 7 MV/cm.

Although TaN mainly serves the barrier function in the conventional barrier/linear bilayer, Ta can also contribute to the blocking of Cu diffusion. Figure 4.4(c) indicates that 1.5 nm TaS_x has similar barrier properties as 3 nm Ta, which is essential to the barrier/liner thickness scaling requirement. Since TaN plays the dominant role in mitigating Cu diffusion, TaS_x is also benchmarked to TaN results from other work [57]. It can be observed in Fig. 4.4(d) that 1.5 nm TaS_x has similar performance as 2 nm TaN in terms of mitigating Cu diffusion. Based on the experimental results of liner and diffusion barrier properties, it is possible to reduce a 5 nm TaN/Ta stack (2 nm TaN + 3 nm Ta) to a 3 nm TaS_x layer while maintaining or even improving the barrier/liner performance. Further scaling can be achieved given the 2D material nature of TaS_x. The projection of significant resistance reduction benefitting from the maximized Cu volume is provided in Fig. 4.4(e).

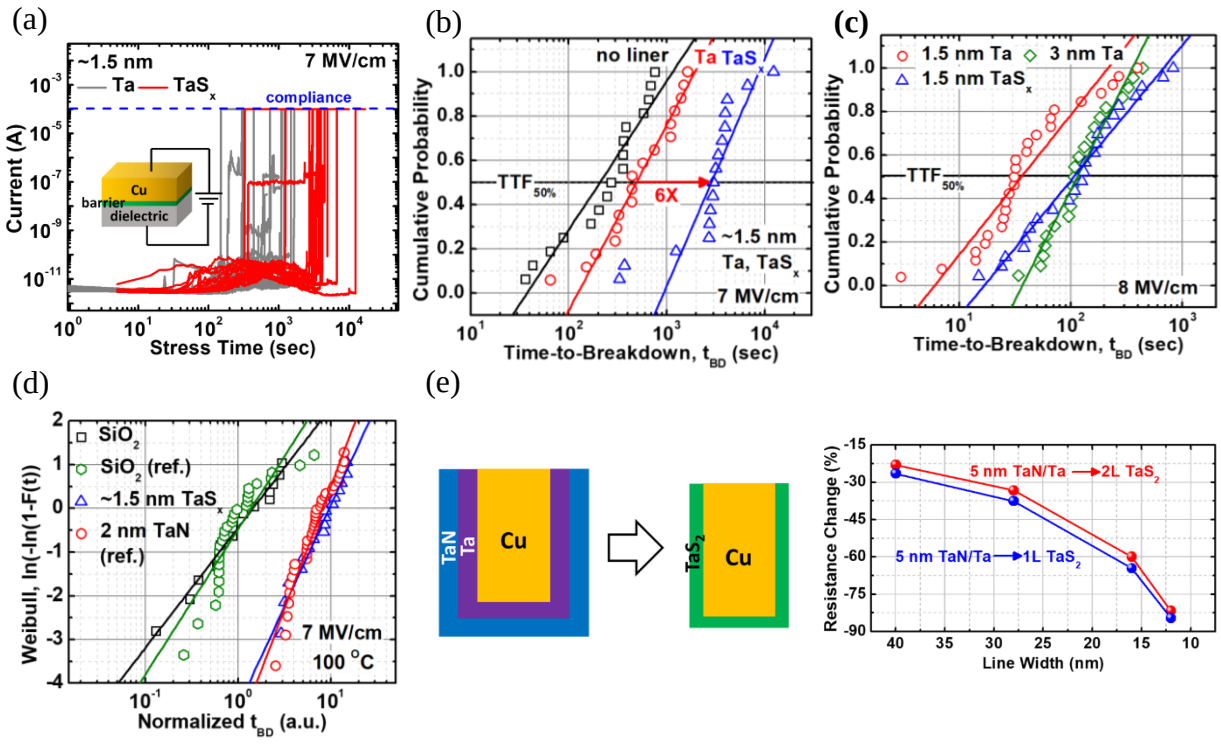


Fig. 4.4 (a) Current versus stress time of devices with Ta and TaS_x. Devices with TaS_x have longer lifetime in general. (b) Statistical distribution of devices with Ta and TaS_x barriers. By converting Ta to TaS_x, medium-time-to-failure ($TTF_{50\%}$) increases by 6 times. (c) 1.5 nm TaS_x has similar diffusion barrier properties as a 3nm Ta. Since Ta also plays a (minor) role in blocking Cu diffusion, this result indicates the Ta liner thickness can be reduced by using a thinner TaS_x and Cu volume can be increased. (d) Benchmarking diffusion barrier properties of ~1.5-nm TaS_x against 2-nm TaN. Two materials have a comparable diffusion barrier property. Improvement of TaS_x qualify can further reduce the required thickness. (e) Resistance reduction at various line widths with the thinner barrier/liner layer by using TaS_x. The improvement in narrower interconnect is more significant. A method to have a single-layer/high-quality TaS_x can lower the resistance much more tremendously.

4.4 Other Aspects of Using TaS_x as Diffusion Barrier and Liner

4.4.1 Electromigration

One of the limiting factors of the lifetime of a metal wire is its resistance to electromigration (EM). EM occurs in metal wires due to the momentum transfer between electrons and metal atoms [85]. Voids in metal wires and vias will eventually appear due to the current induced atom movement, leading to the malfunction of interconnects. According to the International Technology Roadmap for Semiconductors [1], with reduced interconnect cross-sections and increased maximum operation frequency, the maximum current density (J_{max}) required for targeted performance will become closer to or even exceed the current density (J_{EM}) for EM to occur. As a result, EM must be mitigated in order to maintain continued performance improvement. As depicted in Fig. 1.2 (b), a Cu wire is surrounded by barrier/liner on the sidewalls and bottom of the trench. At the top surface, Cu is polished by the CMP process. Studies have shown that this post-CMP surface becomes one of the dominant paths for EM to occur [82]. To alleviate the CMP damage and enhance EM lifetime, various materials, such as Co [86], CoWP [82], [87], and the related [87], have been capped on the top surface of Cu along the history of interconnect development. These layers are also referred to as the "capping layers."

Although TaS_x here is not aimed at being used as a capping layer, it must not deteriorate the EM lifetime. Therefore, we tested the impact of TaS_x on EM. The test structure is similar the Kevin structure illustrated in Fig. 4.2(c). Due to the limitation of a non-industrial setup, J_{max} is measured to avoid extremely long measurement duration. As shown in Fig. 4.5 (a), as the applied current density increases, the wire resistance increases, which can be attributed to both Joule heating and EM. We defined J_{max} as the current density when resistance increases by 10%. Figure 4.5 (b) shows J_{max} of multiple Cu wires with Ta or TaS_x as the liner. It can be observed that TaS_x leads to larger variation due to the less mature process compared to that of Ta. Nevertheless, the average J_{max} values in both instances are similar, indicating TaS_x does not degrade EM lifetime when being used as a liner.

4.4.2 Cu Corrosion during Sulfurization

As extensively discussed in the previous chapters, most parts of barrier/liner are deposited on dielectrics. However, the deposition on Cu should also be considered since a small portion of barrier/liner is deposited on Cu, more specifically, the bottom of a via, as illustrated in Fig. 4.6. The ideal case of TaS_x deposition is described in Fig. 4.6(a), where TaS_x is carried out by sulfurizing Ta deposited in the trench. However, Cu is susceptible to corrosion from the sulfur precursor. Therefore, as depicted in Fig. 4.6(b), lower-level Cu would be corroded during the sulfurization process when it encounters sulfur species from via bottom. In contrast, for conventional sputtered TaN/Ta, no damage to Cu exists with the absence of sulfur species. Note that this corrosion issue of Cu could also occur when growing other types of TMD.

To resolve this issue, a protection layer for Cu from sulfur may be useful. However, depositing an additional layer will result in an increased thickness of barrier/liner, compromising the benefits of using 2D materials. Therefore, a protection layer that can be selectively deposited on Cu surface, without any formation on the trench dielectrics is required. Thanks to the recently increased interest in selective deposition, many works using self-assembled monolayer (SAM) [88] to enable selective depositions have been demonstrated. For example, in the work of Hashemi et al. [89], SAM can be selectively deposited on Cu, instead of on the neighboring Si, which exactly meets our needs. On the other hand, as mentioned in the previous section, graphene prefers to be deposited on Cu than on dielectrics. Therefore, graphene can also be used for this purpose. In fact, studies have shown that both SAM [90], [91] and graphene [92], [93] are promising barrier against corrosion. Therefore, both materials are great candidates to serve as corrosion barriers that can be selectively deposited on Cu. The proposed process flow is illustrated in Fig. 4.6(c), using graphene as the example. First, the protection layer is only deposited on Cu surface instead of on the dielectric, followed by Ta deposition along the trench. Then, the sulfurization process can be performed to convert Ta to TaS_x. To test the feasibility of this approach, ~120-nm Cu is patterned and partially deposited on SiO_2. A graphene layer is then selectively deposited on Cu. Finally, ~3-nm-Ta is deposited on the entire sample. The region with Ta on SiO_2 represents the trench sidewall, while the region with Cu represents the surface of lower-level Cu at the via bottom, as indicated in the middle panel of Fig. 4.6(d). After the sulfurization, clear color change of Ta can be observed in the right panel of Fig. 4.6(d), indicating the conversion to TaS_x. Note that the relatively thick

(~3 nm) Ta was intentionally chosen for a better color contrast. As for the Cu region, although pinholes on Cu are observed, graphene has already largely prevented Cu from the corrosion. Without the presence of graphene, Cu will be completely etched away by sulfur, as shown in the left panel of Fig. 4.6(d). To demonstrate an all-BEOL-compatible process, graphene here is grown at 400 ℃, which has a compromised quality. However, if high-quality graphene grown at low temperatures is available, such as the one developed by Shi et al. [94], the damage can be much more reduced.

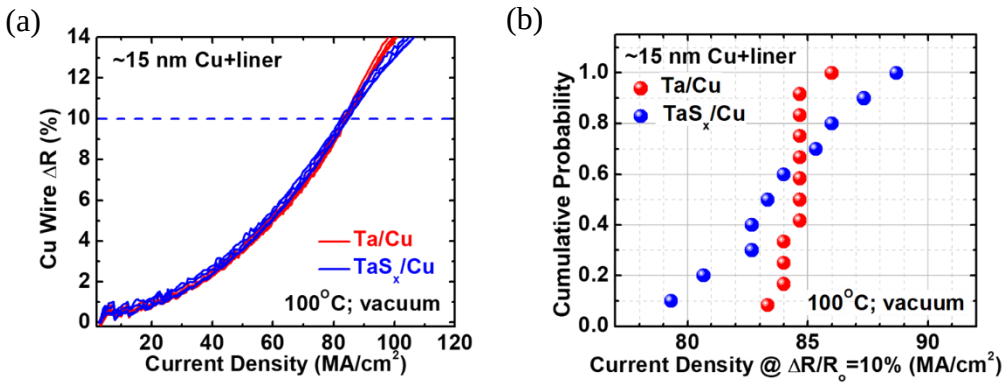


Fig. 4.5 (a) Resistance increase with the stress current density. Current density that leads to 10% of resistance change is defined as the J_{max}. (b) Distribution of J_{max} of Ta/Cu and TaS_x/Cu. Two liners have the similar effect on J_{max}, while TaS_x results in a larger variation. Improving the uniformity of TaS_x could reduce the variation.

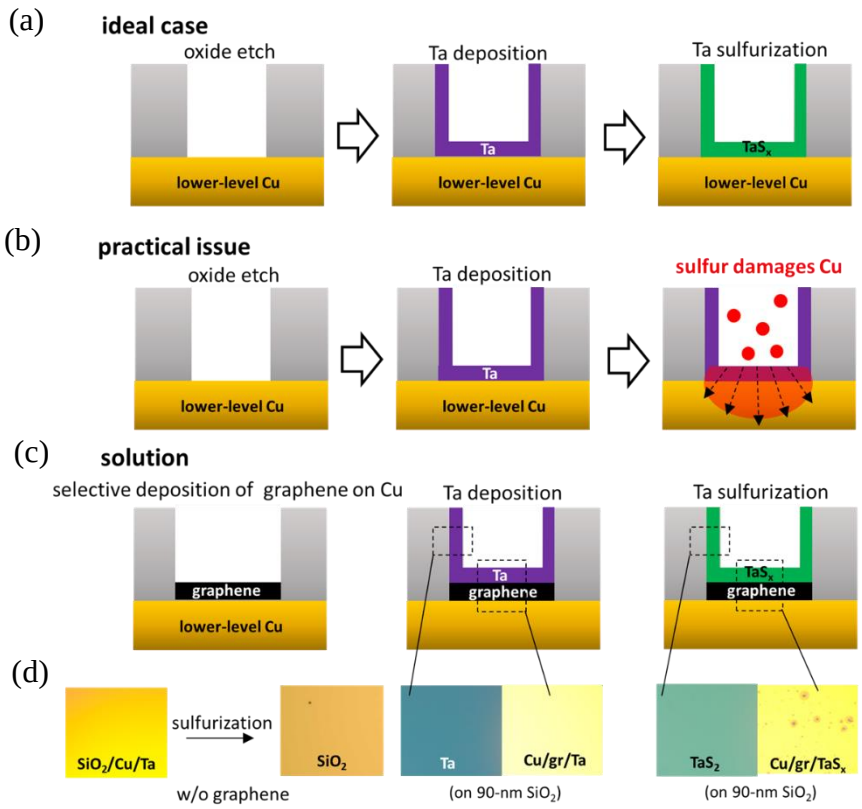


Fig. 4.6 (a) Ideal process flow to synthesize TaS_x in the trench. (b) Practical issue encountered during the sulfurization. The sulfur species can corrode the lower-level Cu from the bottom of via. This issue could also happen during the growth for other types of TMD. (c) Proposed solution adopting a selective-deposited corrosion barrier on Cu. Both SAM and graphene can be used. Graphene is adopted here. (d) (left) Optical image showing Cu can be completely etched away after the sulfurization process if no corrosion barrier is utilized. (middle) Optical image of the sample used to test the feasibility of graphene as the corrosion barrier. In one region, Ta is deposited on SiO_2; whereas graphene is selectively deposited on Cu followed by the same Ta deposition in SiO_2 region. (right) After the sulfurization, most Cu remains thanks to the graphene corrosion barrier. A few pinholes exist due to the low quality of graphene.

4.5 Conclusion

In summary, a ~1.5 nm TaS_x barrier/liner is realized by converting Ta using PECVD at a BOEL-compatible temperature. This work considers critical integration aspects of this 2D material in terms of liner and barrier properties. The liner properties are evaluated based on (i) surface scattering at various interfaces, (ii) wettability that TaS_x can provide for the subsequent Cu seeding layers, and (iii) adhesion of Cu to TaS_x. The TaS_x film passes all the tests, which is demonstrated in 2D layered materials for the first time. The diffusion barrier properties are analyzed by time-dependent dielectric breakdown (TDDB) measurements. The TDDB results show better barrier properties after Ta being converted to TaS_x. Additionally, the benchmark of TaS_x against TaN indicates enhanced Cu blocking capability. The test results of liner and diffusion barrier properties are summarized in Table 4.2. Our accomplishments compared to other works are summarized in Table 4.3. Further improvement of the film quality can be expected to bring even better barrier performance. Based on the evaluations, a conventional TaN/Ta bilayer stack can be replaced with an ultra-thin TaS_x layer to maximize the Cu volume for ultra-scaled interconnects. Further optimization/development of CVD or atomic-layer deposition (ALD) based growth methods may realize even thinner (single-layer; < 1 nm) and more uniform 2D TaS_x barrier/liner. In addition to the benchmark of liner and diffusion barrier properties, the aspects regarding electromigration and Cu corrosion when TaS_x is adopted are discussed.

Table 4.2 Test results of liner and diffusion barrier properties. The liner properties are tested in three aspects, while the analysis of diffusion barrier property focuses on the capability of blocking Cu diffusion

Liner Property		**Diffusion Barrier Property**	
Cu surface scattering	TaS_x reduces surface scattering →Cu resistivity decreases	compared to Ta	better
Cu wetting	no obvious cracks in Cu thin films deposited on TaS_x →TaS_x provides a good surface for Cu seeding layer	compared to TaN	similar
Cu adhesion	pass tape and 4-point bending tests →could survive CMP process		

Table 4.3 Comparison of different works using 2D layered materials as Cu diffusion barriers. Only the TaS_x barrier/liner in this work satisfies all of the requirements.

Material	**Growth Temperature (BEOL-Compatible?)**	**Transfer-Free?**	**BARRIER PROPERTY?**	**Liner Property?**
Graphene [95]	1000 ℃ (NO)	NO	YES	NO
Graphene/ graphene oxide [14]	750 ℃ (NO)	NO	YES	NO
Graphene [12], [13]	NO	NO	YES	NO
Graphene [15]	550 ℃ (NO)	YES	YES	NO
Graphene [80]	400 ℃ (YES)	YES	YES	NO
MoS_2 [96]	850 ℃ (NO)	YES	YES	NO
TaS_x (This Work)	400 ℃ (YES)	YES	YES	YES

5. VERTICAL CONDUCTION OF 2D LAYERED MATERIALS

5.1 Introduction

"Via" is the connection between interconnects at different levels, as can be observed in Figs. 1.1 and 5.1. Via resistance has become one of the major bottlenecks for overall interconnect performance at advanced technology nodes. When current flows from an upper level Cu wire, through a via, to a lower-level Cu wire, it has to go through the highly resistive TaN/Ta layer at the bottom of the via. As mentioned above, since the thickness of the barrier/liner stack cannot be scaled proportionally, the via resistance becomes even larger with the via width (area) scaling. Although the ultra-thin 2D barrier/liner has the advantage of enlarging the Cu cross-sectional area, the vertical current conduction across these novel materials has seldomly been discussed. Therefore, the impacts of 2D materials on via resistance must be investigated before concluding these novel materials can be integrated without performance loss. Among the few 2D materials that have been investigated for BEOL applications, TaS_x is chosen for the study here since it has been evaluated more thoroughly from various aspects and benchmarked with conventional materials, as described in Chapter 4. Early works have shown that in-plain resistivities at room temperature of 1T-TaS_2 and 2H-TaS_2 are ~300 μΩ-cm and 150 μΩ-cm, respectively [97]–[99], both of which are lower than that of TaN (~700 μΩ-cm) [100]. However, unlike TaN or Ta, the conduction in 2D materials is anisotropic, meaning that the out-of-plane (vertical) resistivity of TaS_2 could be very different from their in-plane counterparts. In fact, the out-of-plane resistivity of 2H-TaS_2 is ~5000 μΩ-cm [98], while it reaches 7×10^5 μΩ-cm in 1T-TaS_2 [99]. Despite the high vertical resistivity of TaS_2, the overall resistance of TaS_2/Cu via could still outperform conventional structure of TaN/Ta/Cu since (i) the required thickness of TaS_2 can be thinner and (ii) the enlarged Cu volume by 2D barrier/liner becomes even more significant in ultra-scaled dimensions, both of which will be elaborated in this Chapter.

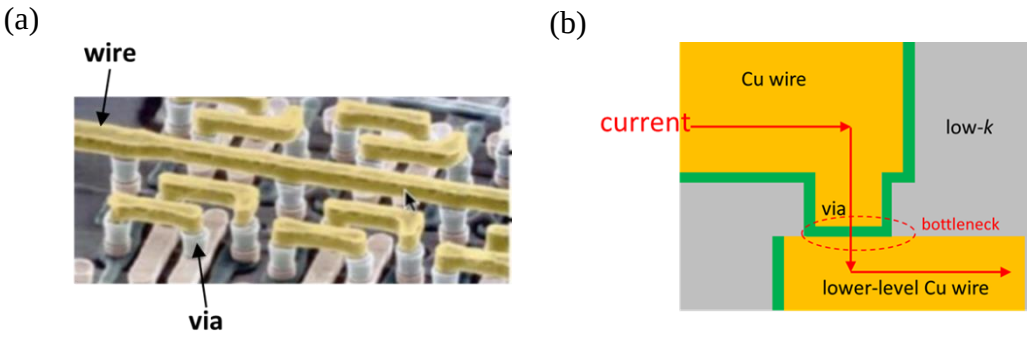


Fig. 5.1 (a) SEM image of an interconnect structure. Cu wires and vias can be observed. (source: Synopsis) (b) Schematic of the cross-section of an interconnect structure with two levels of Cu wires and a via connecting the wires. The direction of current flow is indicated. The conduction across the bottom of via has become the bottleneck due to the resistive and hardly scalable TaN/Ta.

However, the abovementioned vertical resistivity is that of a high-quality and unoxidized film. In reality, because of the material nature, after Ta is converted to TaS_x using the PECVD method described in Chapter 4, the TaS_x film could get oxidized during the transferring to the chamber for metal deposition. The oxide layer in-between 2D barrier/liner and the metal on top could seriously degrade the vertical conduction. The similar situation can also occur to Ta and TaN since both materials are also prone to be oxidized. Nevertheless, the industry has managed to avoid or remove the oxides of Ta and TaN with their well-designed equipment. In this chapter, we will also try to use some similar approaches to realize an oxide-free interface between TaS_x and metal deposited on it. In the following discussions, I will first verify the existence of oxides in our PECVD TaS_x and show the impacts of the oxides on vertical conduction. Then, modified processes will be employed to avoid the oxide layer at 2D/metal interface. Finally, the intrinsic property of TaS_2 will be studied to understand the best possible vertical conduction that can be achieved.

5.2 Impact of Oxide on Vertical Conduction

The vertical resistivity of the PECVD TaS_x is measured using the "vertical Kelvin structure," as illustrated in Figs. 5.2(a) and 5.2(b). The horizontal version of Kelvin structure has been shown in Fig. 4.2(c). This type of structure enables the measurements of current and voltage independently and hence resistance can be measured accurately. 20-nm-Ta is patterned and deposited on Si/SiO_2 substrate as bottom electrodes. Then, the Ta film is sulfurized using the PECVD method for 5

minutes, with other parameters the same as those described in Chapter 4, to form ~2 nm of TaS_x on the surface of Ta. To define the area of vertical current conduction, ~160 nm SiO_x (hydrogen silsesquioxane, HSQ) with an opening patterned (by e-beam lithography) in the middle is deposited as an isolation layer for top and bottom electrodes. Finally, 150-nm Cu/100-nm Al are patterned and deposited as top electrodes. E-beam lithography and lift-off processes are used for this fabrication. The process flow is depicted in Fig. 5.2(c). When conducting a measurement, current (*I*) flows from one of the top electrodes, through the opening in SiO_2, through TaS_x, and finally reaches one of the bottom electrodes, as indicated by the red arrow in Fig. 5.2(b). Meanwhile, the voltage difference (ΔV) between the other top electrode and the other bottom electrode is measured. By diving ΔV by *I*, an accurate vertical resistance value can be obtained. Furthermore, due to the known thickness of TaS_x and its much higher resistance than the metal electrodes, vertical resistivity of TaS_x can be calculated. The best vertical resistivity obtained is ~2.5×10^7 μΩ-cm, which is much higher than ~700 μΩ-cm of TaN. The reasons will be discussed. When current density-voltage (*J*-*V*) sweeps are conducted, "resistive-switching" behaviors are observed in all devices, as shown in Fig. 5.3(a). This is a typical behavior in metal-oxides resistive-switching memories, where the switching is attributed to ion/atom movement in the oxide layer [101]. In fact, a test structure without the SiO_x layer is also fabricated, and the same behavior is also observed, indicating the resistive switching does not happen in the SiO_x layer. Therefore, it is believed that this behavior is directly related to the oxidized TaS_x. In addition, after a few switching operations, the *J*-*V* curve becomes very "linear," as shown in Fig. 5.3(b), which can suggest some of the oxides have been broken through locally and current conducts mainly through those regions. As observed in the process flow in Fig. 5.2(c), there are many steps involving long-term air exposure, which could be the main reason for the oxide formation. To further verify this, a modified process flow that largely reduces the time of air exposure is adopted, as illustrated in Fig. 5.2(d). Shadow masks are utilized for Cu patterning in this modified process flow, instead of using lithography processes, to reduce the duration of air exposure. A control sample without TaS_x formation is also fabricated. As can be seen in Fig. 5.3(c), the current-voltage (*I*-*V*) curve is linear; no resistive-switching is observed, indicating oxides formation is largely prevented. However, accurate resistance cannot be measured in this approach since the vertical Kelvin structure is not available without lithography being employed.

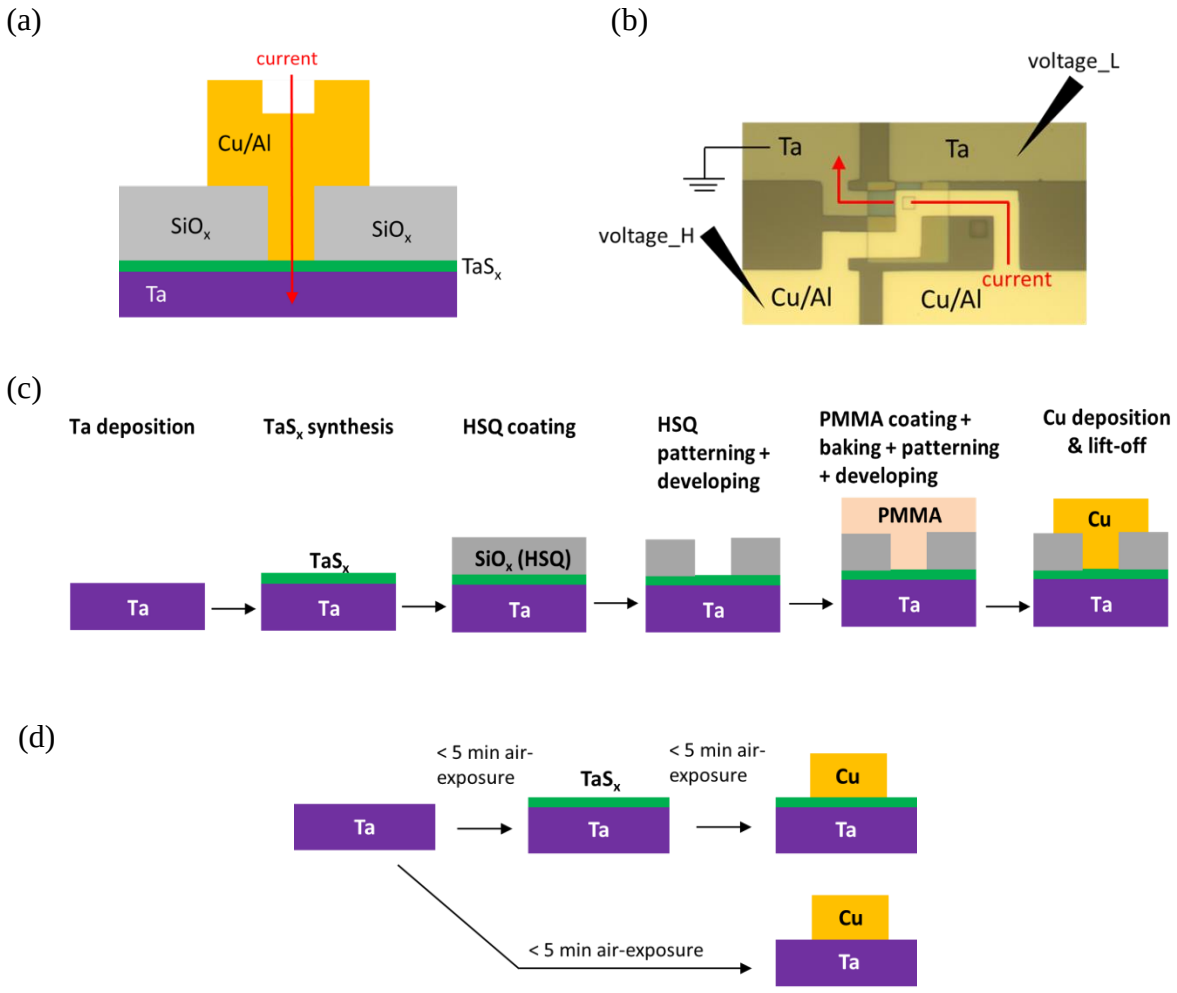


Fig. 5.2 (a) Schematic of the cross-section and (b) optical microscope image of the top view of the vertical Kelvin structure. Current flow from one of the top electrodes through TaS_x area defined by the SiO_x isolation, to one of the bottom electrodes. Voltage difference between the other top and bottom electrodes is measured. By separately measuring the current and voltage difference, accurate resistance can be obtained. (c) Process flow of the vertical Kelvin structure. Lithography is used for metal patterning. Multiple steps involving air exposure is unavoidable. (d) Modified test structure with a process flow that greatly reduces the duration of air exposure. Shadow masks are used for metal patterning.

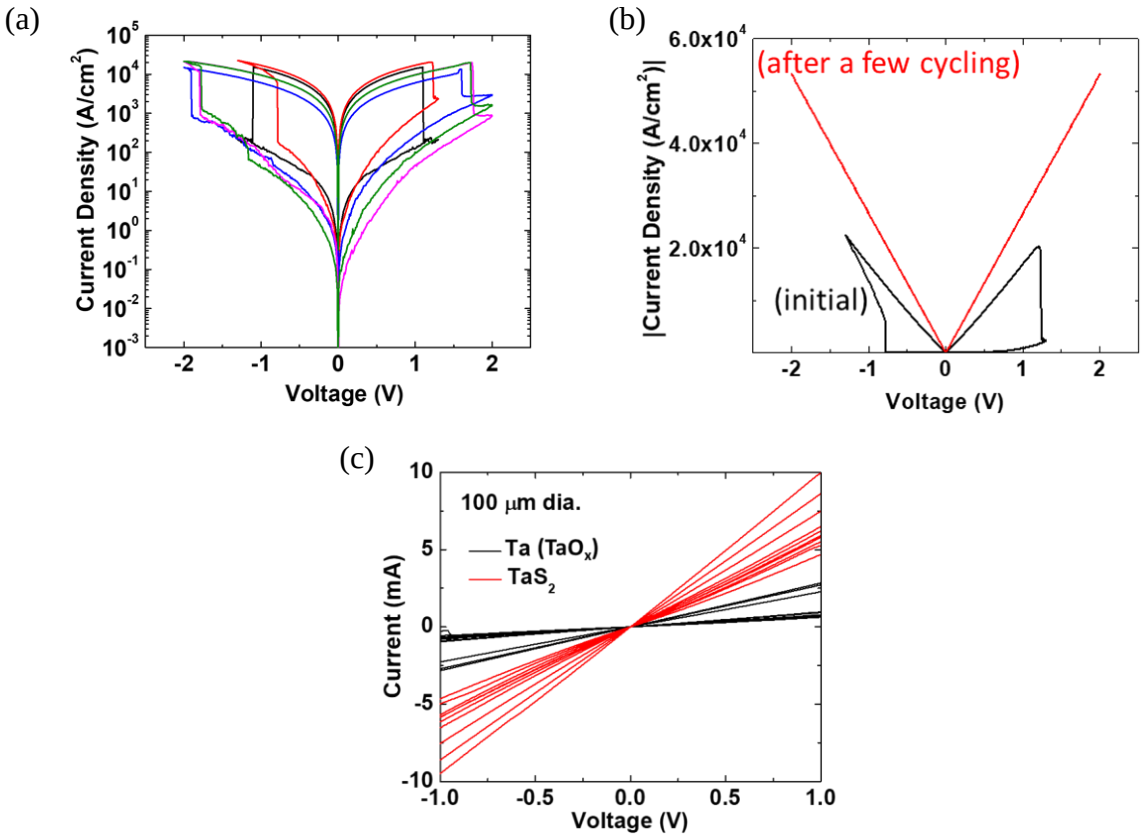


Fig. 5.3 (a) *J-V* characteristics of devices in the vertical Kelvin structure. Resistive-switching behaviors are observed in all devices, which could be attributed to the oxides in TaS_x. (b) After a few *J-V* cycling operations, the curve becomes linear, suggesting some oxides have been broken through locally. (c) *I-V* characteristics of devices fabricated in the modified structure shown in Fig. 5.2(d). Linear behaviors are observed even at the beginning, indicating the oxides formation have largely been prevented.

5.3 Realization of Oxide-Free Interface

To realize an oxide-free interface and improve vertical conduction, two approaches are explored. The first one employs a different (from previous PECVD) system that can form 2D material and deposit metals in the same vacuum system; whereas the second approach sputters out the oxides on the surface of TaS_x grown by the PECVD, followed by metal deposition in the same system.

5.3.1 *In-situ* 2D Material Formation with Metal Deposition

As shown in Fig. 5.4(a), in our standard PECVD process, air exposure is not avoidable, which is also the case for many university-type experimental setups. Although oxidized metal (formed during transferring from a metal deposition chamber to PECVD) could assist in the sulfurization [65], the oxidized surface of 2D material (formed when transferring the sample from PECVD to a metal deposition tool) will definitely be harmful to vertical conduction. To address this issue, a new system set up by Dr. Dimitry Zemlyanov at Purdue University is adopted, where different process chambers are clustered so that air exposure can be avoided when transferring a sample. This system includes chambers for 2D materials formation, metal deposition, and XPS analyses. The process flow is illustrated in Fig. 5.4(b). In this new approach, after Ta is deposited with an e-beam evaporator as before, the sample is loaded in the clustered system. Since a sulfur precursor is not available yet in this system, selenization to form $TaSe_2$ is used as a demonstration of 2D materials formation. Dimethyl selenide is adopted as the precursor is for $TaSe_2$ formation. Before the selenization process, Ta surface is sputtered to remove some surface oxides. During the selenization, atomic hydrogen is utilized to further reduce oxides. Note that the growth temperature is higher than the BEOL-compatible temperature since plasma is not available in this system. Nevertheless, it will be demonstrated that this approach can avoid the formation of the surface oxides. If plasma is installed in the future, it is expected the same results can be obtained at a lower temperature.

Before actually depositing metal on the top of $TaSe_2$, XPS analyses is conducted in the same system. In this way, the film property without being oxidized by the ambient can be captured. All the XPS measurements are conducted on the same position of the same sample so that variation can be excluded. As shown in the left panel of Fig. 5.4(c), with adding more growth time and using higher temperature, Se peak becomes more obvious, indicating more Ta has been converted to

$TaSe_2$. More importantly, the oxygen-related peaks shown in the right panel become less significant. This could be attributed the fact that the oxygen sites of the oxidized Ta film to start with have been replaced with Se. As a result, an oxide-free 2D material film is formed. Since the following metal deposition will be performed in the same system, an oxide-free interface between the 2D film and the metal can be expected, which is advantageous for vertical conduction.

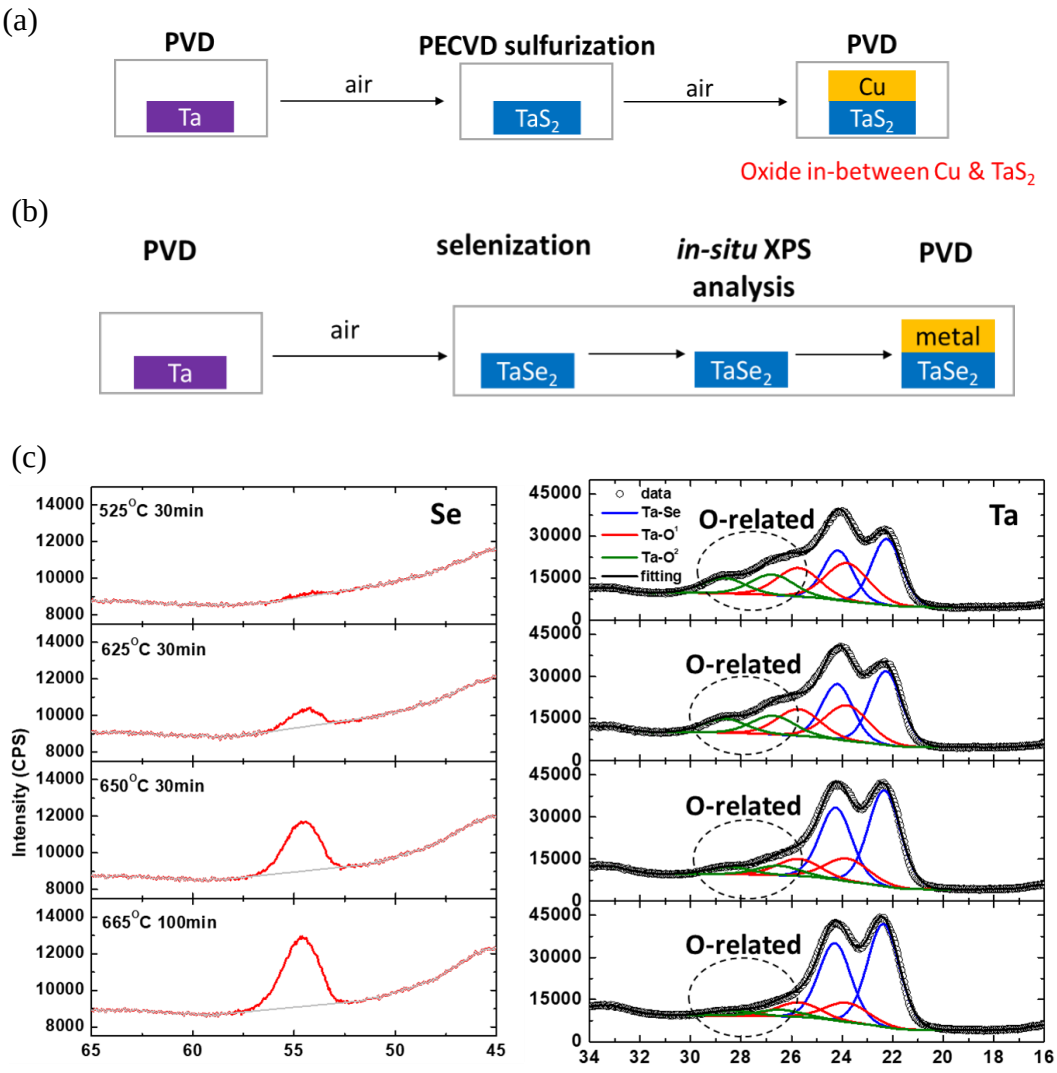


Fig. 5.4 (a) Process flow of the approach using PECVD to sulfurize the pre-deposited Ta. Since sample transferring steps from one chamber to another is required, oxides are formed during air exposure. (b) Process flow of 2D material formation using an *in-situ* system. Since multiple chambers are clustered, air exposure can be avoided. (c) *in-situ* XPS analyses on the selenization process. With longer growth time and higher temperature, more $TaSe_2$ is formed. At the same time, oxygen-related peaks are reduced, indicating an oxide-free interface can be achieved.

5.3.2 *In-situ* Oxide Sputtering before Metal Deposition

In addition to using a clustered system described in previous sub-section, we also want to know whether an oxide-free interface can be realized using our PECVD system, with some post-treatment. Therefore, a metal sputtering system that has the capability of sample surface sputtering using Ar plasma is employed. The process flow is briefly depicted in Fig. 5.5(a). After TaS_x formation by the same PECVD, the sample is loaded into the sputtering system. During the sample transferring, surface oxides are formed on TaS_x. Nevertheless, the *in-situ* Ar sputtering can remove the surface oxides. Finally, a metal layer is deposited on TaS_x and an oxide-free interface is achieved.

To obtain accurate resistance values, the same vertical Kelvin structure shown in Fig. 5.2 is also adopted with a few modifications. First, the bottom electrode now is 60 nm Ti /5 nm Ta for better conducting. The duration of sulfurization is 10 minutes, instead of 5 minutes used previously, to produce a thicker film so that ~2 nm TaS_x can be left after the surface oxide sputtering. Finally, ruthenium (Ru) is used as the top electrode due to the materials choice in the system. Ru is sputtered for 15 minutes with the power of 35 W. The thickness has to be measured. Although the ideal choice of top metal is Cu, Ru would not have obvious impact on the results since the TaS_x is metallic, as confirmed by the linear *I-V* curve shown in Fig. 5.5(c). Figures 5.5 (b) and 5.5 (c) compare the results of this sputtering-treated TaS_x with those from the oxidized TaS_x shown in section 5.2. It can be observed that the vertical resistivity has been reduced by almost two orders of magnitudes. With further removing the oxides and improving the film quality, even better vertical conduction can be expected.

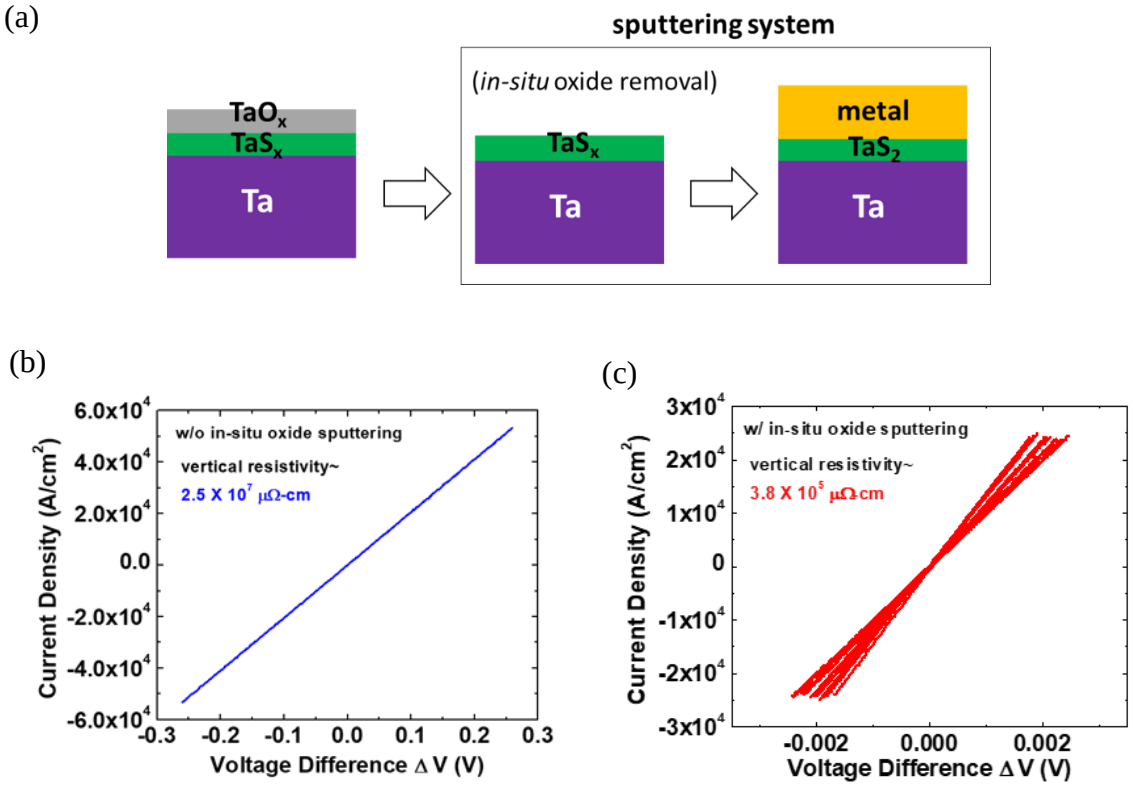


Fig. 5.5 (a) An oxide-free interface achieved by employing a sputtering system to remove surface oxides on the PECVD grown TaS_x. The following metal deposition is performed in the same sputtering chamber. Vertical Kelvin structures are fabricated for accurate resistance measurements. (b) *J-V* characteristics of devices with oxidized PECVD TaS_x. Vertical resistivity is ~2.5×10^7 μΩ-cm. (c) *J-V* characteristics of devices with oxides being sputtered off. Vertical resistivity is ~3.8×10^5, which is significantly lower than that without oxides removal.

5.4 Intrinsic Vertical Conduction of TaS_2

Although surface oxides of TaS_x are detrimental to vertical conduction, whether the targeted performance can be achieved with perfectly oxide-free TaS_x is still unknown. Therefore, the intrinsic vertical conduction must be studied. In addition, an evaluation of the overall performance with an intrinsic material is needed. To understand intrinsic properties and avoid deteriorated characteristics due to imperfect material synthesis at the current stage, we exfoliated TaS_2 films from crystals produced by 2D Semiconductors. We performed electrical measurements on 2H-TaS_2 because of its lower out-of-plain resistivity [98] and potentially lower growth temperatures as opposed to 1T-TaS_2 [36]. Precautions were taken for the test structure design and fabrication, since the vertical conduction can be affected by many subtle imperfections, such as surface oxidation of TaS_2 and electrodes or any process contamination. The device structure is shown in Fig. 5.6(a). A SiO_2 (60 nm) layer was deposited by e-beam evaporator to isolate the top and bottom electrodes. A window was then opened in the SiO_2 layer to guide the current to flow through TaS_2 vertically, followed by the top electrode formation. The choice of the electrodes is critical since both oxidation and poor adhesion could severely affect the vertical conduction. Therefore, bottom electrode is chosen to be Ti/Au (5 nm/25 nm) to avoid oxidation before exfoliating TaS_2 on it. Top electrode is selected to be Ti/Ni (35 nm/70 nm) to have a better adhesion. Note that since 2H-TaS_2 is metallic in the vertical direction [36][102] at room temperature, the choice of metal work function should be less critical on contact resistances. A set of control devices using the identical design but without TaS_2 flakes between the top and bottom electrodes were also fabricated to subtract parasitic resistances. The results from multiple devices in Fig. 5.6(b) show that the vertical resistivity can be as low as ~2000 μΩ-cm.

To estimate the overall via resistance with technology scaling, a semi-empirical model proposed by Ciofi et al. [103] was adopted to calculate Cu resistivity by considering its size effect. Contribution from Ta was first neglected for simplicity, which is a conservative assumption. As demonstrated in Fig. 5.6(d), even with a ~3X higher resistivity of 2H-TaS_2, the contribution from TaS_2 is similar to that from TaN since TaS_2 can be thinner. The resistance contribution from Cu tremendously increases in extremely scaled dimensions because TaN occupies a huge portion. On the contrary, when TaS_2 is used, contribution from Cu is much lower due to the much larger Cu percentage. The significant differences in Cu percentages further lead to pronounced differences

in size effects caused by surface scattering, which make via resistance with TaS_2 as the barrier/liner even smaller. In summary, even with the higher vertical resistivity of TaS_2, replacing TaN/Ta with TaS_2 is still beneficial for via resistance, which further helps reduce the bottleneck of interconnect scaling.

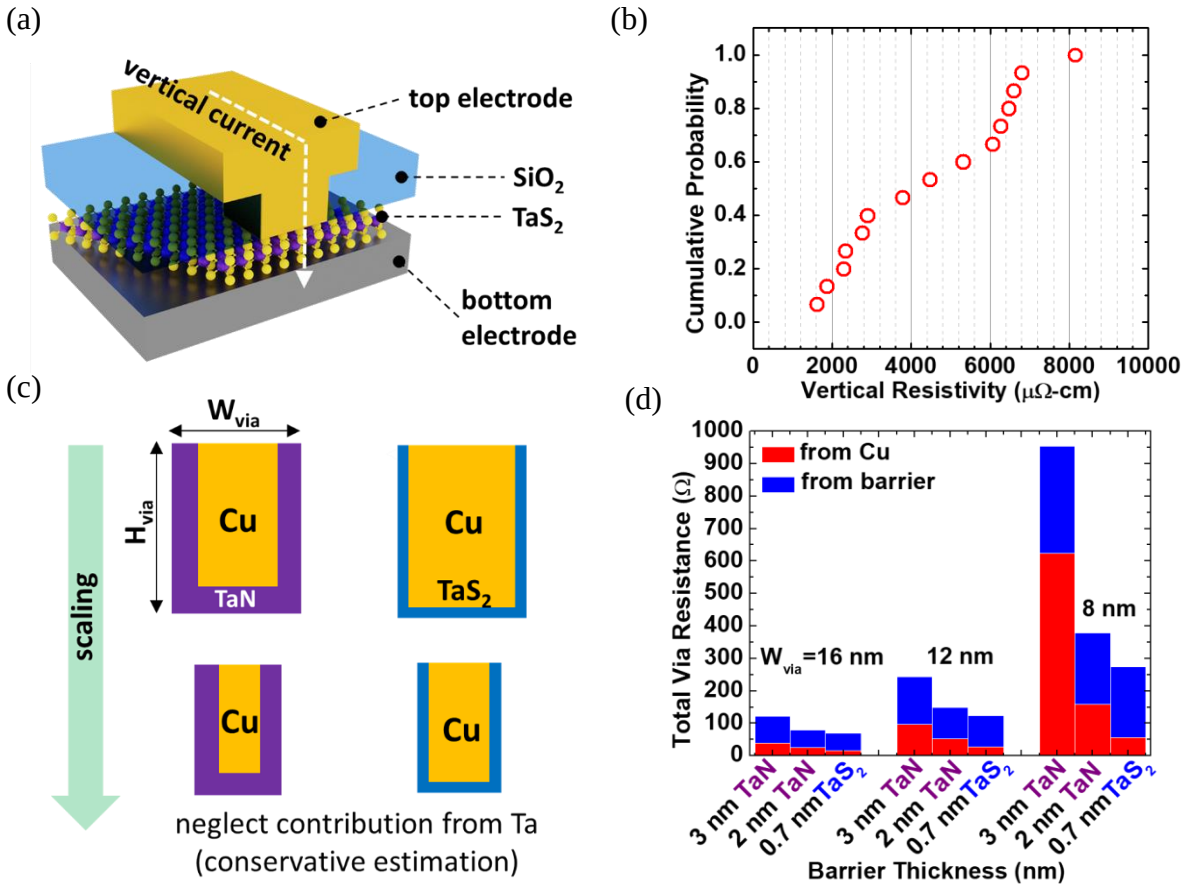


Fig. 5.6 (a) The test device structure to measure vertical resistivity of 2D materials. A SiO_2 layer is adopted as the isolation and to define the area of vertical conduction. (b) Values of vertical resistivity of 2H-TaS_2 from multiple devices. (c) Comparison of via scaling in the cases of using TaN and TaS_2 as the barrier. (d) Comparison of total via resistance using different TaN and TaS_2 barriers. Resistance contributions from Cu segment and barrier are labeled by red and blue color, respectively. Cu resistance escalates as the via is more scaled, which makes a 2D barrier advantageous.

5.5 Conclusion

In this chapter, we have studied the vertical conduction across TaS_x to know its impact on via resistance. Significant oxides are formed on TaS_x during sample transferring, as confirmed by comparing the results from different process flows, which leads to very high vertical resistivity. Two approaches have been explored to realize an oxide-free interface between TaS_x and the metal on its top: (i) *in-situ* XPS analyses performed in a clustered system show oxygen-related peaks are largely reduced with the formation of 2D materials. Followed by the metal deposition that can be performed in the same system, an oxide-free interface can be expected. (ii) By utilizing a metal sputtering system with *in-situ* oxide sputtering capability, the vertical resistivity of the PECVD TaS_x is decreased by two orders of magnitudes. In addition to finding engineering ways to avoid the oxides, the intrinsic property of TaS_2 has also been studied to understand the best-possible performance this material can deliver. The results demonstrate that with further scaling of interconnects, a via using 2D barrier/liner will outperform that using conventional TaN/Ta.

6. OTHER APPLICATIONS AND FUTURE WORKS

6.1 Introduction

We have investigated the potentials of various 2D layered materials in a wide variety of aspects and identify the best candidate and its remaining challenges. In this chapter, other possible interconnect-related applications that could benefit from 2D layered will be proposed and some of the preliminary results will be demonstrated. In addition, future directions will also be suggested. As shown in Fig. 4.2(d) and in [16], [76], by integrating 2D layered materials with Cu nanowires or nanofilms, Cu resistivity can be reduced due to the suppression of surface scattering. The reduced Cu resistivity can lower *RC* delay and enhance computation speed of standard CMOS circuits. In addition to this well-known advantage, we will further apply the capability of reducing resistivity to other applications. For example, the reduced resistivity could bring benefits to radio-frequency (RF) transmission lines. Moreover, as cobalt (Co) interconnects would be adopted in near future, impacts of 2D barrier/liner on Co interconnects are also investigated. In addition to the aspect of interconnect performance, conformal deposition of 2D materials is explored, and the results suggest that more efforts are required to achieve the goal.

6.2 RF Transmission Line

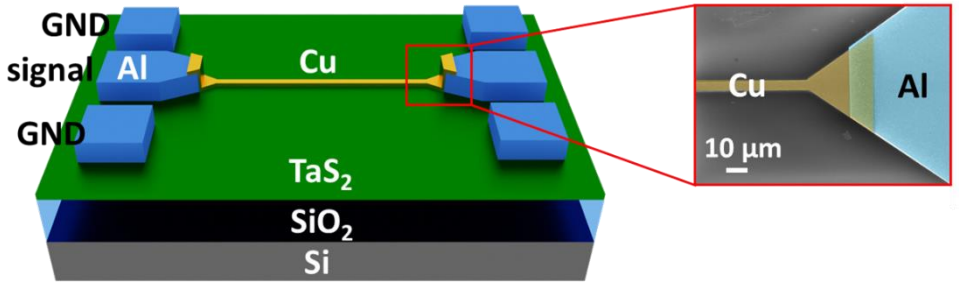
With the emergence of 5G communication and increased interest in millimeter-wave (mm-wave) applications, much effort has been made to increase the maximum frequency of RF circuits and systems. This not only requires active devices with higher cut-off frequencies, but also requires passive components, such as transmission lines, to operate at higher frequencies. At higher frequencies, the RF power loss along typical metal transmission lines can increase drastically, limiting operational bandwidth of the entire circuit. Conventionally, RF transmission lines are designed on the top layers of interconnects since thicker and wider transmission lines exhibit lower

power losses [104]. Recently, with the increased interest in the monolithic integration of mm-wave capabilities with CMOS technology, high bandwidth transmission lines with dimensions in the range of tens of nanometers are required, to be comparable to the dimensions of low level interconnects in standard CMOS structures [105], [106]. This highlights the need for RF "nano-transmission" lines in the recent years [107]–[110], explored here using 2D layered materials.
The reason of integrating 2D layered materials with RF transmission lines lies in the fact that 2D materials can reduce inelastic surface/interface scattering of Cu wires and hence reduce Cu resistivity, as discussed in Chapter 4. Reducing the line resistance directly translates to reduction of transmission line power loss.

Here, we used our PECVD grown, large area TaS_x films for initial prototype testing. The structure of the transmission line is shown in Fig. 6.1(a). 2-nm TaS_x was first deposited on top of 1.5-µm SiO_2. Thick SiO_2 was selected to minimize the electrical feedthrough in the Si substrate during RF measurement. A 500-nm Al layer was then deposited and patterned to form electrodes for probing. Finally, 15-nm-thick/5-µm-wide Cu transmission line was deposited and patterned to connect the two Al electrodes. Such a thin Cu layer was chosen to enlarge surface/interface scattering, as discussed in Chapter 4. In addition to the transmission line structure, "open" and "short" structures were also fabricated for the de-embedding process. "Open" structures have no Cu line between the two Al electrodes, while "short" structures connect Al signal pads directly to adjacent ground (GND) pads. RF characterization was performed using a standard two-port S-parameter measurement, with RF input power being set at -10 dBm. The measured information from the "open" and "short" features were used to de-embed the parasitic capacitance and inductance from the metal electrodes and electrical routing. Thus, the results after the de-embedding procedure reflect the behavior of the isolated Cu transmission line. Note that the conduction through TaS_x film is negligible here since the resistivity of TaS_x (~10^7 µΩ-cm) is orders of magnitude higher than Cu (~10 µΩ-cm with this dimension). The measured results of different devices with and without TaS_x are shown in Fig. 6.1(b). It can be clearly observed that with the presence of TaS_x, the power loss of transmission lines is reduced, even when taking the device-to-device variation originated from the fabrication into account. The reduction of power loss is attributed to the reduction in Cu resistivity. In the DC regime, as shown in Fig. 4.2(d), the reduction in Cu resistivity is around 10%, while an average reduction of around 2% is obtained in the RF regime. Further

power loss reduction can be achieved through quality improvement of the 2D films since we have observed a much larger resistivity reduction (~46%) by using exfoliated, high quality MoS_2 films (Table 4.1) [76]. Nevertheless, our results provide the initial validation that the benefits of 2D materials in the DC regime to reduce Cu resistivity can be translated to the RF regime to mitigate power loss.

(a)



(b)

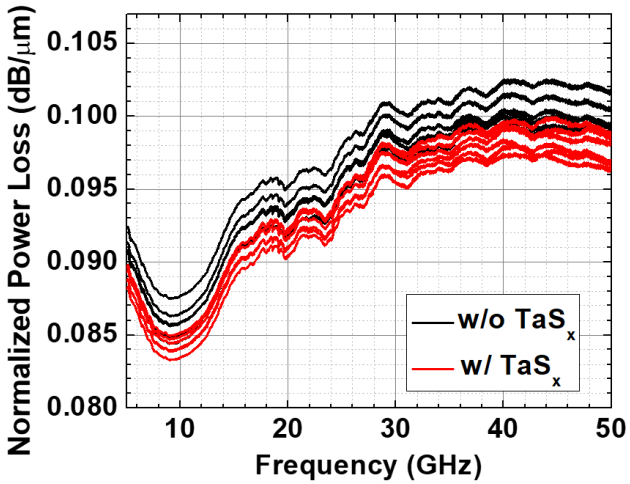


Fig. 6.1 (a) Device structure for RF transmission line measurements. Thicker Al is first deposited as the electrodes. Thin (to enlarge surface/interface scattering) Cu transmission line is then deposited. "Open" structure with no Cu line in-between two Al signals lines and "short" structure with two Al signal lines directly connected are also fabricated for the de-embedding process. (b) Normalized RF power loss of devices with and without TaS_x. It is shown that TaS_x can reduce the power loss, which can be attributed to the reduction of Cu resistivity/resistance.

6.3 Cobalt Interconnects with TaS_x Barrier/Liner

Cobalt (Co) and ruthenium (Ru) have been extensively investigated in the past few years as the replacement of Cu. Their promises lie in the possibility to be barrier-free, lower resistivity compared to Cu in extremely scaled dimensions due to shorter mean free path [111]–[114], and superior electromigration lifetime [115]–[117]. Even without the need of a diffusion barrier, an adhesion layer, in analogy to the liner for Cu, is generally required [111]. Therefore, the surface/interface scattering between ultra-scaled Co or Ru and their adhesion layers could play a critical role in their resistivities [118], as discussed in Chapter 4. In addition, despite the early presumption that a barrier would not be necessary, Co and Ru have been found to diffuse into dielectrics under certain conditions [119], [120]. Here, PECVD TaS_x grown at 400 ℃ was tested to explore whether the benefits for Cu interconnects in terms of blocking diffusion and scattering reduction also apply to Co interconnects. Figure 6.2(a) shows the test results of Co diffusion using the capacitor structure described in earlier chapters. It can be observed that with TaS_x in-between Co and SiO_2, t_{BD} of devices increases in general, indicating the suppression of Co diffusion. In addition, when thin Co (~12 nm) is patterned in the Kelvin structure and is deposited on TaS_x, it is found in Fig. 6.2(b) that Co resistivity is reduced, indicating a more elastic surface/interface scattering facilitated by TaS_x. In short, TaS_x provides desired barrier and liner properties for Co interconnects, which might be useful for future interconnect technologies.

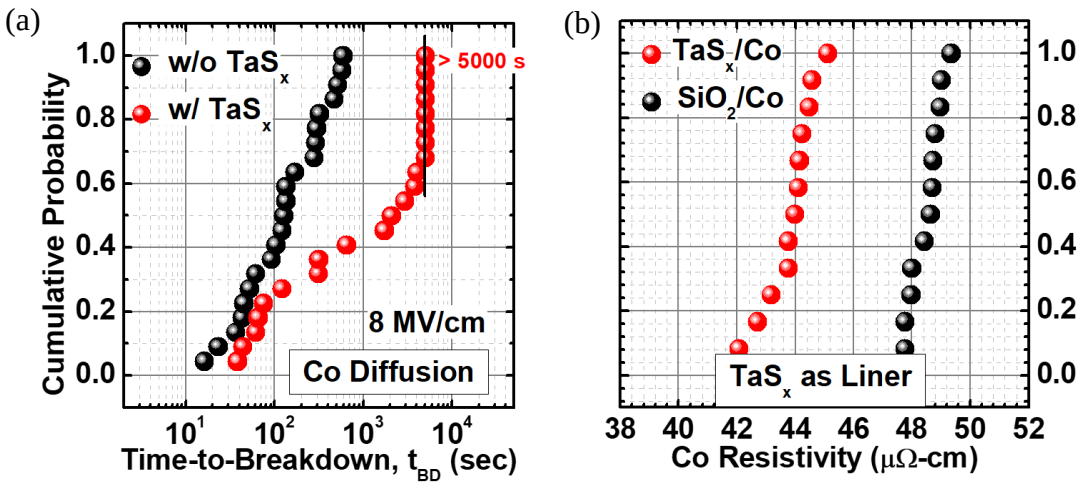


Fig. 6.2. (a) TDDB measurements for Co diffusion. Devices with TaS_x barriers have longer t_{BD}, indicating the suppression of Co diffusion. (b) When TaS_x is used as the liner for Co interconnects, Co resistivity decreases, which is attributed to the mitigation of inelastic surface/interface scattering.

6.4 Deposition of 2D materials in Trench Structure

Even with the numerous advantages of using 2D layered materials as the barrier and/or the liner for interconnects of many kinds, these novel materials can only be integrated if conformal deposition along the Damascene trench structure can be accomplished. In principle, two methodologies have been utilized. In the MoS_2 work of Martella et al., ALD MoO_x layers were first deposited, followed by sulfurization [121]; whereas Jin et al. directly deposited MoS_2 and WS_2 using MOCVD [122]. Here, we also demonstrate direct deposition of MoS_2 in trench structures using thermal CVD at high temperature (just to explore the conformability), as shown in Fig. 6.3(a). Thick films are deposited for preliminary investigations with the focus on conformability at some critical positions in the trench. It is found that trench edges and sidewalls are much harder to cover compared to the2 bottom surface. Note that none of the works mentioned above is BEOL-compatible up to date. Therefore, lower growth temperatures, more conformal deposition, and thinner films are the goals to achieve for trench deposition. Since conformal deposition of Ta (and TaN) has already been developed by the industry, we believe that converting pre-deposited TaN or Ta into uniform TaS_x in the trench through the PECVD sulfurization process discussed in Chapter 4 is potentially feasible, as illustrated in Fig. 6.3(b). Besides, ALD methods that can directly form conformal 2D layered materials is also preferred [123]. However, in both of

the approaches, grain size would be limited due to the nature of PVD-metals (Ta in this case) and ALD films. As discussed in Chapter 3, small grain size results in more Cu diffusion since there are more grain boundaries to facilitate the event. Nevertheless, achieving single-layer 2D materials with large grain size is fundamentally possible due to the material nature. On the other hand, TaN/Ta would already be discontinued at the same atomic thickness due to their 3D natures. Therefore, future efforts have to be made in developing single-layer and high-quality 2D barriers/liners conformally deposited in trench structures.

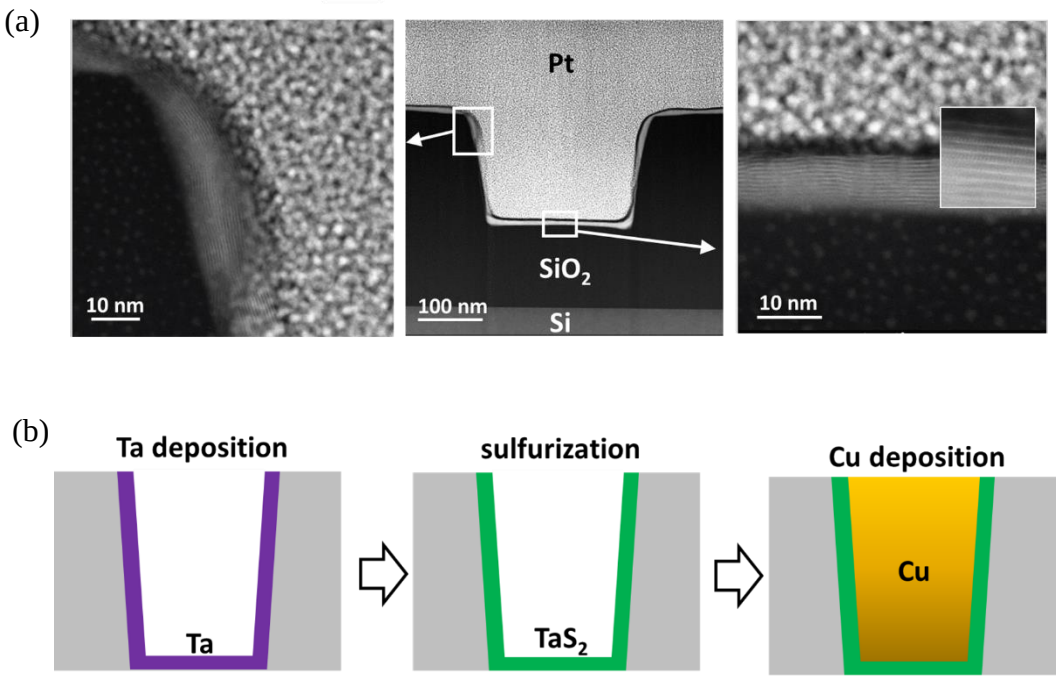


Fig. 6.3. (a) Deposition of MoS_2 along a trench structure using thermal-CVD. Layered structures can be observed. However, conformity still needs to be improved. More conformal and thinner 2D films deposited at a BEOL-compatible temperature is the goal to pursue. (b) Proposed method for a BEOL-compatible TaS_x deposited in the trench. Since conformal deposition of Ta (and TaN) has been well developed by the industry, a conformal TaS_x could be realized by sulfurizing the Ta (or TaN) film using the BEOL-compatible PECVD process described in Chapter 4.

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VITA

Chun-Li Lo was born in Kaohsiung, Taiwan in 1989. He received both BS and MS in Electronics Engineering from National Chiao-Tung University, Taiwan in 2011 and 2013, respectively. His master's thesis mainly focused on the device-circuit interaction of Resistive-Switching Random Access Memories (RRAM). He joined Purdue University in January 2016 and pursued his Ph.D. degree in the School of Electrical and Computer Engineering. His Ph.D. thesis focused on the applications of two-dimensional materials for advanced interconnect technologies. He has discovered and developed the first two-dimensional materials, namely tantalum disulfide, that meets the critical requirements of interconnect technology integration. He was hired as a consultant by Taiwan Semiconductor Manufacturing Company (TSMC) in 2019. In his leisure time, he enjoys immersing himself in the cultures of cocktails and Jazz music.

PUBLICATIONS

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