4H-SIC VERTICAL TRI-GATE POWER MOSFETS TECHNOLOGY DEVELOPMENT

by

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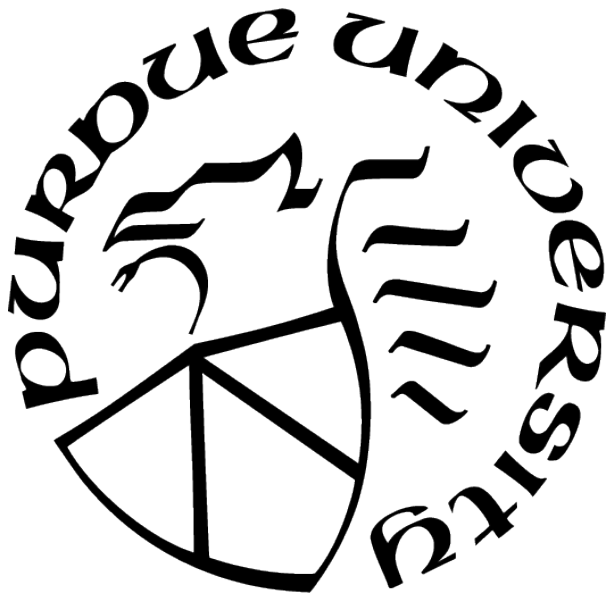

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To The Almighty God

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Advances in power electronic systems, especially those in hybrid and electric automobiles and renewable power generation systems, demand high blocking voltage, fast switching performance and low thermal budget from power semiconductor devices. State-of-the–art, silicon based power semiconductor devices are limited by material properties in meeting these demands. Due to the relatively low critical electric field, the on-resistance of the devices is high, and increases significantly with blocking voltage. As a result, current silicon (Si) power MOSFETs rated at above 600 V suffer from unacceptably high conduction losses. Innovative designs, such as the insulated gate bipolar transistor (IGBT), have been developed which use conductivity modulation through the injection of minority carriers to reduce on-resistance. But the involvement of minority carriers gives rise to stored charge and a turn-off delay, dramatically increasing switching losses compared to unipolar devices. Silicon carbide (SiC), a wide band gap semiconductor provides an alternative to Si, and offers a 7x higher electric field strength, 2x higher saturation velocity, and 3x higher thermal conductivity. A thinner, more heavily doped drift region is required for a SiC power device for a particular voltage, which reduces on-resistance and power consumption. However, the channel resistance of SiC metal oxide semiconductor field effect transistors (MOSFETs) is high due to the poor quality of the dielectric-semiconductor interface. Thus the SiC MOSFET fails to live up to the full promise of the material. Minimization of the channel resistance is essential, especially for applications requiring blocking voltages under 1 kV, where this component dominates others. In this work, a novel tri-gate SiC MOSFET is proposed to address this issue. This new structure utilizes both the conventional horizontal surface as well as the sidewalls of a trench to increase the effective width of the channel without increasing the device area. With proper optimization, it should be possible to achieve 3x lower specific on-resistance compared to current SiC unipolar power devices.

1. INTRODUCTION

Silicon – the element which has had perhaps the most widespread impact on the human race in the last century – when combined with the ubiquitous element carbon, gives rise to an intriguing compound material, silicon carbide (SiC). It is a wide band gap semiconductor, and offers the potential of high performance, high efficiency power electronic devices with robust thermal stability. While state-of-the-art silicon power devices are reaching their theoretical limits of performance [1], SiC has its own material and technological constraints which will be addressed, and a proposal will be made to meet these challenges.

This thesis has been organized into six chapters. A brief introduction to power electronics and the motivation to use SiC in fabricating power devices will be presented in this chapter. Progress and challenges in SiC power semiconductor devices, along with a proposal for improving device performance will be provided in chapter 2. The mask layout and design architecture of the proposed novel device is described in chapter 3, and in chapter 4, the detailed fabrication and processing steps to build the device are discussed. The device characterization is discussed in chapter 5, and finally in chapter 6, the future work will be suggested and conclusions will be drawn.

1.1 Power Semiconductor Devices

In general, power electronics is a field which involves electrical energy flow regulation and conversion using power semiconductor devices. The concept is so integrated in our day-to-day life, from comfort to necessity, that it is often taken for granted. Imagine the cell phone – almost everyone carries one in his pocket. It is operated by a battery where electrical energy is added and managed by chargers and regulators. The omnipresence of power electronics is reflected from the data presented by International Energy Agency (IEA) in 2014, where it says that electricity comprises 20% of the total energy consumed on this planet, and is the second highest after oil related power consumption at 40% [2].

The building block of such electronics is the power semiconductor device. The continuous progress and development of these devices is not just a luxury, but a requirement for ever growing technology. Since the early days, after discovering the semiconductor p-n junction

operating principle in 1940, silicon has been the material of choice in the fabrication of these devices, based on its performance, availability and cost. It opened the door for the electronic revolution which we are still harnessing. Even now, power semiconductor devices are dominated by silicon. But unfortunately, nothing is indestructible, and so neither is the element - silicon. The demand in technology is pushing to a regime where the material is reaching its theoretical limits. The need of high blocking voltage applications, superior switching performance, and robustness in operation make wide band gap semiconductors a viable alternative to silicon. Among the wide band gap semiconductors, the most popular for power devices are – silicon carbide (SiC), gallium nitride (GaN), diamond (a crystalline form of carbon), and gallium oxide (GaO). Silicon carbide currently presents the best opportunity due to recent advances in high quality wafer growth and process technology [3].

1.2 Silicon Carbide

Silicon carbide (SiC) process technology is by far the most mature among the other wide band gap alternatives, and is now beginning to dislodge Si as the preferred semiconductor for power electronics, with the inevitable increase in demand for higher blocking voltages, superior switching performance, better efficiency and reliability. This compound semiconductor, formed in a stoichiometry of equal Si and C, holds many virtues to be the perfect candidate for future power electronics. Some of these inherent physical properties are discussed below, followed by a review of the SiC crystal structure.

SiC is well known for polytypism, the ability to grow the material in different crystallographic configurations, without changing the chemical composition. Polytypes are generally subdivided into two broad groups based on the arrangement of the constituent atoms in the unit cell: β-SiC and α-SiC. β-SiC is cubic in atomic arrangement while any other arrangements belong to α-SiC group. One of the most popular polytypes of SiC is 4H-SiC, which is a hexagonal close-packed system in which four Si-C bilayers form the a unit cell along the c-axis. SiC is normally grown by sublimation in a physical vapor transport (PVT) technique at 2000-2800°C [4].

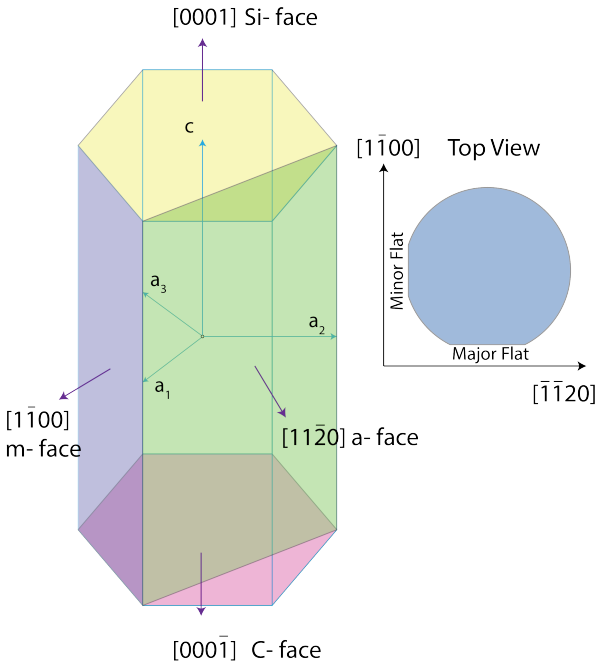


Figure 1.1. Hexagonal unit cell in 4H-SiC with important faces highlighted. Typical SiC wafer orientation is also shown

Growth of 4H-SiC during sublimation is controlled by creating a C rich environment with the necessary dopant impurity at 2280°C and 10 Pa pressure [5]. The important faces of the 4H-SiC hexagonal structure is shown in Fig. 1.1. The usual wafer orientation of [0001] Si face is also shown in the figure.

The bandgap of SiC is in the range of 2.36–3.8 eV, depending on the polytype. The most common polytype of SiC for electronic purposes is 4H, mainly because of its high electron and hole bulk mobility, and less mobility anisotropy in different crystallographic directions [4]. This polytype of SiC exhibits a bandgap of 3.26 eV, and the saturation velocity of 4H-SiC at room temperature is 2×10^7 cm/s [6], which is almost twice than in Si material. This property is very attractive for high frequency electronic applications. However, for power electronics, the two most important properties this compound material offers is high critical electric field and high thermal conductivity. These useful properties are discussed separately in the following subsections.

1.2.1 Critical Electric Field

In power semiconductors, the off-state voltage supported by the device is ultimately limited by avalanche breakdown. Mobile carriers, accelerated by the high electric field generated by the applied voltage, can collide with atoms while passing through the drift region. Such collisions may promote electrons from the valence band to the conduction band, generating new electron-hole pairs. These new carriers are again accelerated by the field, and can further collide with other atoms and ionize them as well, in a cascade of such events. Generation of electron-hole pairs in this way is called impact ionization. Under this condition, significant current flows through the device, and catastrophic damage may occur if allowed to continue indefinitely. This avalanche process is described by the impact ionization coefficients for electrons and holes, represented as α_n and α_p, respectively. These basic material properties are strong functions of the local electric field, and represent the number of electron-hole pairs generated by a carrier as it traverses a unit distance. If electron-hole pairs are generated at certain distance x from the edge of the depletion region in an abrupt P^+-N junction, the electron will be swept through the depletion region to the N side, while the hole will traverse to the P^+ side, as shown in Fig. 1.2.

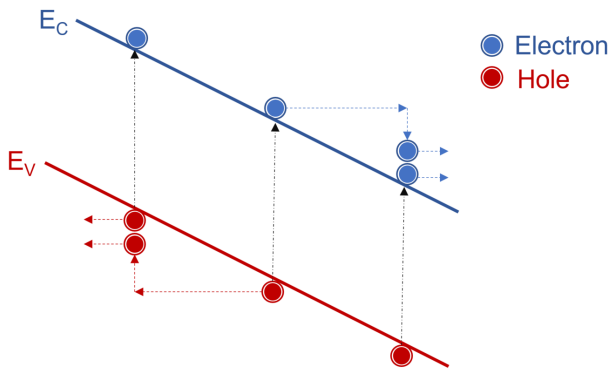


Figure 1.2. Impact ionization at a high electric field showing an energetic electron creating a electron-hole pair

A generated electron or hole will generate α_n or α_p additional electron-hole pairs, respectively, while traversing a unit distance. So the total number of electron-hole pairs that

will be generated by a specific electron traversing dx distance would be $\alpha_n dx$ and the total electron-hole pairs that will be generated by a specific hole traversing dx distance would be $\alpha_p dx$. Additionally generated electron-hole pairs will participate in further impact ionization events, and the total number of electron-hole pairs due to the generation of one electron-hole pair at distance x from the junction can thus be expressed as

$$M(x) = 1 + \int_0^x \alpha_n M(x')dx' + \int_x^W \alpha_p M(x')dx' \tag{1.1}$$

The solution of this expression can be written as - $M(x) = M(0)\exp\left[\int_0^x (\alpha_n - \alpha_p)dx'\right]$

Where M(0) is the total number of electron-hole pair generated at the edge of the depletion region (x=0).

$$M(0) = \frac{1}{1 - \int_0^W \alpha_p \exp\left[\int_0^x (\alpha_n - \alpha_p)dx'\right] dx'} \tag{1.2}$$

Substituting the expression for $M(0)$ into the solution gives the following expression for $M(x)$-

$$M(x) = \frac{\exp\left[\int_0^x (\alpha_n - \alpha_p)dx'\right]}{1 - \int_0^W \alpha_p \exp\left[\int_0^x (\alpha_n - \alpha_p)dx'\right] dx'} \tag{1.3}$$

At avalanche breakdown, defined as the generation of an infinite number of electron-hole pairs, the denominator of the Equation 1.3 becomes 0, which occurs when the following integral is equal to 1.

$$\int_0^W \alpha_p \exp\left[\int_0^x (\alpha_n - \alpha_p)dx'\right] dx' = 1 \tag{1.4}$$

This integral is called the ionization integral for holes, and when combined with a proper impact ionization model for a particular material, it is used in a device simulation to numerically find the critical electric field which results in avalanche breakdown.

In general, for a particular electric field, the α_n and α_p for SiC are very small compared to Si. These coefficients can be expressed as [7]

$$\alpha_{n.SiC} = 1.69 \times 10^6 \exp\left(\frac{-9.69 \times 10^6}{E}\right) \tag{1.5}$$

$$\alpha_{p.SiC} = 3.32 \times 10^6 \exp\left(\frac{-1.07 \times 10^7}{E}\right) \tag{1.6}$$

On the other hand same parameters for Si at room temperature can be expressed as [8]

$$\alpha_{n.Si} = 0.426\, E \exp\left(\frac{-4.81 \times 10^5}{E}\right)^2 \tag{1.7}$$

$$\alpha_{p.Si} = 0.243\, E\, \mathrm{e}\left(\frac{-6.53 \times 10^5}{E}\right)^2 \tag{1.8}$$

Here the unit of E is in V/cm and the unit of coefficients are in 1/cm.

The impact ionization coefficients for both SiC and Si are plotted in Fig. 1.3.

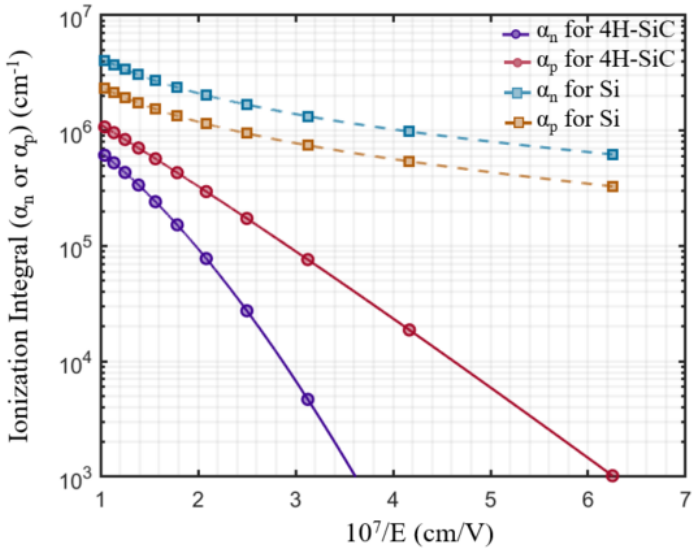


Figure 1.3. Comparison of the impact ionization coefficients for SiC and Si as a function of inverse electric field, based on equations 1.5 - 1.8

At a certain electric field, known as the critical electric field, the value of theses coefficients are such that the ionization integral approaches 1 (see Equation 1.4). At the onset of this situation, a huge number of electron-hole pairs are generated and material breaks down.

Strictly speaking, the critical electric field should be calculated numerically for each specific device structure. However, the critical electric field of SiC and Si at room temperature can be approximated by the following expressions [7]–

$$E_{CR.SiC} = \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log_{10}(N/10^{16})} \tag{1.9}$$

$$E_{CR.Si} = \frac{4 \times 10^5}{1 - \frac{1}{3}\log_{10}(N/10^{16})} \tag{1.10}$$

These equations, plotted in Fig. 1.4, are valid for a simple planar, constant doping structure, but are reasonable approximations for other more complex structures as well. It can be easily seen from this figure that the critical electric field of SiC is up to 7x more than Si.

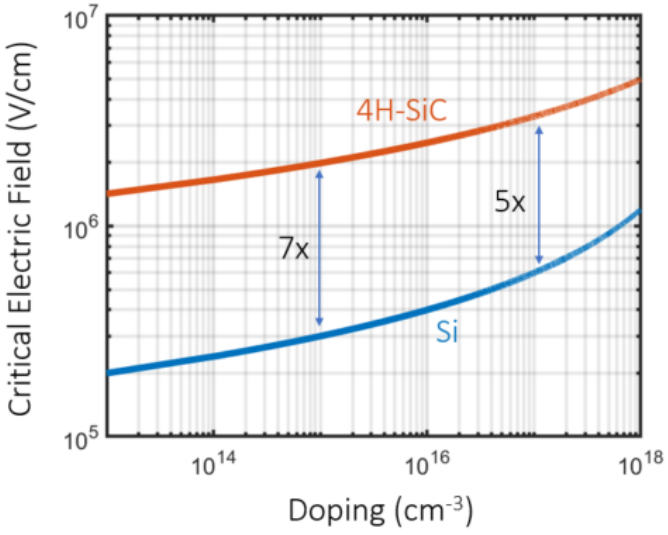


Figure 1.4. Critical electric field of SiC and Si as a function of doping

The higher dielectric strength of SiC directly provides an advantage in achieving high blocking voltages. As shown in Fig. 1.5 for a non-punch-through case, the electric field profile is a triangle. At the blocking voltage, the maximum field will be equal to critical electric field, E_C, and the voltage can be expressed as the area under the triangle (neglecting the voltage drop in the heavily doped $P+$ region) –

$$V_B = \frac{1}{2} E_C x_{db} \tag{1.11}$$

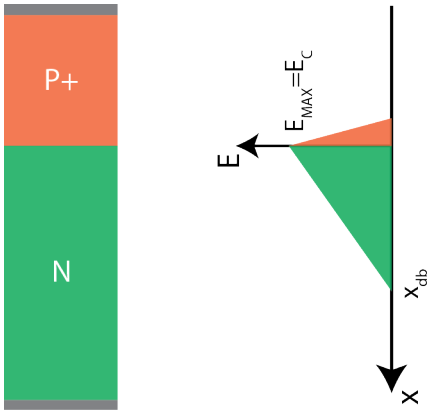


Figure 1.5. Abrupt P^+-N diode and the electric field profile at blocking voltage in non punch through case

The depletion depth in the N region of permittivity ϵ_S and doping N_D, under blocking voltage V_B, can be written as –

$$x_{db} = \sqrt{\frac{2\epsilon_s V_B}{qN_D}} \tag{1.12}$$

where q is the charge on an electron. Substituting this expression for x_{db} in Equation 1.11, the blocking voltage becomes –

$$V_B = \frac{\epsilon_S E_C^2}{2qN_D} \tag{1.13}$$

As shown in Equation 1.13, blocking voltage is proportional to the square of the critical electric field. Therefore, since the critical field is $\approx 7\times$ higher in SiC than in Si, $50\times$ higher blocking voltage is achievable for a given doping level. Alternatively, to obtaining a certain blocking voltage, SiC can be doped much more heavily than Si, and the drift region can be made much thinner, resulting in significantly reduced on-resistance.

The specific on resistance (defined as the product of resistance and area) of a uniformly doped block of material, can be written as -

$$R_{ON.SP} = \rho x_{db} = \frac{x_{db}}{q\mu_N N_D} \tag{1.14}$$

where μ_N is the electron mobility, and full dopant ionization has been assumed. Substituting (1.11) for x_{db}, and N_D from (1.13) into (1.14), we arrive at an expression for specific on-resistance–

$$R_{ON.SP} = \frac{4V_B^2}{\mu_N \epsilon_S E_C^3} \tag{1.15}$$

The specific on-resistance of a device is therefore a strong function of critical electric field. This fact gives SiC a clear advantage over Si: Due to the 7× higher critical electric field, it offers about 300× less resistance for the same blocking voltage.

1.2.2 High Temperature Operation and Thermal Conductivity

The intrinsic carrier concentration is a very sensitive function of temperature. In the case of Si, at about 300°C, this becomes comparable to the semiconductor doping. In this intrinsic state, the device looses its ability to function as intended, imposing a fundamental limit to the temperature of a device while in use. For example, in modern automobile exhaust sensing and control, the ambient temperature exceeds 600 °C. Silicon devices are thus prevented from use in this type of application, due to fundamental material properties.

On the other hand, 4H-SiC, having 3x higher bandgap than Si, offers very low intrinsic carrier concentration. At room temperature this parameter is around 5×10^{-9} cm^{-3} [4], which is 10^{19} times lower than Si. As a result, SiC based devices are functional at high temperatures —like 600 °C or even above.

High density power operation and internal power losses cause heat dissipation in the device. For maintaining reliable operation, a complex air or water based cooling system is needed to control the junction temperature. This carries an extra weight to the system and becomes an overhead which may affect the system cost and reliability. Therefore a material like SiC is very attractive, offering high thermal conductivity and thus low thermal resistance, which ensures efficient heat dissipation and reduces—or in some cases eliminates completely—the size and weight of complex cooling system. However, due to gate oxide reliability concerns, MOS-based devices are normally limited to temperatures below 200°C. On the other hand, JFET-based structures which do not rely on gate oxides are able to sustain extended operation above 400 °C [9].

A comparison chart of different power semiconductor materials is shown below -

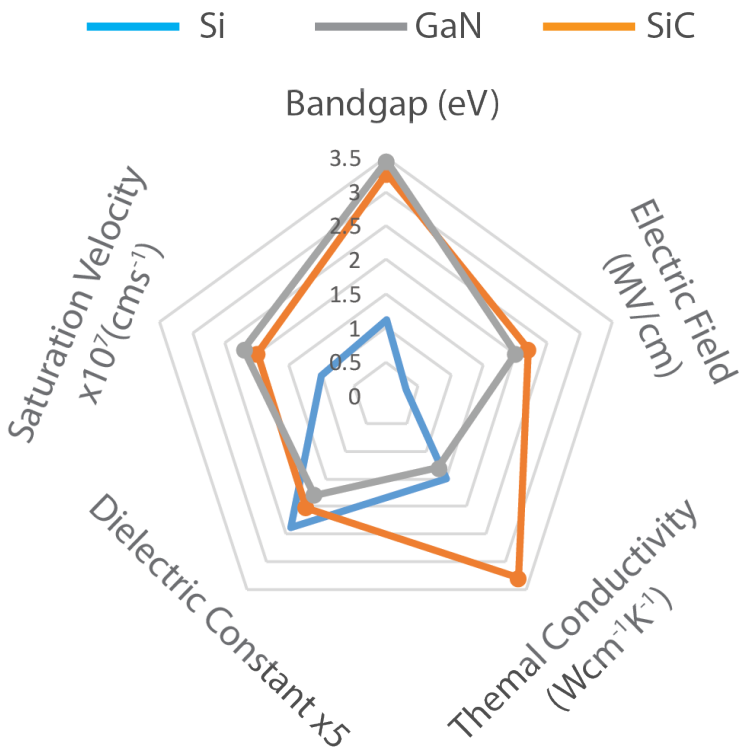


Figure 1.6. Radar graph of selected material parameters of Si, SiC and GaN

2. A NOVEL APPROACH TO SIC POWER SWITCHING DEVICES - THE TRI-GATE MOSFET

2.1 Silicon Carbide MOSFET Applications

Silicon Carbide (SiC) power devices, which have evolved gradually over last 20 years, are now at a stage to shape the power semiconductor industry. The exhibition of high electric field operation, low on-resistance and better thermal transport holds significant promise for the next generation of power semiconductor devices - the second revolution after silicon (Si) [10]. The first SiC power device, a Schottky diode rated at 600 V and 6 A, was introduced to the market by Infineon in 2001, and targeted the automobile industry and power factor correction (PFC) circuitry [11]. Today Wolfspeed fabricates 6 inch diameter SiC wafers with no micropipes (a formerly common yield limiting defect) per square centimeter.

Rohm offers a 2^{nd} generation 650 V and 1200 V planar SiC DMOSFETs, and a 3^{rd} generation trench UMOSFET with similar voltage ratings. The potential applications of such devices are widespread, from the high voltage smart grid to home appliances. SiC devices are now gaining popularity as an alternative to Si counterparts. Due to the higher critical electric field, SiC MOSFETs offer 5–7× lower specific on-resistance compared to Si MOSFETs. However, the Si IGBT, which uses conductivity modulation, can achieve significantly reduced on-resistance in this voltage range. However, the Si IGBT is a bipolar device, while the MOSFET is a unipolar device, which means it does not exhibit the slow minority carrier recombination process during transitions to the off state, and thus has lower switching losses compared to the IGBT. Thus, the unipolar SiC MOSFET enables higher switching frequencies and lower dynamic losses than Si-IGBTs.

A recent trend in power technology is the move toward to greener options, meaning more environmentally friendly technologies and reduced CO_2 emissions. One example is the development of electric or hybrid vehicles in the automobile industry. Toyota manufactures around two million hybrid or electric vehicles a year, promoting the stand against the greenhouse effect and global warming. These vehicles operate at a drive voltage of 600 V, which requires switching transistors rated at 1200 V where SiC MOSFET devices are superior to state-of-the-art Si devices. Better thermal transport, in addition to superior efficiency and

performance, is inherent in SiC devices, which can operate efficiently at as high as 200°C, while Si devices fail below 150°C [12]. This helps to eliminate or reduce cooling mechanisms needed for power devices in harsh environments. This is one of the key features taken into account while using these devices in large data centers with a 380 V distribution scheme, rated at 1200 V [13].

SiC MOSFET devices can also be utilized to design inverters or converters for industrial motor applications and renewable energy generation systems. For example, inverters can be used to convert the DC voltage produced by a photovoltaic array to match the requirements of the synchronous AC grid system. A recent trend in the solar industry is to move toward the higher power ratings and higher system voltages to minimize the cost of inverters and wiring. This then requires power devices with increased voltage ratings. SiC power devices used in the inverter of a photovoltaic system increase the efficiency of the inverter to 97.5%, and reduce inverter losses by 22% compared to Si based devices [12].

The faster switching frequency of SiC MOSFETs can be exploited in the implementation of the smart grid system[14]. This vision of a next generation power grid includes distributed generation sources, and provides for communication between sources to build a resilient and flexible power network [15]. The communication must be done digitally with high bandwidth bidirectional power converters where the associated circuit breakers should act rapidly as per the information - the criteria that can be easily and efficiently met with SiC devices. SiC MOSFET devices, rated at 10 kV, provide the compactness and speed that the smart power grid system demands.

There are many other areas where SiC-based MOSFET devices could be beneficial, including military applications such as electric ships and aircraft, and electric or hybrid combat vehicles [12]. Other possibilities include AC motor controls [16], servo controls, and uninterrupted power supplies, etc. In summary, SiC devices have widespread potential applications, driven by the demand of low power consumption and high voltage operation. Realizing this potential requires significant investment in research and development in both academic and industrial segments.

2.2 SiC MOSFET Status and Prospects

Despite the promise of the SiC MOSFET, it has yet to meet its full potential. For an instance, the poor quality dielectric interface degrades the electron mobility an order of magnitude in the channel compared to the bulk, resulting in higher static loss than desirable. Despite this, the SiC MOSFET already surpasses the performance and efficiency of existing Si power devices for many applications, especially in high voltage applications where device performance is mainly limited by the bulk material resistance, and where the interfacial mobility plays little role. This provides strong motivation to further improve SiC MOSFETs at low to moderate voltage (600-1200 V) applications. In order to do so, it is imperative to address the limitations and current challenges. These key challenges are discussed in the next subsections, followed by a description of the approach adopted in this thesis for device improvement.

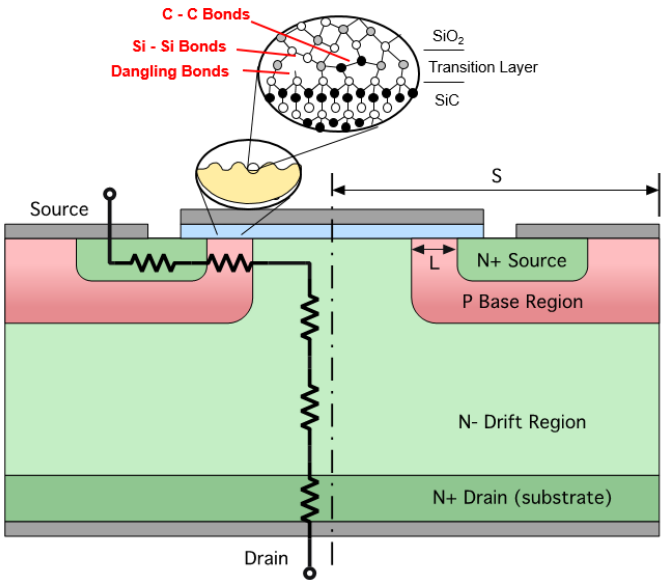
2.2.1 Dielectric Interface

One major advantage of SiC over other wide band gap semiconductors is that it can be oxidized to grow a dielectric at the surface. Thermal oxidation at 1100°C to 1300°C, produces a high quality silicon dioxide (SiO_2) thin film, when combined with an appropriate passivation technique [4]. The basic reaction which takes place during thermal oxidation can be expressed as-

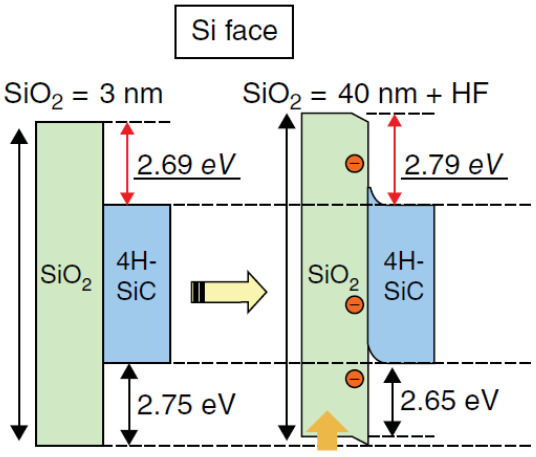
$$SiC + \tfrac{3}{2}O_2 \rightarrow SiO_2 + CO$$

Under the proper conditions, SiC is consumed to grow SiO_2, with carbon (C) diffusing from the structure mainly in the form of carbon monoxide (CO). Of the resulting oxide thickness, 46% is below the original surface, while 54% is above. While the oxidation reaction appears simple at the macroscopic level, at the atomic level the interfacial reaction is far more rich and complex. The process is not yet fully understood, and remains an active area of research. The best mobility recorded in SiC devices, as of today is around 100 $cm^2/(V \cdot s)$ in the channel [17], which is a factor of 10 less than in the bulk (around 1000 $cm^2/(V \cdot s)$).

One theory is that some carbon remains in the near interface region, potentially degrading the oxide-semiconductor interface quality. Experimental work has been done to prove this theory by intentionally inducing conditions which result in reduced out gassing of carbon from the interface, resulting in higher trap density [18]. Another theory suggests higher surface density of atoms in SiC, is the source of high density dangling bonds at the interface[19]. In yet another example, oxidation of the compound semiconductor may lead additional phases. One or more of these factors, none fully proven, might contribute to a poor quality SiC/SiO_2 interface. Dangling bonds and excess C at the interface has been illustrated in the Fig. 2.1(a).



(a)



(b)

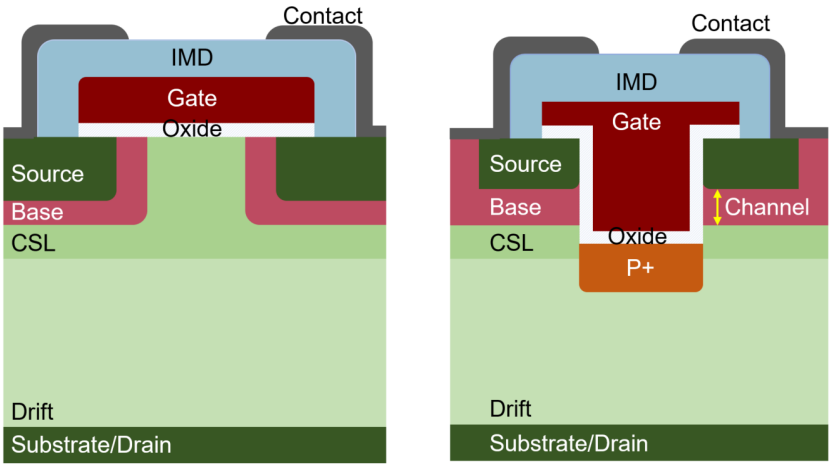
Figure 2.1. (a) Dangling bonds and abruptness at SiC/SiO_2 interface and (b) The low conduction band offset between SiC and SiO_2 leads to Fowler-Nordheim tunneling

Oxide reliability is also challenging, since SiC, as a wide bandgap semiconductor, exhibits a lower electron affinity than Si, resulting in a smaller conduction band offset between SiO_2 and SiC as shown in the Fig. 2.1(b). The smaller barrier height results in Fowler-Nordheim tunneling at lower oxide fields than in Si, and may lead to undesirable oxide leakage which can cause long term reliability issues like threshold voltage drift instability. Constant research and study are ongoing to better understand the SiC/SiO_2 interface, and hence to develop processes to improve quality. One promising process is post-oxidation annealing in the nitrogen environment, especially in nitric oxide (NO) or nitrous oxide (N_2O) at up to 1,300°C. The annealing process passivates the surface to create 4× lower interface trap density compared with non-annealed thermal oxide, which improves the mobility of the channel interface [20].

Further improvement can be availed in phosphoryl chloride ($POCl_3$) annealing at 1000°C for 10 min, which helps to reduce interface state density and thus increases the mobility in the channel [21]. The mobility in the channel at the NO annealed interface is reported as high as 45 $cm^2/(V \cdot s)$ while annealing in $POCl_3$ is reported to produce a mobility around 100 $cm^2/(V \cdot s)$. Despite having higher interfacial mobilities, $POCl_3$ annealed devices show threshold voltage instabilities which are a major reliability concern. Therefore the NO anneal technique is still the most widely accepted method of improving oxide interface quality in SiC technology.

2.2.2 Design Innovation

Structural innovation and design development is important to optimize the performance and maximize the reliability of devices.



(a) (b)

Figure 2.2. Two primary types of SiC MOSFETs: (a) DMOSFET, and (b) UMOSFET.

In current SiC MOSFET technology, devices are typically one of two different flavors - 1) Double Implanted (planar) (DMOSFETs), as shown in the Fig. 2.2(a) and 2) Trench Gate MOSFETs (UMOSFETs) as shown in Fig. 2.2(b). In both designs, current flows vertically from source to drain in the on-state. The difference between the two is the directionality of the channel formed by the base region near the interface underneath the gate electrode. In the former case, the channel is in lateral direction as defined by the source and base implantations, forming a intrinsic junction field effect transistor (JFET) region as shown in the Fig. 2.2(a). This JFET region contributes a certain resistance in the overall device, which can be largely eliminated in UMOSFET type devices. In the UMOSFET, the channel is formed vertically by forming a trench filled with the gate electrode with proper gate dielectric insulation as shown in Fig. 2.2(b). Moreover, the elimination of JFET region and repositioning of the channel and gate-source overlap areas to the trench sidewall reduces the cell pitch, aiding in specific on-resistance reduction. However, the oxide underneath the trench is more prone to early breakdown due to crowding of the electric field at the trench corners. A novel approach to shield the oxide at the bottom of the n-channel UMOSFET trench, is to implant a shallow, heavily doped p-type region underneath the trench [22] as depicted in the figure.

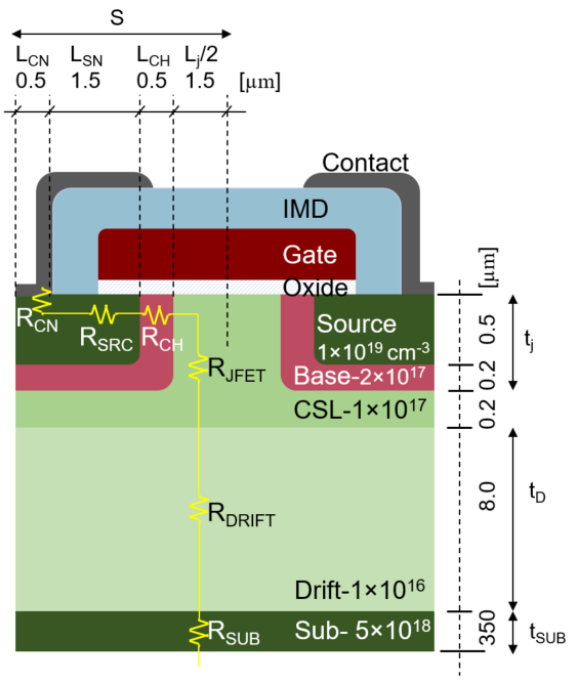


Figure 2.3. Resistance components of DMOSFET device

Apart from the dielectric reliability issue, these devices require an analysis and optimization of the different resistance components and cell pitch reduction. The resistance components and some critical dimensions of a SiC DMOSFET are illustrated in Fig. 2.3. The primary resistance components are the source contact and implant (R_{SOURCE}), channel (R_{CHAN}), JFET (R_{JFET}), drift (R_{DRIFT}) and substrate (R_{SUB}), respectively. The thickness of the JFET, drift and substrate layers are t_J, t_D and t_{SUB}, respectively, and S and L_J are the cell pitch and JFET width of a given unit cell as shown in Fig. 2.3.

With all the parameters defined, the total resistance of the device can be written as -

$$R_{ON} = R_{SOURCE} + R_{CHAN} + R_{JFET} + R_{DRIFT} + R_{SUB} \qquad [\Omega] \tag{2.1}$$

Assuming the width of the device be W, the specific on-resistance, the parameter to minimize, can be written as -

$$R_{ON.SP} = R_{ON} \times (SW) \qquad [\Omega \cdot \text{cm}^2] \tag{2.2}$$

The different resistance components are discussed in more detail below, with an estimate of their relative contributions to the overall specific on-resistance.

2.2.2.1 Source Contact Resistance

Metal is deposited to form an ohmic contact layer with the heavily doped n-type source region. Important factors to consider in order to achieve low contact resistance are the doping concentration of the source region and the barrier height between SiC and the metal. The doping concentration should be made as high as practical, e.g. 1×10^{19} cm^{-3}. The metal, with a work function around 4 eV, near the SiC electron affinity (3.8 eV), is chosen to make ohmic contact. In practice, nickel (Ni) with a 5.01 eV work function is normally used. Study has shown that 100-200 nm thick Ni is sufficient for making reliable contact with n-type SiC [23]. Titanium (Ti) is another metal that can also be considered. As deposited ohmic metal on source region results in about $1{\times}10^{-3}$ to $1{\times}10^{-4}$ $\Omega \cdot cm^2$ contact resistivity. The contact resistivity can further be improved by sintering the deposited Ni contact at 1,000°C for 2 min by rapid thermal processing (RTP) [4]. During this RTP process, Ni reacts with the SiC surface to form nickel silicide (Ni_2Si), and excess carbon accumulates near the surface. The accumulated carbon is removed, normally using a RIE etch step, to achieve a reduced barrier height between Ni−Si and SiC[4]. This process reduces contact resistivity to as low as 1×10^{-6} $\Omega \cdot cm^2$, which contributes less than 1% of the total resistance of a typical DMOSFET, and thus can often be neglected when calculating the total specific on-resistance. The same design considerations apply to the n-type drain contact at the bottom of the substrate. However, design constraints here are more relaxed due to the large contact area at the drain.

2.2.2.2 Source Resistance

During the on-state, electrons are injected from metal source contact, then flow through the source region to the channel. This source region, depending on the implant concentration,

exhibits a finite resistivity. A typical value for resistivity in the region is around 350 Ω/□, and the specific on-resistance due to source region alone can be expressed as -

$$\begin{aligned} R_{S,SP} &= \left(\rho_S \frac{L_{SN}}{W}\right) (SW) \\ &= \rho_S \, L_{SN} \, S \\ &= 350 \, L_{SN} \, S \end{aligned} \tag{2.3}$$

where L_{SN} is the total length of the gate to source contact gap and the gate source overlap regions, ρ_S is the sheet resistance of the source implant. Assuming L_{SN} and S be 1 µm and 3 µm respectively, the resistance contribution from only the source regions alone is about 0.01 $\text{m}\Omega \cdot \text{cm}^2$. This simplistic calculation, however, does not consider the crowding resistance due to current squeezing into the channel region, or for any accumulation of electrons near the interface in the gate-source overlap region which helps to reduce the resistance.

2.2.2.3 Channel Resistance

For gate voltages above the threshold voltage, the p-base region beneath the gate electrode becomes inverted to n-type, creating a channel from source to drain. If a positive drain bias is then applied, current flows through this channel region, which exhibits a finite resistance. In current SiC MOSFETs, especially those designed for applications rated for 1 kV or below, this component contributes a significant percentage of the total resistance. It depends on a number of factors, and can be expressed as simply as -

$$\begin{aligned} R_{CH,SP} &= \left(\rho_{CH} \frac{L_{CH}}{W_{CH}}\right) (SW) \\ &= \left(\frac{1}{q\mu_{CH} n_S} \frac{L_{CH}}{W}\right) (SW) \\ &= \frac{L_{CH} S}{q\mu_{CH} n_S} \end{aligned} \tag{2.4}$$

where L_{CH} is the channel length as shown in Fig. 2.3, μ_{CH} is the mobility of the channel carriers, and n_S is the channel carrier concentration in cm^{-2} at a given bias and threshold

voltage. For an n-type MOSFET, electrons act as the channel carriers in a p-type well. Here it is assumed that channel width is same as the device width, which usually the case for SiC DMOSFETs.

The channel mobility μ_{CH} as discussed in the Section 2.2.1, suffers from poor oxide-semiconductor interface quality, with a correspondingly large interface trap density D_{it}. With the adoption of the NO annealing technique, the mobility of the channel is around 20∼25 $\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$, as reported in [24]. Alternative annealing techniques or surface passivations may be developed to improve the mobility, opening a window for further research in the community. Channel resistance can also be reduced by shrinking the channel length L_{CH}. In a self-aligned process, L_{CH} can be shrunk to 0.5 µm. Further reduction in L_{CH} is limited by drain induced barrier lowering (DIBL) and p-base punch through. With a certain fixed cell pitch S of the device, the only other way to reduce the channel resistance is to increase the majority carrier density n_S. Using the simple gradual channel approximation, the density of channel carriers under an particular gate voltage, V_G and specific threshold voltage, V_{TH} can be written as -

$$\begin{aligned} qn_S &= C_{OX}\,(V_G - V_{TH}) \\ &= \frac{\epsilon_{OX}}{t_{OX}}\,(V_G - V_{TH}) \end{aligned} \tag{2.5}$$

where C_{OX} is the specific capacitance of the oxide, which depends on the dielectric constant (ϵ_{OX}) and thickness (t_{OX}) of the oxide. The specific on-resistance reduces with the increasing n_S. High n_S in (2.4), at a fixed V_G can be obtained by achieving high value in C_{OX} or low value in V_{TH}. A high-k dielectric, could potentially be used to increase the carrier density in the channel, but this may come at the expense of oxide reliability due to reduced conduction band offsets between SiC and the dielectric, since most high-k dielectric materials also have smaller bandgaps. Additionally, the dielectric strength of such materials is typically lower than SiO_2 restricting device operation to lower oxide fields, which compromises the channel carrier density and thus limits any possible resistance reduction. A thinner oxide is another way to increase the free carrier density, but is limited by the maximum electric field supported

by the oxide. The nominal thickness of the dielectric in current technology is around 30 nm–50 nm.

At an overdrive voltage ($V_G - V_{TH}$) of 15 V, a 0.5 µm long channel exhibits around 1.55 m$\Omega \cdot$ cm^2 specific on-resistance, with an assumption of a cahnnel mobility of 15 cm^2/(V $\cdot$ s). For a device designed for 1 kV or less, this component contributes around 70% of the total resistance. A novel approach to counter this issue will be proposed later in Section 2.3 to minimize this dominant resistance factor.

2.2.2.4 JFET Resistance

The inherent JFET region in a DMOSFET device plays an important role in total specific on-resistance. At a given doping, the JFET length as shown as L_j in Fig. 2.3 must be optimized to achieve minimum specific on-resistance. An increase in the JFET length, increases the total cell pitch, and thus the specific on-resistance. On the other hand, aggressive reduction is constrained by pinch-off of the JFET region, which effectively prevents current flow. Therefore the optimized JFET length must be found for a device at a given doping concentration.

Another important parameter to optimize this resistance component is the JFET region doping density. The JFET resistance decreases with an increase in doping, but this comes with unwanted electric field crowding near the corner of the base implant, which may cause early device breakdown. Additionally, the high energy p-type base implantation must counter dope this high JFET doping to form the base layer. High p-type base doping increases the threshold voltage, and thus increases the channel resistance. Typically, the JFET region can be doped as high as 1×10^{17} cm^{-3}, and may extend below the base region. This extension is known as a current spreading layer (CSL), and its purpose is to efficiently spread the current over the whole area of the drift layer. This effectively reduces the drift layer resistance by

increasing the effective current conducting area. The JFET specific on-resistance of a device with the dimension specified in the Fig. 2.3, can be expressed as

$$\begin{aligned} R_{J,SP} &= \rho_J \frac{t_J}{(L_J/2 - x_{dj})W} \, (SW) \\ &= \rho_J \frac{t_J S}{(L_J/2 - x_{dj})} \end{aligned} \tag{2.6}$$

In this expression ρ_J is the resistivity at the JFET region defined by doping concentration and the mobility, and x_{dj} is the width of the space charge region at the p-base to JFET junction, can be written as

$$x_{dj} = \sqrt{\frac{2\,\epsilon_S}{q\,N_J}\,(V_{BI} + V_J)} \tag{2.7}$$

Where ϵ_S is the permittivity of SiC, N_J is the JFET doping concentration, V_{BI} is the built in potential at base-JFET junction and V_J is the JFET voltage drop at a certain current ($\sim$250–300 A/cm^2). The JFET node voltage can be calculated as follows -

$$V_J = I_{ON}(R_S + R_{CH}) \tag{2.8}$$

Here, I_{ON} represents the device on current and R_S and R_{CH} are source and channel resistance respectively. This analysis does not assume any lateral straggle of the implantation which is normally the case and a function of implant energies. To better capture the JFET votlage and JFET resistance contribution, a numerical simulation must be done.

The resistivity of the JFET region with mobility μ_J can be expressed as -

$$\rho_J = \frac{1}{q\mu_J N_J} \tag{2.9}$$

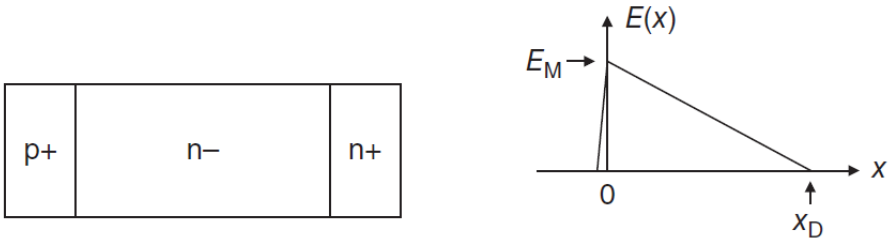
The mobility in JFET region can be expressed as [25]-

$$\mu_J = \frac{1141(T/300)^{-2.582}}{1 + (N_J/1.94 \times 10^{17})^{0.61}} \tag{2.10}$$

With the nominal values of the parameters as shown in the Fig. 2.3, the JFET resistance can be approximated at around 0.08 m$\mathbf{\Omega} \cdot$ cm^2.

2.2.2.5 Drift Resistance

The drift layer resistance is defined by the thickness and the doping concentration of this layer, which are determined by the desired blocking voltage. In a simple one sided p-n junction as shown in the Fig. 2.4(a), the electric field will be as shown in Fig. 2.4(b) for a non-punch-through case.



(a) (b)

Figure 2.4. (a) Simple one sided p-n junction, (b) Electric field profile in the non-punch-through case

The depletion width is mainly comprised of the space charge region in the lightly doped n-type drift layer, which at a given blocking voltage V_B and doping concentration N_D can be expressed as -

$$x_{DB} = \sqrt{\frac{2\epsilon_S V_B}{qN_D}} \tag{2.11}$$

Blocking voltage, in turn, is the total area under the curve in Fig. 2.4(b), and can be expressed as -

$$V_B = \frac{1}{2} E_C x_{DB} \tag{2.12}$$

Combining (2.11) and (2.12), the expression for blocking voltage can be written as –

$$V_B = \frac{\epsilon_s E_C^2}{2qN_D} \tag{2.13}$$

To achieve higher blocking voltages, the doping density of the drift layer must be reduced. Reduced N_D will give rise to increased x_{DB}, and eventually punch-through will occur when x_{DB} is greater than the drift layer thickness, which is illustrated in Fig. 2.5.

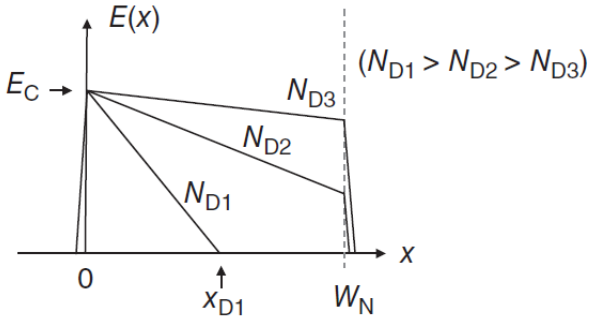


Figure 2.5. Electric field profile under punch-through at lower doping concentrations

In the limit of zero doping, the blocking voltage reaches its maximum V_{BMAX}, which can be written as–

$$V_{BMAX} = E_C W_N \tag{2.14}$$

The typical blocking voltage as a function of doping concentration and drift layer thickness can be plotted as shown in the Fig. 2.6.

A high blocking voltage can be achieved with a lightly doped drift region as shown in Fig. 2.5, but the specific on-resistance during on-state will increase. On the other hand, if the drift layer doping is increased, the on-resistance will be reduced with a corresponding decrease in blocking voltage. Therefore the drift layer thickness should be designed in order to maximize the device figure of merit V_B^2/R_{ON}. To design the drift layer thickness, a method described in [25] is followed. In this method, a drift layer thickness is assumed, and the blocking voltage at a certain drift layer doping is found from the hole or electron ionization integral. Then the doping level is adjusted and a family of blocking voltage curves as a function of doping is obtained at a given drift layer thickness. The same procedure is followed for different drift layer thicknesses, and a complete set of curves of drift layer specific on-resistance is generated as a function of blocking voltage and doping. From this curve set, an optimal punch-through drift layer thickness has been chosen to maximize the device figure of merit.

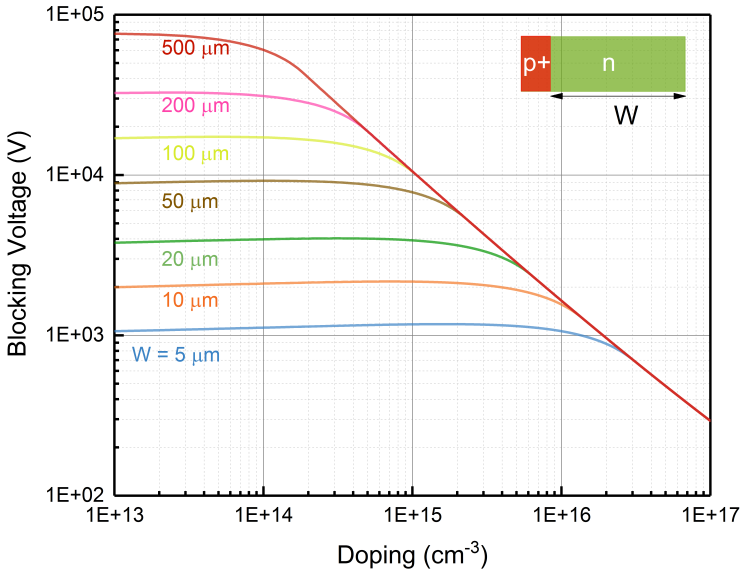


Figure 2.6. Blocking voltage as a function of drift layer doping concentration and thickness

To design a device rated at a blocking voltage of 1300 V, a 8 µm thick and 1×10^{16} cm^{-3} doped drift layer is needed. These parameters will ultimately define the resistance contribution of the drift layer.

The drift layer specific on-resistance in a non-CSL design, and assuming a 45°angle current spread from JFET to drift, can be written as

$$R_{DR,SP} = \rho_{DR}[S \ln(1 + \frac{S - L_J/2 + x_{dj}}{L_J/2 - x_{dj}}) + (t_D - S + L_J/2 - 2x_{dj})] \tag{2.15}$$

The dimensions are defined in the Fig. 2.3. The space charge region at base-drift junction is expressed as x_{dj} while ρ_{DR} is the resistivity of the drift layer which can be expressed as

$$\rho_{DR} = \frac{1}{q\mu_N N_D} \tag{2.16}$$

where μ_N and N_D are the electron mobility in the drift layer and the drift layer doping concentration, respectively. The mobility of the drift layer depends on both temperature and doping concentration and can be empirically expressed as [25]

$$\mu_N = \frac{1141(T/300)^{-2.582}}{1 + (N_D/1.94 \times 10^{17})^{0.61}} \tag{2.17}$$

At room temperature, with the dimensions and doping specified in Fig. 2.3, the drift layer specific on-resistance contribution without a CSL layer is 0.63 m$\Omega \cdot$ cm^2. If a CSL layer was included in this particular case, a 16% reduction in resistance could be achieved. Drift layer resistance is not the dominant factor in a device rated at 1 kV or below, where the channel and the substrate resistances dominate.

2.2.2.6 Substrate Resistance

The nominal thickness of a SiC wafer is generally 350 µm. The substrate plays an important role in the total specific on-resistance in devices designed for low voltage applications. The region is heavily doped to minimize the resistance and to provide a good ohmic drain contact. The substrate resistivity is given as a specification with the wafer, and is generally between 15–28 mΩcm at room temperature, corresponding to a doping concentration of 10^{18}-10^{19} cm^{-3}. The specific on-resistance due to substrate can be written as –

$$\begin{aligned} R_{SUB.SP} &= \left(\rho_{SUB}\frac{t_{SUB}}{SW}\right)(SW) \\ &= \rho_{SUB}t_{SUB} \end{aligned} \tag{2.18}$$

In this equation, ρ_{SUB} is the resistivity, and t_{SUB} is the thickness of the substrate. With a thickness of 350 µm and a resistivity of 28 mΩcm, the specific on-resistance contribution from the substrate is around 0.98 m$\Omega \cdot$ cm^2. Special consideration should be given to minimizing this dominant resistance component for devices designed to block less than about 2 kV. This may include thinning the wafer to as low as 120 µm after device fabrication.

Specific on-resistance as a function of blocking voltage for various devices on both SiC and Si are shown in the Fig. 2.7.

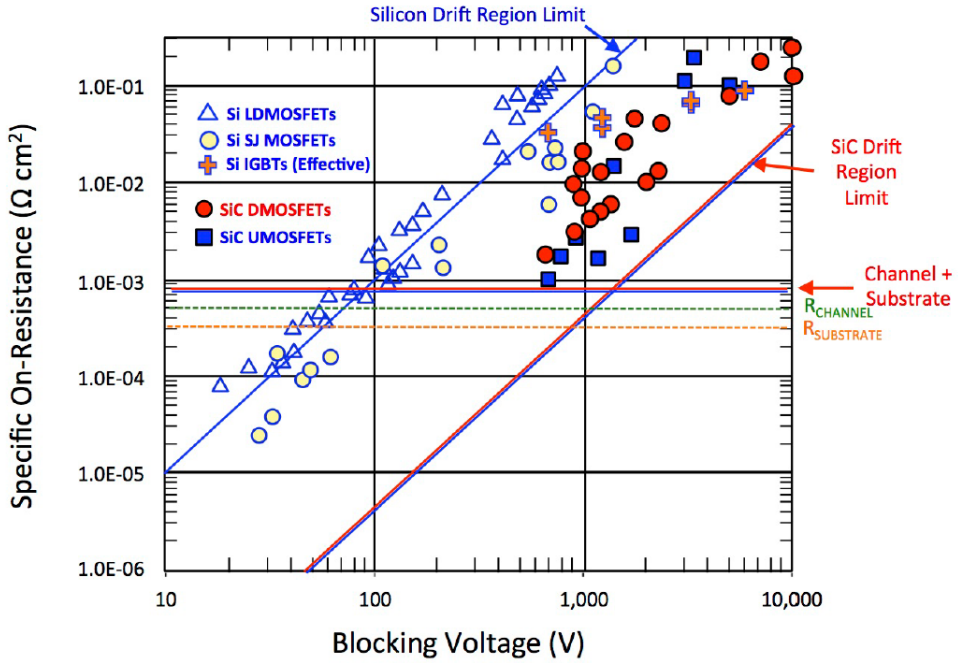


Figure 2.7. Specific on-resistance as a function of blocking voltage for different device designs in SiC and Si [4], [26]

It can be seen that for applications below 1 kV, channel and substrate resistances play the dominant role, while drift resistance becomes significant at higher blocking voltages due to the decrease in doping and increase in required thickness of the drift layer. The approximate resistance contribution from different components are shown in Fig. 2.8 for a 900 V device with a 0.5 µm, 2×10^{17} cm^{-3} doped channel exhibiting 30 cm^2/(V · s) peak field effect mobility. The contact resistivity is assumed to be 6×10^{-6} $\Omega \cdot$ cm^2.

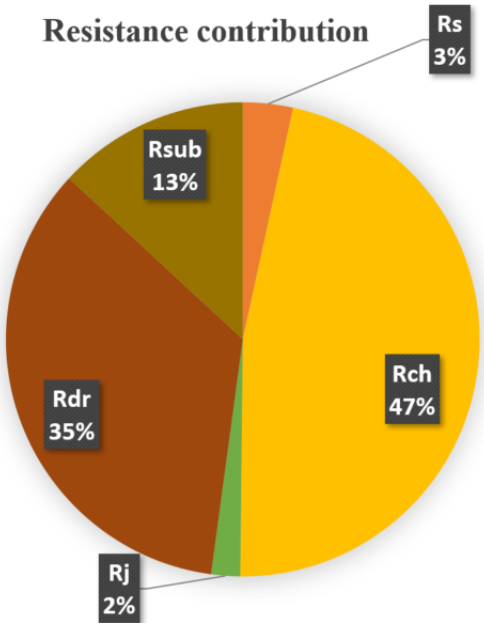


Figure 2.8. Resistance contribution of 900 V DMOSFET device

For lower voltage applications (<1 kV) as discussed in the Section 2.1, it is imperative to develop an improved design to minimize the resistance contributions from the channel and the substrate.

2.3 Proposed Tri-gate SiC MOSFET

As seen in the previous section, a dominant contribution, above 70% of total specific on-resistance, comes from the channel region for voltage applications below 1 kV. Improvement in the channel resistance is necessary in order to fulfill the promise of low conduction losses in SiC devices. The challenge can be addressed in a number of ways. A novel approach in this proposal will be embraced to increase the effective channel width without increasing the total device area, reducing the specific on-resistance by a factor of 3 or more. Other methods that may improve channel mobility complement this approach, and could provide even more significant improvements. A brief discussion on these parameters is given in Section 2.2.1 and 2.2.2.3.

The channel resistance in an n-type SiC MOSFET device can be written as -

$$R_{CHAN} = \frac{L_{CH}}{W_{CH}} \frac{1}{\mu_N C_{OX}(V_G - V_{TH})} \tag{2.19}$$

where L_{CH} and W_{CH} are the channel length and width respectively. From here, specific channel on-resistance can obtained by multiplying (2.19) by the area of a unit cell.

$$R_{CHAN} = \frac{L_{CH}}{W_{CH}} \frac{1}{\mu_N C_{OX}(V_G - V_{TH})} (SW) \tag{2.20}$$

In a normal DMOSFET or UMOSFET, the channel width W_{CH} is essentially same as the total width of the device W. Thus the channel specific on-resistance does not depend on any additional parameter. However, if a device can be elegantly engineered to decouple these two parameters and make W_{CH} larger than W, a significant reduction in channel resistance is possible. An adaptation of a tri-gate type structure, similar to the FinFET originally proposed at U. C. Berkeley [27] and later applied by Intel for their 22 nm node for improved gate control and reduced drain induced barrier lowering [28], can be applied to the power MOSFET, but for a completely different purpose. In this case it is used to increase the effective current path area by reducing the W/W_{CH} factor less than unity.

The idea is explained first by depicting the structure of a conventional DMOSFET with interdigitated source and gate fingers as shown in Fig. 2.9(a). The whole device can be zoomed in to show a closer view of source and gate fingers like in Fig. 2.9(b) If an isometric angle is taken along the cut line shown, the device would look like in Fig. 2.9(c). From this figure it is clear that the width of the channel and the device (into the page) is same, giving a unity W/W_{CH} factor.

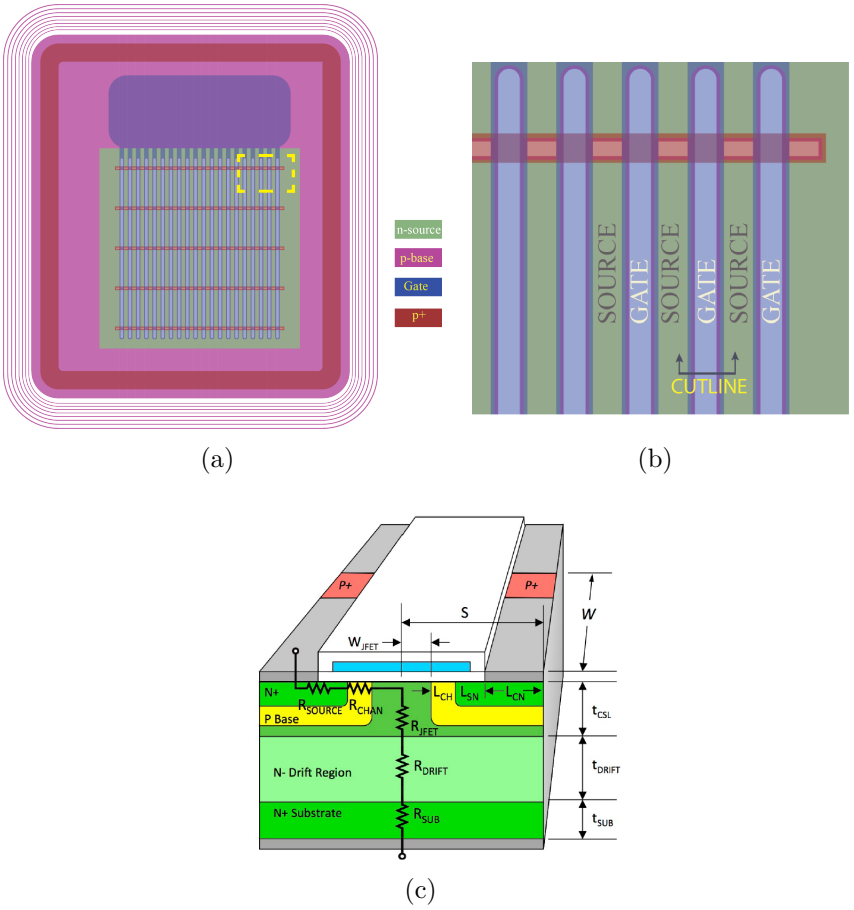
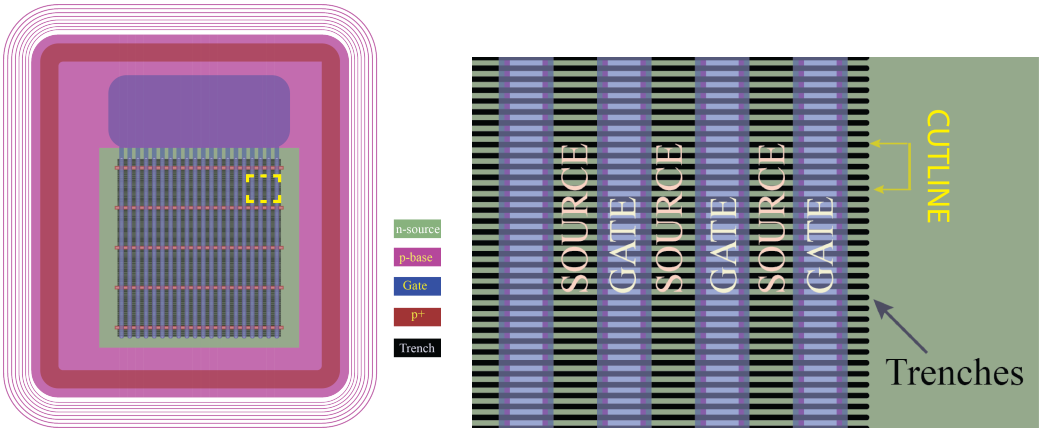
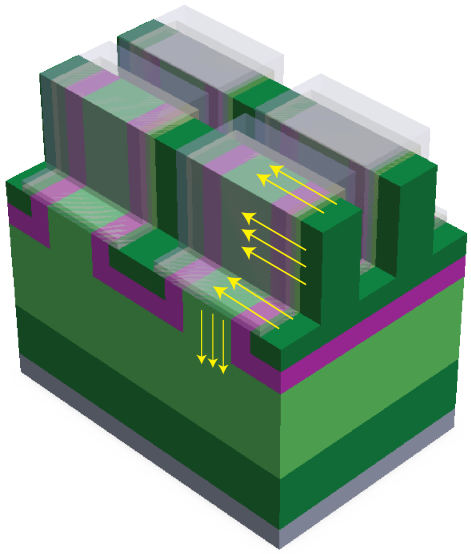


Figure 2.9. DMOSFET design structure (a) Complete device, (b) Close-up view, and (c) An isometric view from the cut-line of (b)

In the proposed tri-gate MOSFET structure (also referred to as a 3G-MOSFET), narrow fins and trenches are formed perpendicular to source and gate fingers, before gate oxidation as shown in the Fig. 2.10. An isometric view of such a design is shown in Fig. 2.10(c). The etch opens up an additional current path along the sidewall of the trench, along a $\{11\bar{2}0\}$ face, in addition to the current on the top and the bottom of the trench along (0001), as usual. The additional current path is shown in Fig. 2.10(c) in arrows. The design utilizes the sidewall to increase the channel width, keeping the cell pitch and width the same, making W/W_{CH} less than unity.



(a) (b)



(c)

Figure 2.10. Tri-gate MOSFET design structure (a) Complete device, (b)Closer view of a and (c)An isometric view from the cut-line of (b)

The specific on-resistance of the channel decreases proportionally with the decrease in the W/W_{CH} ratio, as seen directly from Equation 2.20. Moreover, the electron channel mobility along a sidewall $\{11\bar{2}0\}$ face may be as much as 4 times higher than along the (0001) face [29].

Considering the additional effective channel width, and taking into account the mobility difference on the two faces, the $W_{CH}\mu_N$ term in (2.20) can be expressed as

$$W_{CH}\ \mu_N = W_{(0001)}\ \mu_{(0001)} + W_{(11\bar{2}0)}\ \mu_{(11\bar{2}0)} \tag{2.21}$$

The channel resistance of tri-gate MOSFET can be approximated by replacing $W_{CH}\ \mu_N$ from the Equation 2.21 in the Equation 2.20 as written below

$$R_{CHAN.3G} = \frac{L_{CH}S}{C_{OX}(V_G - V_{TH})} \frac{W_{(0001)}}{W_{(0001)}\ \mu_{(0001)} + W_{(11\bar{2}0)}\ \mu_{(11\bar{2}0)}} \tag{2.22}$$

In the conventional DMOSFET, with W/W_{CH} factor as unity, the expression for the specific on-resistance for the channel would be

$$R_{CHAN.DMOSFET} = \frac{L_{CH}S}{\mu_{(0001)}C_{OX}(V_G - V_{TH})} \tag{2.23}$$

To compare the advantage of the tri-gate MOSFET, Equation 2.22 can be divided from Equation 2.23 -

$$\begin{aligned} \frac{R_{CHAN.3G}}{R_{CHAN.DMOSFET}} &= \frac{\mu_{(0001)}W_{(0001)}}{W_{(0001)}\ \mu_{(0001)} + W_{(11\bar{2}0)}\ \mu_{(11\bar{2}0)}} \\ &= \frac{1}{1 + \frac{W_{(11\bar{2}0)}\mu_{(11\bar{2}0)}}{W_{(0001)}\mu_{(0001)}}} \\ &= \frac{1}{1 + 4\frac{2T}{W}} \end{aligned} \tag{2.24}$$

In this equation it is assumed that sidewall mobility, $\mu_{(11\bar{2}0)}$ is 4 times higher than horizontal surface mobility, $\mu_{(1000)}$. T is the trench depth, and since there are two sidewalls in each unit cell, $W_{(11\bar{2}0)}$ is equal to $2T$ and the horizontal surface $W_{(0001)}$ is expressed as W for simplicity. From Equation 2.24, the specific on-resistance is expected to fall with proportional increase in

trench depth. However, deep trenches require deep source and base junctions, which involves high energy ion implantation. Ion implantation above several MeV is challenging and difficult to achieve. The trench depth can also be limited by other resistance components, such as the JFET resistance. Increasing the trench depth also increases the thickness of the JFET region, increasing its resistance. Therefore the benefits of the tri-gate eventually saturate as the trench depth increases.

3. DEVICE DESIGN AND MASK LAYOUT

The device design and mask layout is discussed in this chapter, which starts with a brief overview of the top level mask layout organization, showing the different device variations. Simulation studies using the Sentaurus suite of TCAD tools are discussed next, which were performed to determine the optimal device parameters. Finally, the mask layout design will be discussed in detail.

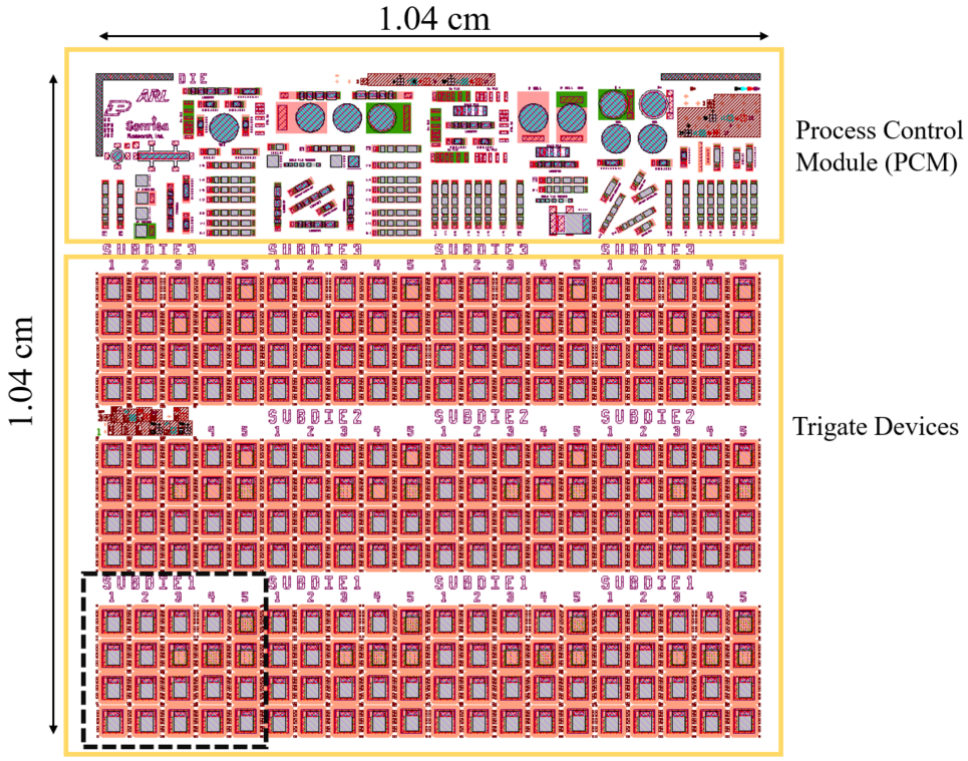


Figure 3.1. Trigate mask layout die.

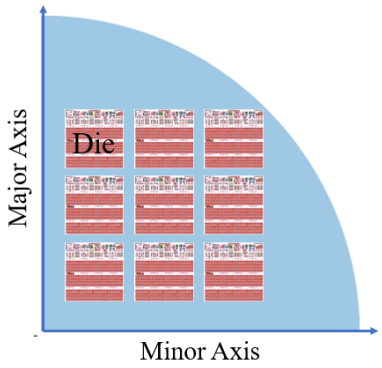


Figure 3.2. Tri-gate device die in the quarter wafer SiC sample.

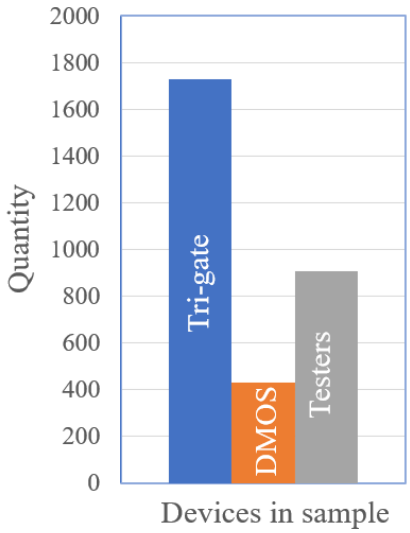


Figure 3.3. Device distribution in a Tri-gate sample.

Each die is composed of 3 sub-die as shown in Fig. 3.1. The active region of the die can be divided into 3 rows of equal size. All of the dies and sub-dies are arranged such that the x-axis in Fig. 3.2 lies along the minor axis of the wafer, which makes the trench sidewall faces to be revealed on $\{11\bar{2}0\}$ or a-faces. The bottom, center, and top rows are named 'SUBDIE1', 'SUBDIE2', and 'SUBDIE3' respectively. Each sub-die consists of a total 25 devices which include 4 non-trench or DMOS vertical MOSFET devices. A typical sub-die is shown in Fig. 3.4 where green dashed line indicates the location of the DMOS devices. The device distribution in each die is shown in Fig. 3.5. The letters on the devices denote

the type of each device. There are total 12 types of devices which differ from each other in the combination of JFET length and source contact length. Table 3.1 shows the all the variations of device type included in the mask, and defines the letter based nomenclature used throughout this thesis. The JFET and contact length definitions are shown in Fig. 3.6 on a finished tri-gate device.

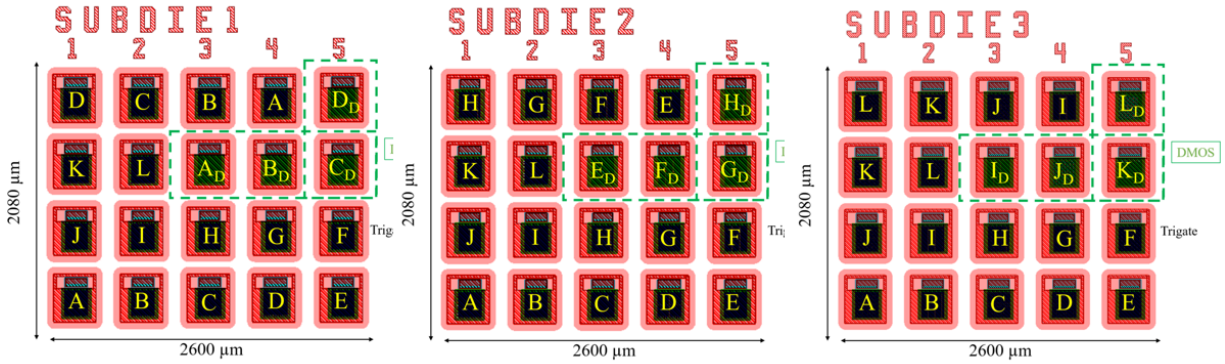


Figure 3.4. Tri-gate mask layout sub-die. 'D' subscript indicates the location of a DMOSFET of the specified design

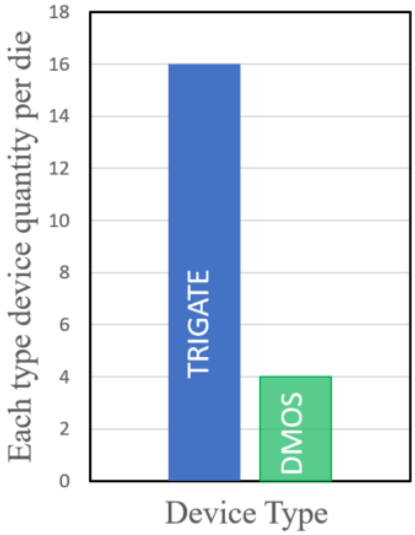


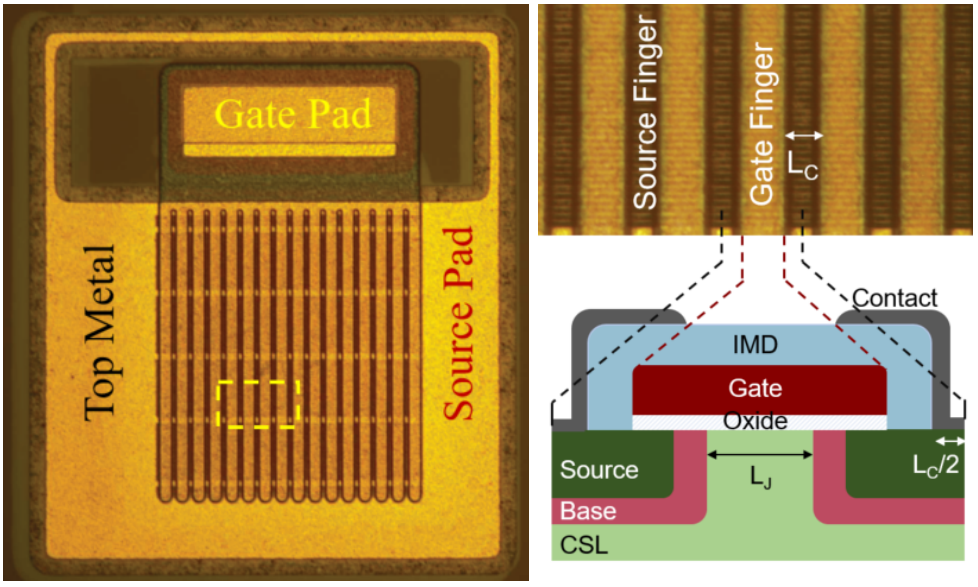
Figure 3.5. Device distribution in a single die.

Table 3.1. Device variation in Gen-1 tri-gate mask layout.

Device Name	JFET length (µm)	Contact length (µm)	FFR design type
A	2.0	1.0	i
B	2.0	3.0	ii
C	2.5	1.0	iii
D	2.5	3.0	iv
E	3.0	1.0	iv
F	3.0	3.0	iii
G	3.5	1.0	ii
H	3.5	3.0	i
I	4.0	1.0	i
J	4.0	3.0	ii
K	4.5	1.0	iii
L	4.5	3.0	iv

FFR type	Initial spacing (µm)	Initial width (µm)	Expansion ratio
i	1.15	1.0	1.05
ii	1.25	1.0	1.05
iii	1.35	1.0	1.05
iv	1.45	1.0	1.05

*Gen-2 tri-gate mask layout orientation is different, and is described in Appendix B



(a) (b)

Figure 3.6. Process parameter– JFET length and contact length visualization: (a) A finished tri-gate device, and (b) Closer view on the highlighted region showing JFET length and contact length in the device.

3.1 Device Design - JFET Length

In power devices, a fundamental unit cell, as shown in the example of a DMOSFET in Fig. 3.7, is repeated and connected in parallel to make up the overall device. It is thus desirable to achieve a minimum unit cell pitch, while minimizing specific on-resistance, in order to accommodate as many of these cells as possible in a given die area. However, compactness of the design may lead to an unwanted increase in resistance.

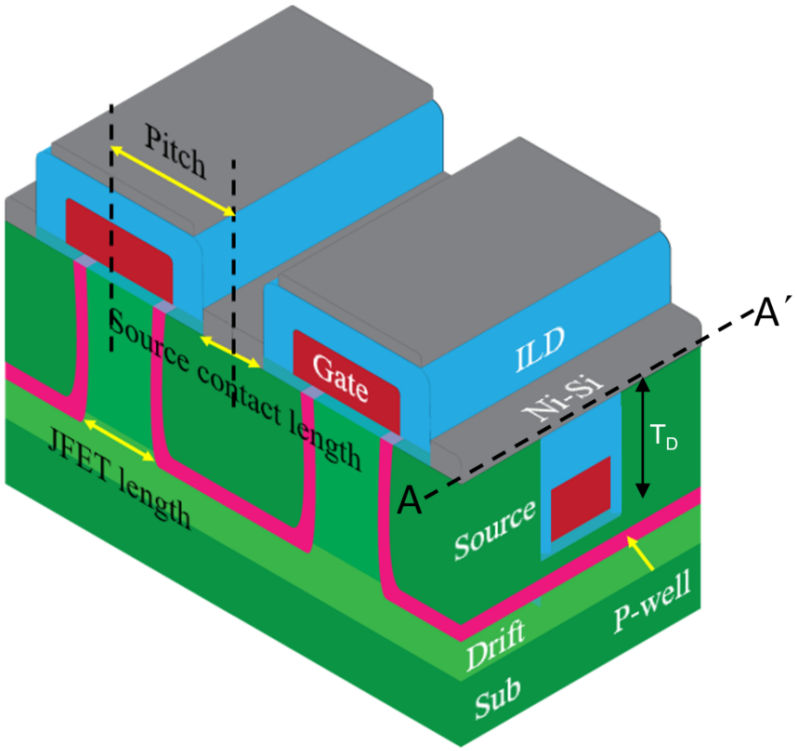


Figure 3.7. Tri-gate device structure.

One way to shrink the cell pitch is to reduce the JFET length. However, aggressive reduction in the JFET length will lead to pinching off of the region between two adjacent p-base regions, increasing resistance, and ultimately preventing current flow entirely. So an overall optimization in JFET length is needed to achieve optimum cell pitch and minimum possible specific on-resistance.

A TCAD simulation of the tri-gate MOSFET was done to identify the optimal JFET length. In this study, the trench depth was held constant at 2 µm, with a 1 µm cell pitch

along the A-A′ direction as shown in Fig. 3.7. Trench and fin widths are both assumed to be 0.5 µm. It is also assumed that the doping of the JFET region is 1×10^{17} cm^{-3} and the sidewall carrier mobility and horizontal surface mobility are equal to ∼25 $cm^2/(V \cdot s)$.

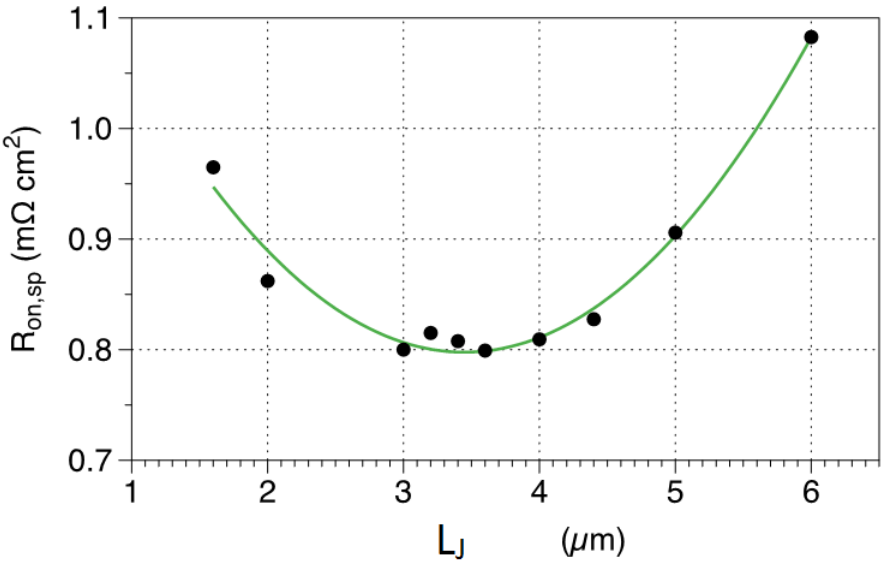


Figure 3.8. Simulated specific on-resistance variation with the JFET length .

From the analysis it can be concluded that aggressive scaling, such as JFET length less than 2 µm, results in pinch-off, while the dimension greater than 4.5 µm results in an excessive increase in device area and thus increased specific on-resistance. Hence an optimum range for the JFET length is between 2.0 – 4.5 µm as shown in Fig. 3.8, which is the range used in the mask design to find the true optimal value experimentally.

3.2 Device Design - Contact Length

Another way to shrink the cell pitch is to reduce the source contact length as shown in Fig. 3.7 In theory, this length should be carefully designed to restrict it to about the transfer length, which is the effective distance the current spreads underneath the contact, and is a function of both contact resistance and the semiconductor sheet resistance beneath the contact. The portion of the contact outside this margin does not contribute significantly to

the total current, and thus only increases area. Therefore the source contact length should be on the order of the transfer length.

$$L_T = \sqrt{\frac{\rho_C}{\rho_S}} \tag{3.1}$$

where ρ_C and ρ_S are the specific contact resistivity and semiconductor sheet resistivity respectively, and L_T is the transfer length. The value of ρ_C can be made as low as 1×10^{-6} $\Omega \cdot \text{cm}^2$. The sheet resistance, ρ_S of the n-type source region depends on the mobility and doping of the source. The sheet resistance of a 2 µm deep source region doped at 1×10^{19} cm^{-3}, can be estimated to be around 50 $\Omega/\square$ at room temperature. The values of the parameters, then can be used to calculate L_T, which is estimated to be approximately 1.4 µm.

Based on this estimation, two schemes for source contact length have been deployed in the design:

1. Conservative approach: contact length = 1.5 µm

2. Aggressive approach: contact length = 0.5 µm

The latter approach will reduce the cell pitch. A reduction in cell pitch may yield low on-resistance, but aggressively short contact lengths increase the source resistance contribution, but this can be tolerated to a point, since the channel and substrate resistances are typically higher. The combination of 6 different JFET lengths and 2 different source contact lengths gives rise to 12 different device types in the mask layout as listed in the Table 3.1.

3.3 Device Design - Floated Field Ring (FFR) Edge Termination

The edge of power devices are susceptible to electric field crowding and premature breakdown if not terminated properly. There are a number of ways the edges can be protected, each technique having its own pros and cons. The edge termination technique adopted in this work is an array of floated field rings. Floated field rings are usually concentric, isolated, highly acceptor doped rings surrounding the main device. These rings are fabricated during the same processing level as the main junction, so no extra lithography step is needed. An-

other advantage of the FFR design is that there is no need to maintain precise control of the implantation dose, which is imperative for other approaches like the junction termination extension (JTE) method. Another advantage of a FFR structure, since it is not connected to the base layer, is that it has greater dV/dt ruggedness compared to a JTE. Essentially it eliminates any recombination or diffusion of minority carriers from the termination region during an off to on switching transition.

The spacings and widths of these rings are carefully chosen so that the electric field peaks at the device edge is evenly distributed among the rings. If the initial spacing sufficiently large, then device can break down at the corner of the main junction before reaching the first ring. The same argument applies for the subsequent spacings of the rings - if any one of them is designed to be too large, the field may reach breakdown prematurely at the corner of the previous ring. On the other hand, if the widths and spacings are small, then electric field will not be distributed evenly among the rings and main junction. The outer ring, suffering from field crowding similar to the unterminated p-base region, will break down earlier than the other rings, hence not utilizing the full potential of the technique. Between these two extremes, a range of optimized spacings and widths of rings has to be chosen to distribute the field evenly and cause all rings to break down at the same voltage. Both cases are illustrated in Fig. 3.12.

A TCAD simulation analysis by Professor Dallas Morisette, principal investigator and major professor of the author, has been done to find the optimized spacing and width of the rings to achieve 900 V design or 600 V target voltage. The doping of the rings is the same as the p-base region, which is 2×10^{17} cm^{-3}. An optimized design is shown in Figure 3.9 with initial spacing of 1.25 µm and 1.0 µm initial width respectively. Both dimensions increase progressively with a 5% expansion ratio. The Fig. 3.9(a) shows the net doping profile and the depletion junction boundary at the breakdown which covers 9 rings. The Fig. 3.9(b) shows the potential distribution at breakdown which occurs at a drain voltage of 750 V which is 1.25× higher than the application voltage. The breakdown condition has been determined by evaluating the hole ionization integral. The Fig. 3.9(c) shows the hole ionization integral approaches 1 at the corner of the main junction during breakdown. The electric field surface component and potential distribution at the bottom of the p-type junctions are shown in

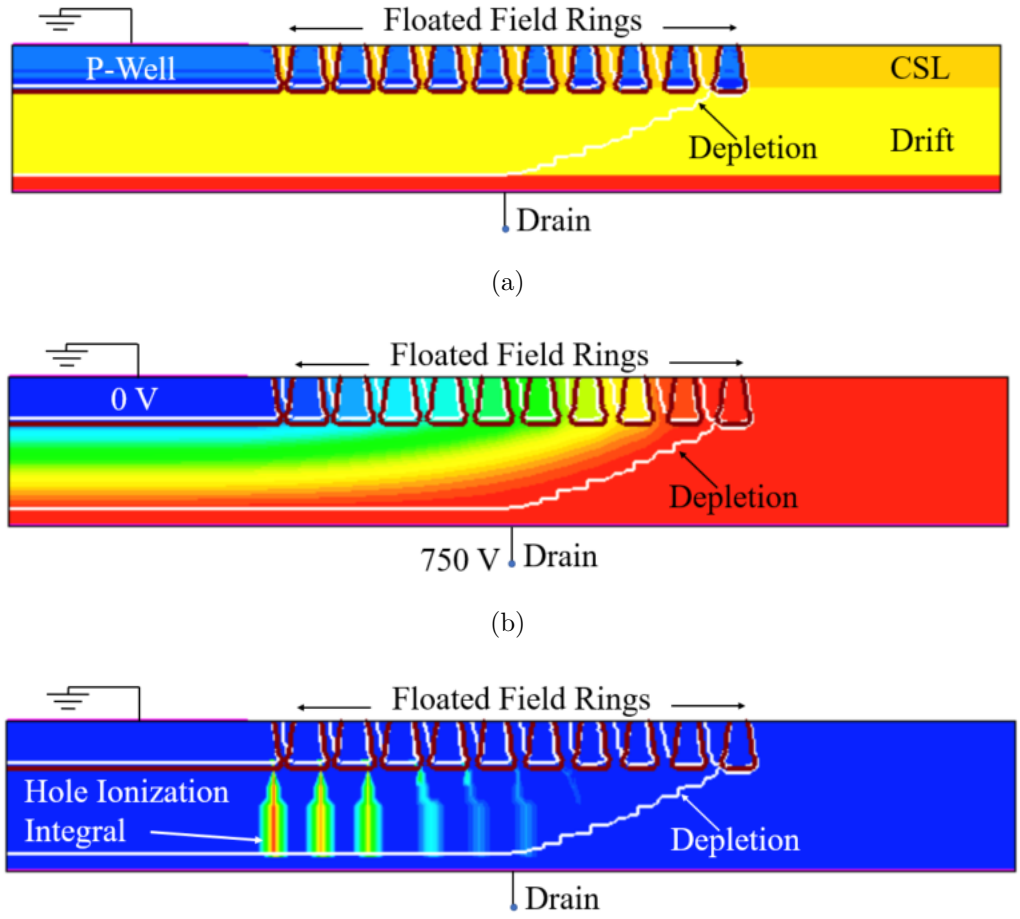


Figure 3.9. Optimzed FFR edge termination design for 600 V application: (a) Net doping profile with 10 FFR rings; (b) Potential distribution at breakdown occurring at V_D=750 V, and (c) Hole ionization integral path at breakdown.

Fig. 3.10. Ideally, the peak electric field at each corner of p-n junction should be equal. So, there is more room to improve the FFR edge termination design as shown in Fig. 3.9. Furthermore, in the simulation study, no surface charge effect has been considered. So in the design layout additional variations are included for experimental study. In contrast to the FFR design termination, the unterminated structure is also simulated as shown in Fig. 3.11, which shows a premature breakdown at 122 V. In this case, the breakdown primarily occurs due to the electric field crowding at the bottom corner of p-type junction.

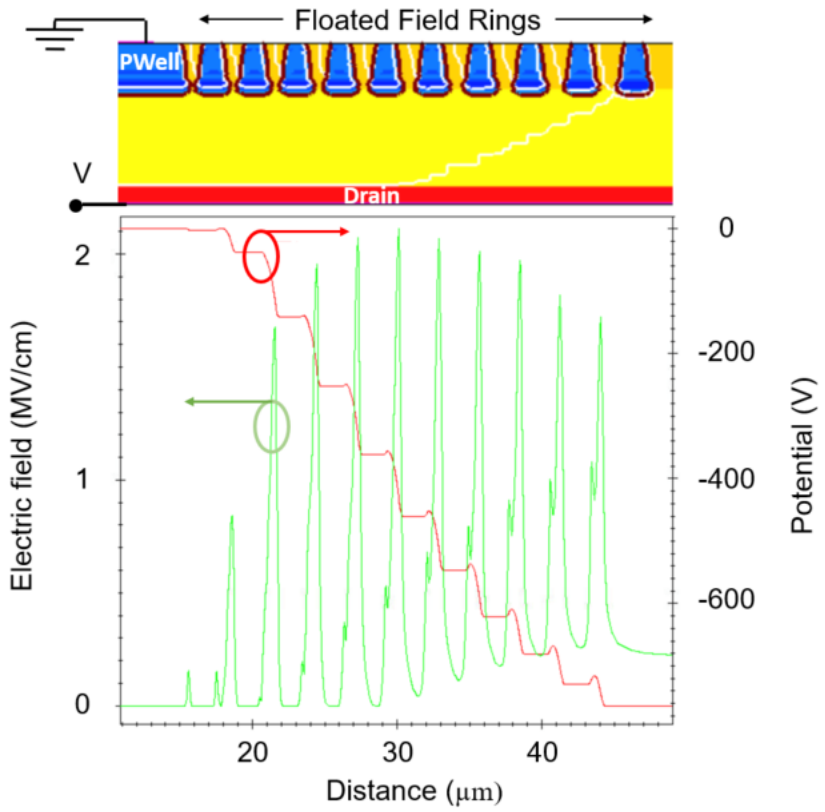
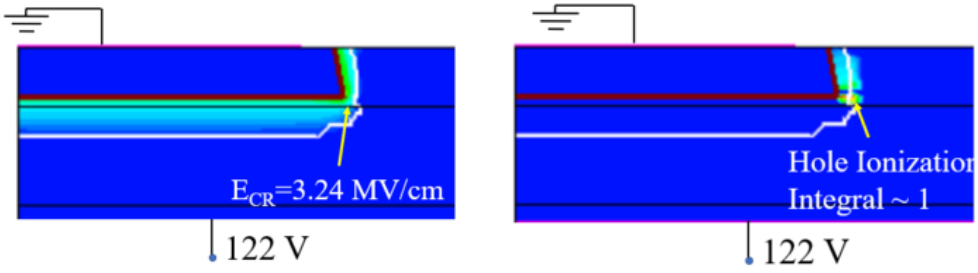
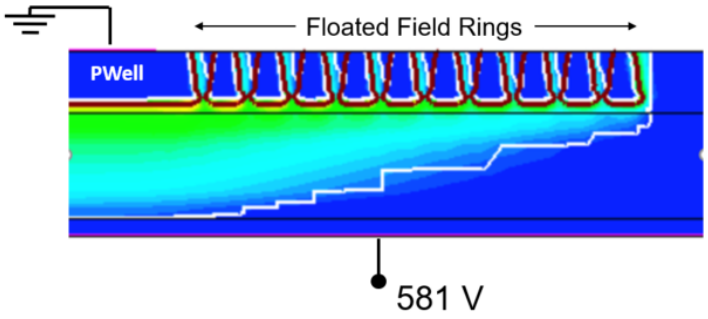


Figure 3.10. The electric field and potential distribution at breakdown condition.

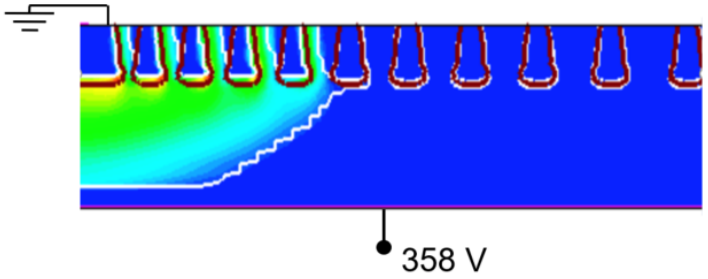


(a) (b)

Figure 3.11. Unterminated strcture: (a) Electric field at breakdown occuring at V_D=122 V, and (b) Hole ionization integral at breakdown.



(a)



(b)

Figure 3.12. Non-optimized FFR termination design for 900 V device : (a) FFR rings are tightly distributed making early depletion of all rings and premature electric field breakdown at the corner of last ring at 581 V drain voltage, and (b) FFR rings are loosely distributed making a few rings depleted and premature electric field breakdown at the corner of main junction at 358 V drain voltage .

3.4 Mask Layout

A detailed mask layout description used for Gen-1 and partly for Gen-2 tri-gate MOSFET is given below. In the description, mask numbers are for the reader's convenience, and other information are related to the mask layout file. The original mask was designed using the Mentor Graphics Pyxis software package, and later the design was converted to GDS file to use in a different tool. KLayout is an open source software package which can be used in several different operating systems. The names of the layers differ from the Pyxis design to the KLayout version, which is clearly discussed in the following description. The layer numbers are same for both of the environments, but the layer number must be within 1000 for the available fabrication tools to recognize the layer properly. This can easily be renamed and renumbered as needed in KLayout*. The resist information is also provided in the list, but a detailed fabrication description will be provided in the next chapter. The mask type information is also included, where "Light" means to expose the drawn features, while "Dark" means to the expose the inverse of the drawn features. This is consistent with the typical terminology used in the photomask industry.

The critical dimensions and alignment accuracy in some levels require very high resolution lithography, which only can be realized by e-beam lithography. However, this suffers from poor throughput, and the mask layer cannot be patterned in a practical exposure time. In order to solve this problem, features equal to or less than 4 µm are patterned in the e-beam lithography tool and a subsequent optical lithography tool is used for creating larger features. This threshold was set based on the practical lithographic limitations imposed by the optical Suss MJB-3 mask aligner tool in the facility. Later, with the arrival of a Heidelberg MLA-150, a high resolution optical mask-less aligner tool, the threshold dimension separating optical and e-beam lithography is reduced to 1 µm. However, any mask levels which require very tight alignment (e.g. < 0.5 µm) are still done in e-beam lithography irrespective of the minimum feature dimensions.

*Pyxis file location in the sharedrive wbg/masks/trigate/devices/MaskLayouy_p6GSO_ILD1_v1/
Klayout file location: wbg/masks/trigate/devices/Trigate_Naeem_Thesis.gds

3.4.1 P-well Implant - Optical Lithography

Mask# 1

Layer# 2012

Layer name: PO_pwell (Pyxis) / P_well_optical_allow (KLayout)

Mask Type: Light

Resist: AZ9260 (positive tone)

Description: This is an optical mask without any alignment to open windows to etch previously deposited 200 nm thick oxide in a wet chemistry. This 200 nm thick oxide acts as the mask for the 6 µm thick polysilicon etch in the field area. In the active region, the polysilicon etch mask to define JFET and FFR rings is implemented by the next level of e-beam lithography.

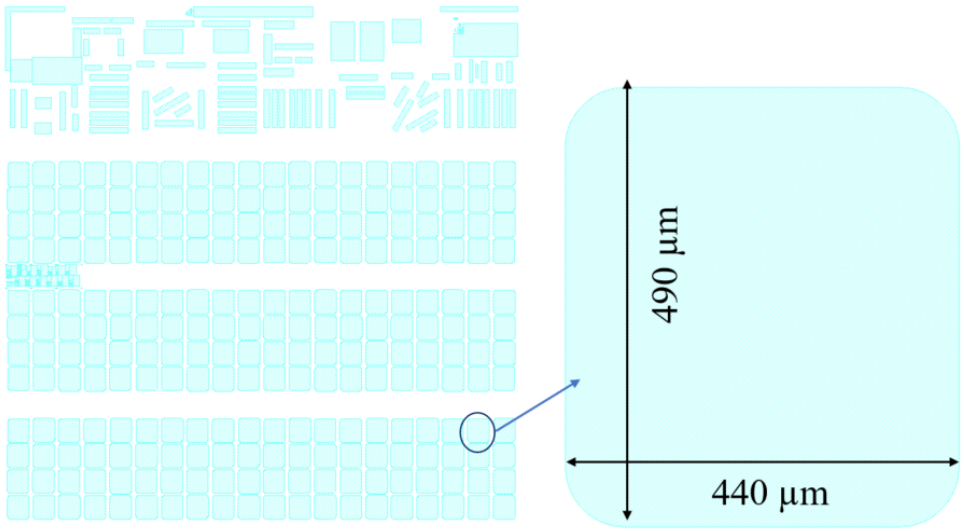


Figure 3.13. P-well implant optical lithography in the die and in the tri-gate device.

3.4.2 P-well Implant - E-beam Lithography

Mask# 2

Layer# 2011

Layer name: PE_pwell (Pyxis) / P_well_ebeam_block (KLayout)

Mask Type: Light

Resist: FOX-16 HSQ (negative tone)

Description: HSQ is a negative tone e-beam lithography resist. The resist is exposed under e-beam irradiation inside the active area to define the JFET regions and the FFR rings. The exposed resist becomes hardened to form an organic layer of Si_xO_y. This is used as a mask to pattern the polysilicon implant mask in the active region. It is a dual e-beam / optical lithography step to define the p-well implantation. The overlap between the optical and e-beam patterns is 10 µm.

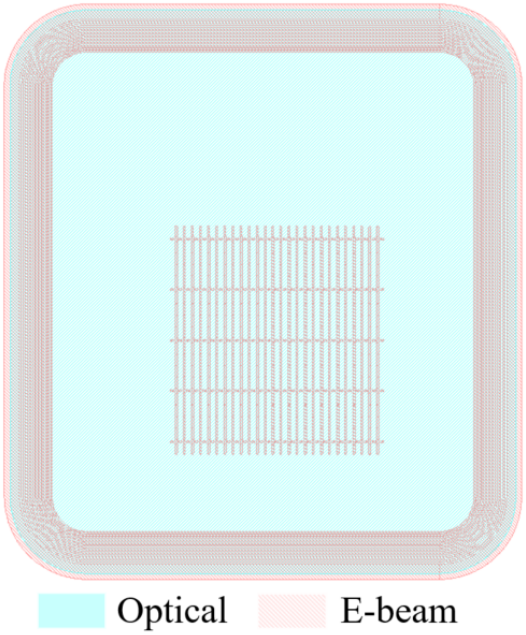
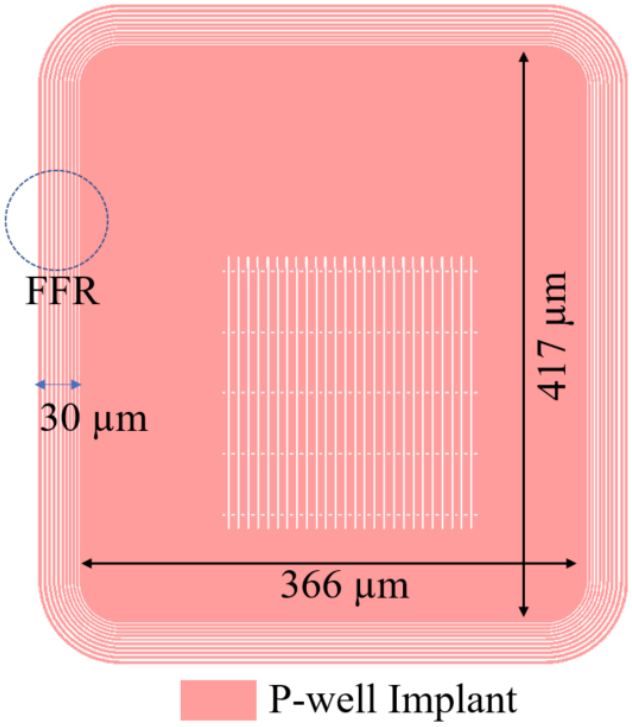
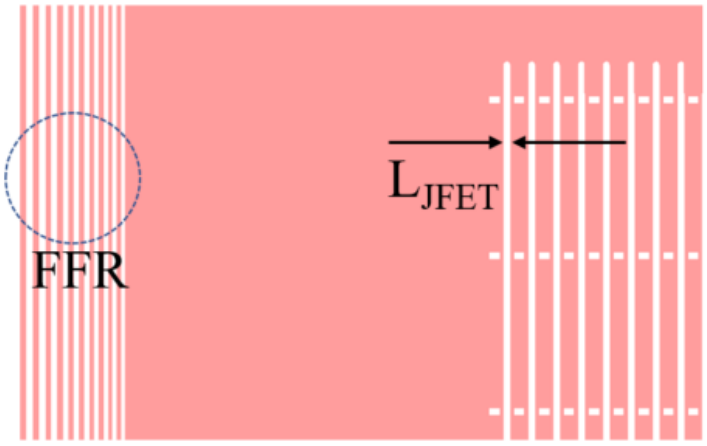


Figure 3.14. Dual e-beam/optical P-well implant mask



(a)



(b)

Figure 3.15. P-well implant mask: (a) Overall tri-gate device, and (b) Close view of FFR and JFET regions.

3.4.3 Alternate P-well Implant Single Step Mask

Layer# Composite of dark field version of 2011 and light field 2012

Resist: CSAR-6200 (positive tone)

Description: An alternative to the dual lithography process described above is a single e-beam lithography step which is enabled by AllResist CSAR-6200 resist. This is a very highly sensitive resist which results in high throughput e-beam writing. Even though a significantly larger exposure area is required compared to the dual lithography process, the high sensitivity enables an acceptably high throughput.

3.4.4 Alignment Mark

Mask# 3

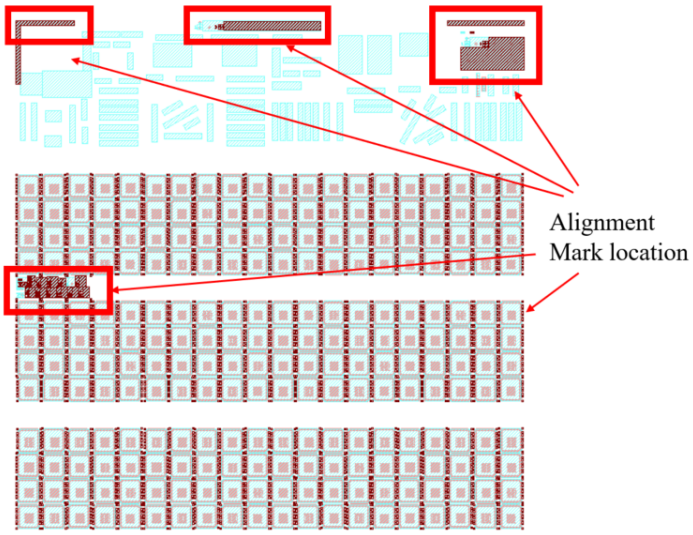
Layer# 2014

Layer name: PwellAMEtchAllow (Pyxis) /AM Etch alow (KLayout)

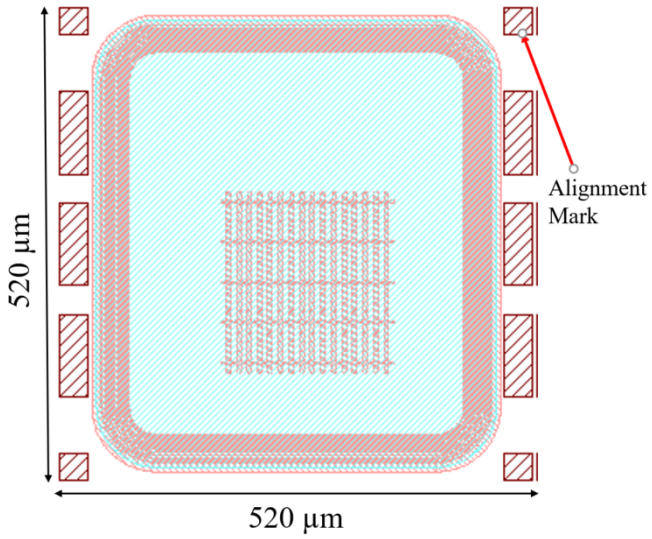
Mask Type: Light

Resist: AZ9260 (positive tone)

Description: The alignment marks are formed by patterning an AZ9260 photoresist layer to mask a 1 µm deep SiC etch. Three different types of alignment marks are designed to maintain compatibility with different systems. Square (10 µm × 10 µm) alignment marks are placed around the each device for use in a Vistec VB-6 e-beam lithography tool. Cross registration marks with a length of 40 µm and a width of 8 µm are used for Karl Suss MJB-3 optical mask aligner systems. A second type of cross registration marks with a length of 60 µm and 3 µm wide are included for the JOEL JBX-8100 FS e-beam lithography system and the Heidelberg MLA maskless aligner.

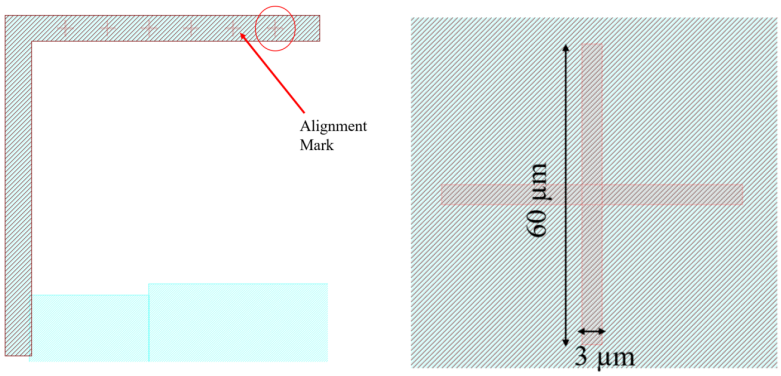


(a)



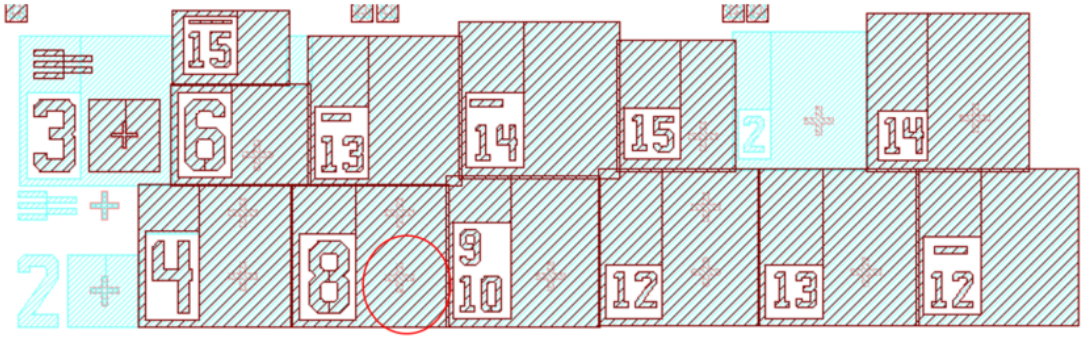
(b)

Figure 3.16. Alignment mark locations (a) within the die, and (b) Vistec VB6 e-beam alignment marks surrounding the tri-gate devices.

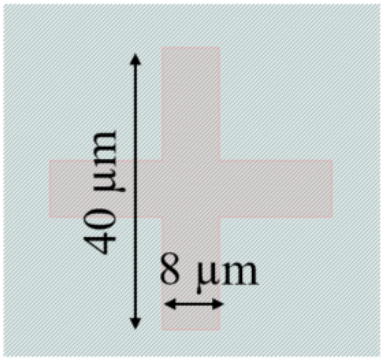


(a) (b)

Figure 3.17. JEOL JBX 8100FS e-beam or Hiedelberg laser writer registration marks: (a) Location, and (b) dimensions of alignment mark.

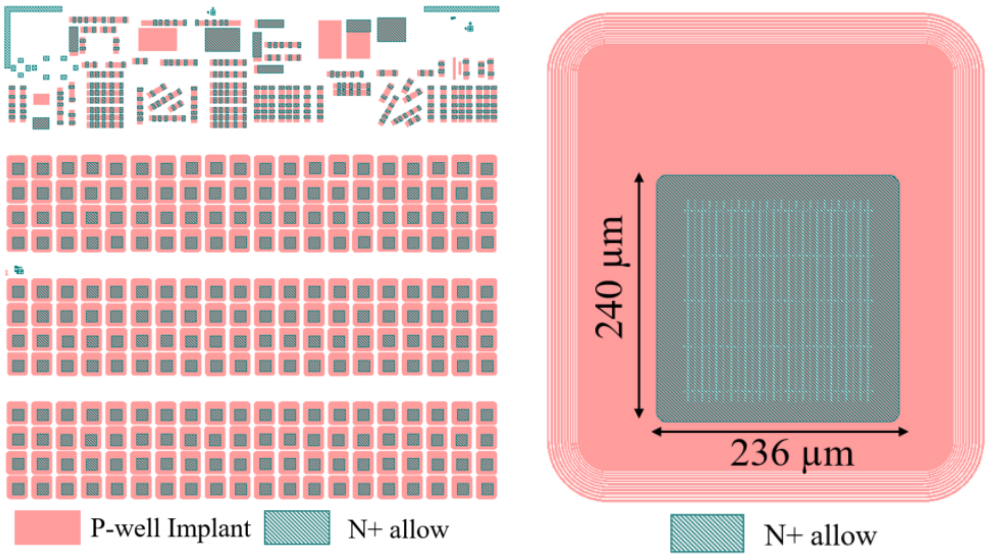


(a)



(b)

Figure 3.18. MJB 3 optical aligner registration mark: (a) Location and (b) dimensions of optical lithography alignment marks.



(a) (b)

Figure 3.19. Source implant mask: (a) Die level view, and (b) Device level view.

3.4.5 N+ Source Implant - Optical Lithography

Mask# 4

Layer# 21

Layer name: N+Allow (Pyxis) / N+_allow (KLayout)

Mask Type: Dark

Resist: AZ9260 (positive tone)

Description: The N-type source implantation is implemented in the active area by a self-aligned oxidized poly mask. But the source implant in the field and PCM areas is defined by this additional layer. A 8 – 10 µm thick AZ9260 mold is patterned to prevent the growth of electrodeposited Ni. Later, the resist is stripped and these previously resist coated areas allow source implantation, while the electroplated Ni blocks the implant outside the drawn regions.

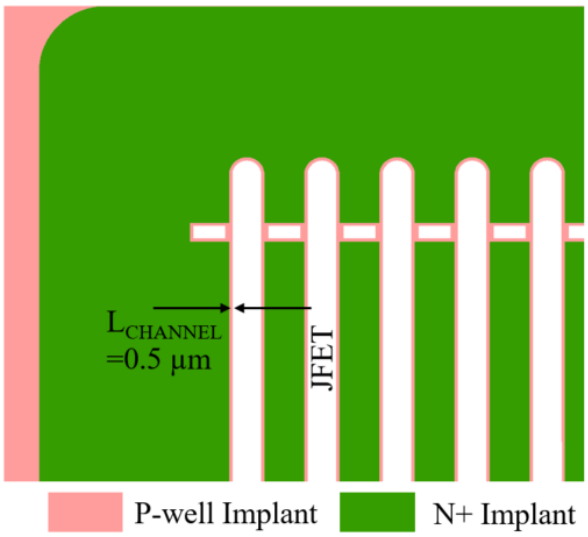


Figure 3.20. P-well and N-source implant in the tri-gate device showing the channel length.

3.4.6 P^+ Implant - E-beam Lithography

Mask# 5

Layer# 2031

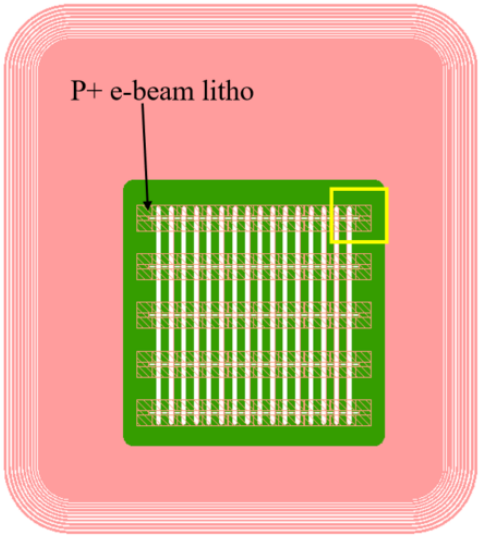
Layer name: PE_P+ (Pyxis) / P+_ebeam_block (KLayout)

Mask Type: Light

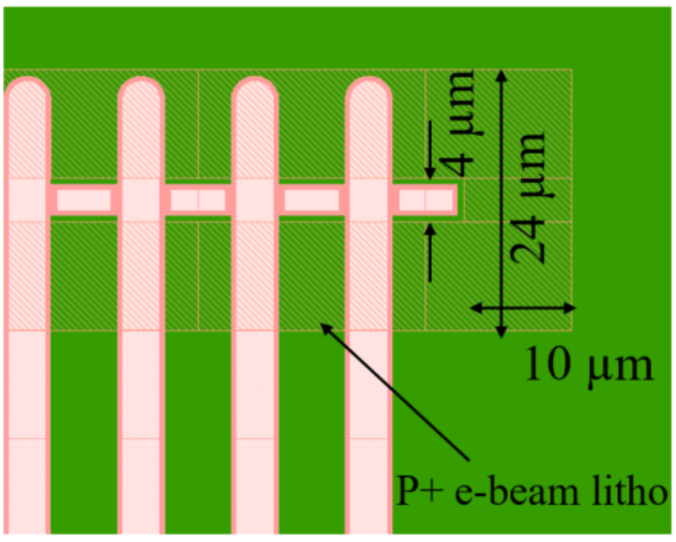
Resist: PMMA EL11 + 950 K PMMA A4/A6 (positive tone)

Description: The P^+ stripe windows are opened in this layer to allow a heavily doped p-type implantation to make contact to the p-well layer for improved dV/dt ruggedness. The critical dimension is at or below 4 µm in this level, and a dual lithography process was initially established. Later, with the availability of the optical mask-less aligner in the Birck facility, better alignment accuracy and critical dimension control become achievable, thus making a single step lithography possible. Both the dual- and single-step process mask layout information are provided below.

In the dual lithography process, this layer exposes the bi-layer e-beam resist in the drawn area to deposit 400-500 nm thick Ti/Ni metal stack in a lift-off process. The area not in the active region is defined by the next level of optical lithography.



(a)



(b)

Figure 3.21. P^+ implant e-beam lithography: **??** Device level view, and **??** Closer view with the dimension.

3.4.7 P^+ Implant - Optical Lithography

Mask# 6

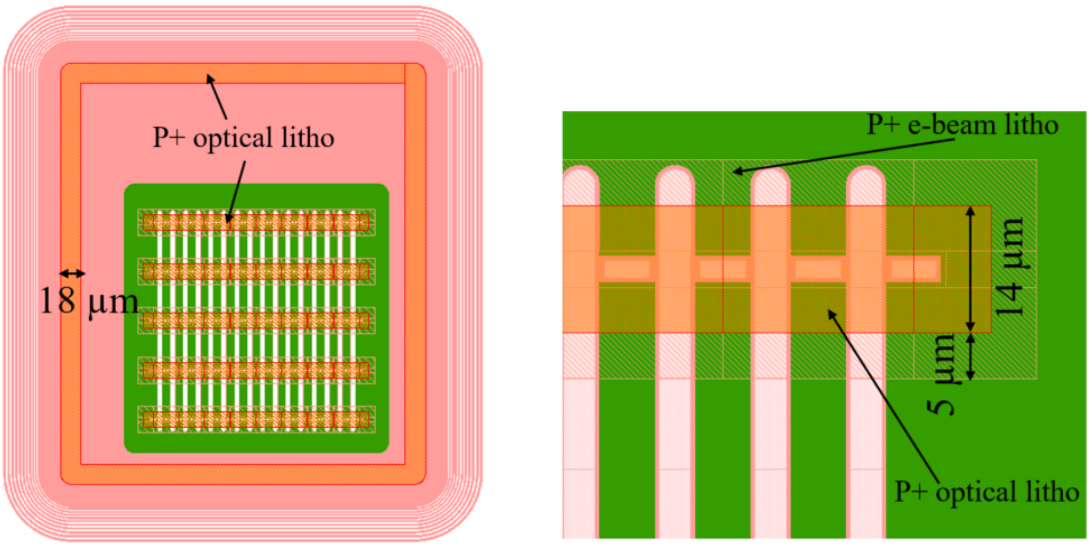
Layer# 2032

Layer name: PO_P+ (Pyxis) / P+_optical_allow (KLayout)

Mask Type: Dark

Resist: LOR3B + AZ1518 (positive tone)

Description: This layer is used to define the P^+ implantation ring around the active device, as well as features in the PCM module. The inverse of the drawn feature is exposed to deposit 400–500 nm of Ti/Ni metal stack to act as the implantation mask. The overlap between this and the previous layer is 5 µm.



(a) (b)

Figure 3.22. P^+ implant optical lithography: (a) Device level view, and (b) Closer view with the dimension.

3.4.8 Alternate P+ Implant - One-step Lithography Process

Layer# 15

Layer name: P+_oneLayer (Pyxis) / P+_OneStep_allow (KLayout)

Mask Type: Dark

Resist: LOR 3B + AZ1518 (positive tone)

Description: A critical dimension of ∼1 µm can be patterned using the maskless Heidelberg MLA-150 tool. Since the tool became available in the Birck center, the dual layer lithography process was collapsed into a single layer using a LOR3B and AZ1518 bilayer lift-off process.

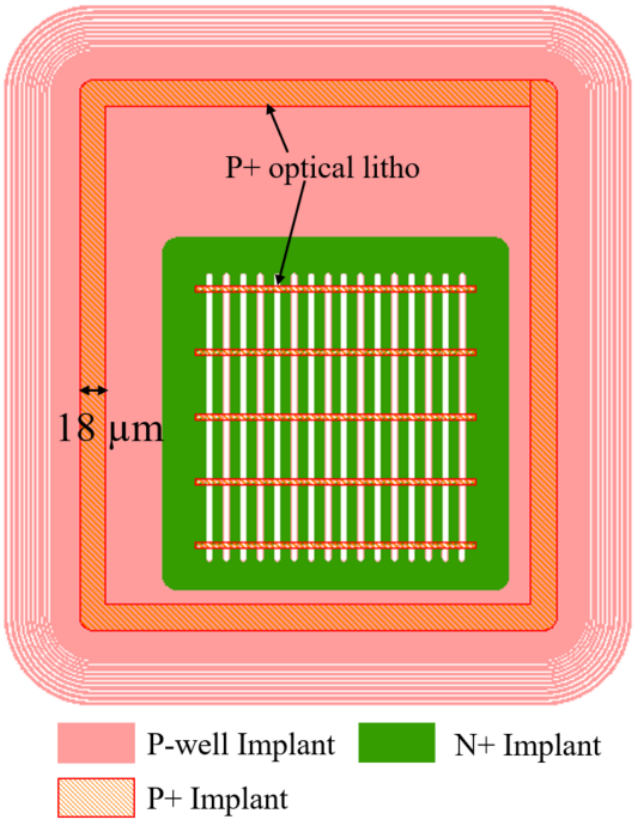


Figure 3.23. P^+ implant one step lithography in the Heidelberg maskless aligner.

3.4.9 Trench - E-beam Lithography

Mask# 7

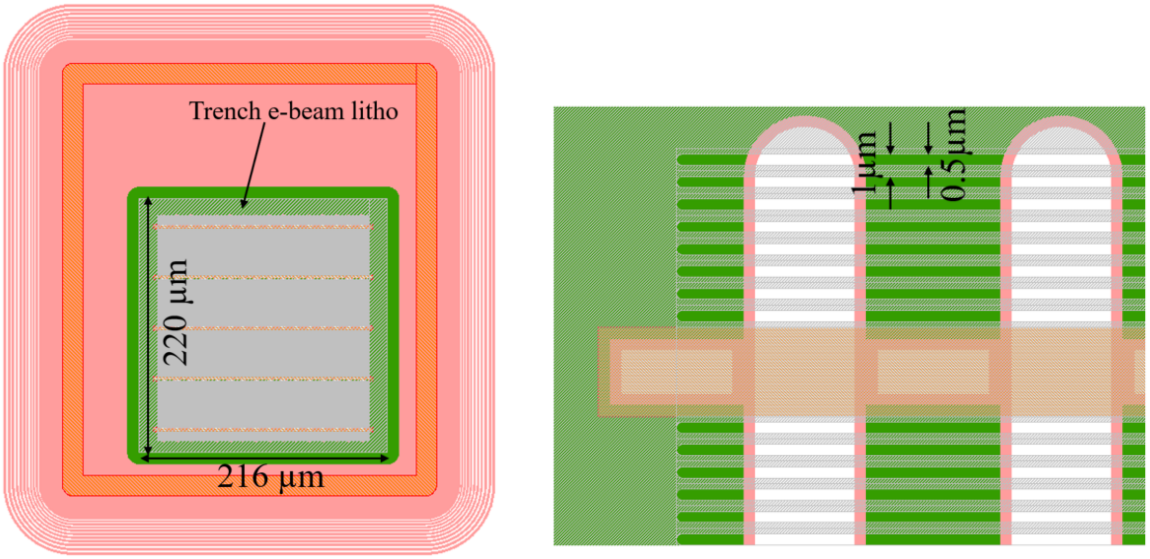
Layer# 2041

Layer name: PE_trench (Pyxis) / Trench_ebeam_block (KLayout)

Mask Type: Light

Resist: 950K PMMA A6/ CSAR-6200 (positive tone)

Description: The trench patterns in the active and PCM regions are defined by e-beam lithography because of the small critical dimension required (0.5 µm), and alignment accuracy. In this level, the drawn features are exposed with e-beam irradiation, and a 200 nm Ti/Ni metal stack is deposited in a lift-off process. The field area and some features in PCM region are patterned by optical lithography in the next level.



(a) (b)

Figure 3.24. Trench e-beam lithography: (a) Device level view, and (b) Closer view with dimensions.

3.4.10 Trench - Optical Lithography

Mask# 8

Layer# 2042

Layer name: PO_trench (Pyxis) / Trench_optical_allow (KLayout)

Mask Type: Light

Resist: AZ9260 (positive tone)

Description: An 8 – 10 µm thick AZ9260 resist is patterned to block the SiC etch in the field area and some features in the PCM region. A 5 µm of overlap is maintained between this layer and the previous e-beam lithographic layer. Later it was found that this overlap is not sufficient, as the resist reflows due to local heating during the etch process and affects the trench features in the active region. An increase in this dimension to 10 µm is recommended for future tri-gate processing. A significant aspect ratio dependent etch rate is also observed in this process. Wider windows etch faster than the 0.5 µm wide features in the active region. Despite this, only 4 tester devices in PCM region are affected. However, in the future, a 2-step etching process – one longer etch for the active area, and a second shorter etch for the field area - can be implemented to achieve a uniform etch depth across the wafer.

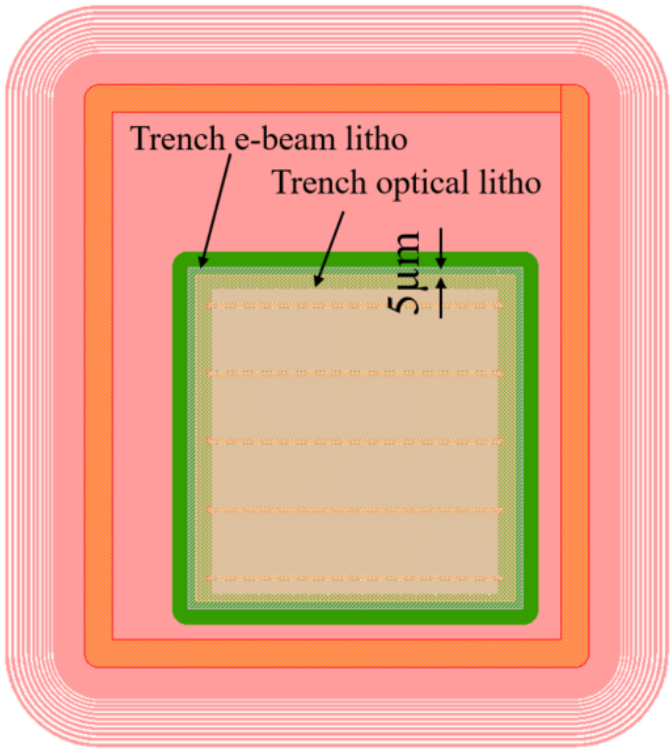


Figure 3.25. Trench optical lithography.

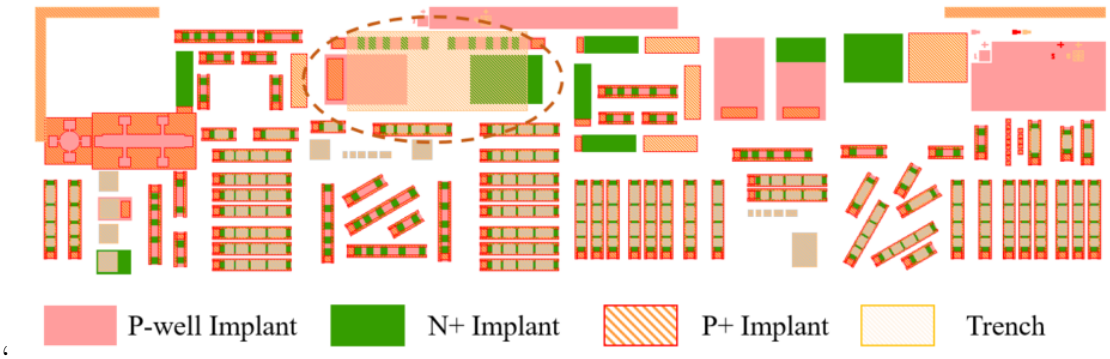


Figure 3.26. The marked region in the PCM region etches deeper compared to active area due to aspect ratio dependent etching.

3.4.11 Field Oxide - Optical Lithography

Mask# 9

Layer# 61

Layer name: FieldOxide_OP (Pyxis) / FOX_Etch_allow (KLayout)

Mask Type: Light

Resist: AZ9260 (positive tone)

Description: This layer is used to etch the 1 µm deposited field oxide in the contact region in both active and PCM areas. The layer also features opening of the resist in the alignment mark area to clear the oxide for ensuring high alignment accuracy. The windows is 10 µm inset of the source implant, creating a large window in the active region and a 5 µm wide inset window in the P^+ stripe contact ring.

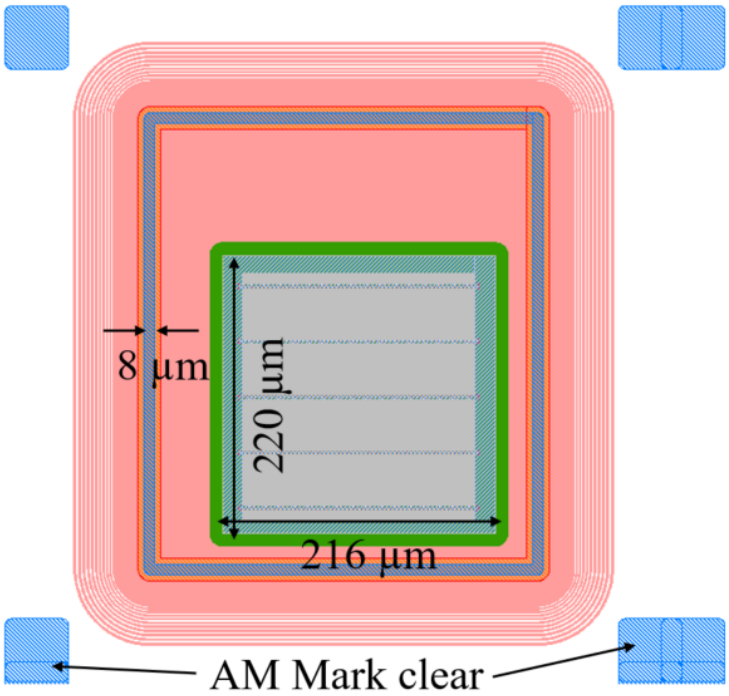


Figure 3.27. Field oxide optical lithography - blue shaded regions are opened in resist mask to allow a wet chemical oxide etch.

3.4.12 Gate - E-beam Lithography

Mask# 10

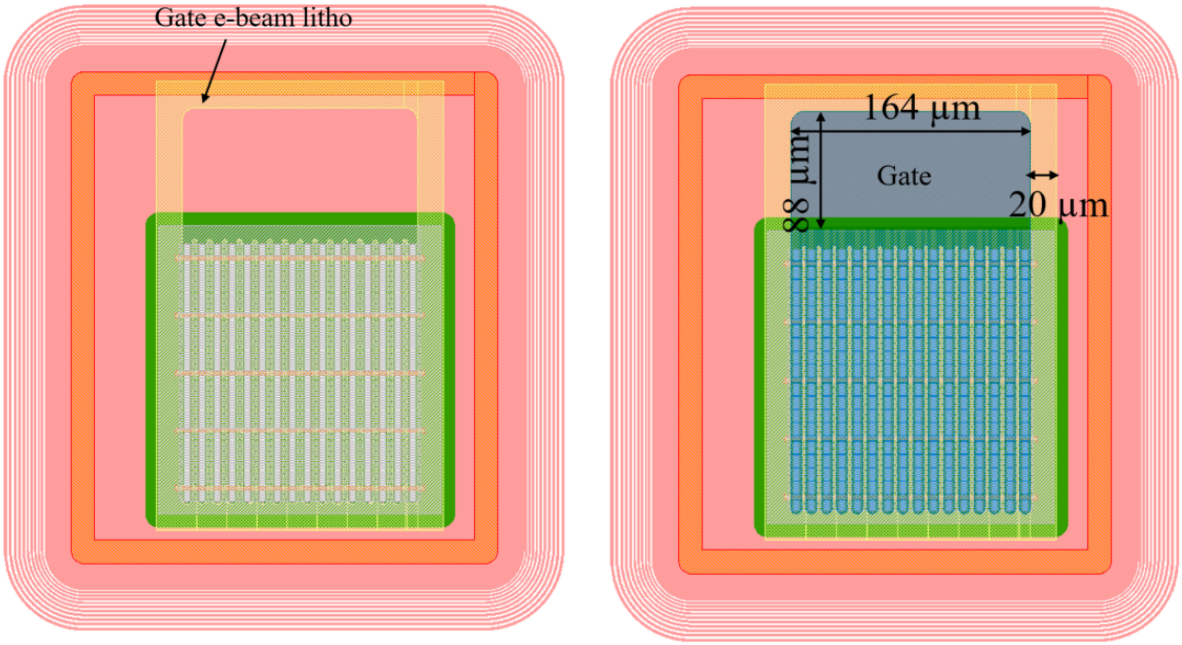
Layer# 53

Layer name: Gate_ebeam (Pyxis) / Gate_ebeam_posResist (KLayout)

Mask Type: Light

Resist: CSAR-6200 (positive tone)

Description: The gate patterning is split into a dual lithography process: first, an e-beam lithography and etch, and second an optical lithography and etch. The critical dimension of this layer is large enough to perform using either a high current e-beam exposure or a maskless Heidelberg MLA-150 optical lithography. However, neither of the process provide better than 0.3 µm of alignment accuracy, which only be achieved in a low current (30 nA or below) e-beam exposure of CSAR resist. The yellow shaded area in Fig. 3.28(a) is exposed in the e-beam lithography to open windows in the 1 µm thick doped polysilicon layer. A polysilicon etch follows, which results in a feature shown in blue in Fig. 3.28(b) inside the yellow drawn boundary. The polysilicon beyond the yellow boundary in the field area, and patterns in the PCM region are etched in the next level using optical lithography.



(a) (b)

Figure 3.28. Gate e-beam lithography: (a) The yellow region is exposed and opened in the resist mask to etch polysilicon mask, and (b) The blue polysilicon gate pattern results after the etch with the yellow shaded mask inside the boudary of the mask.

3.4.13 Gate - Optical Lithography

Mask# 11

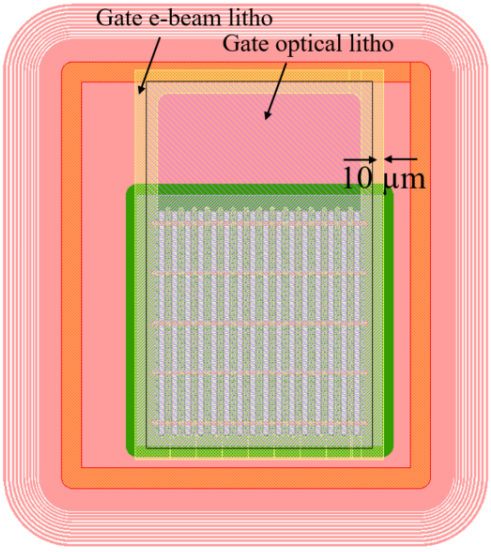
Layer# 2053

Layer name: PO_GateMask (Pyxis) / Gate_Etch_block_optical (KLayout)

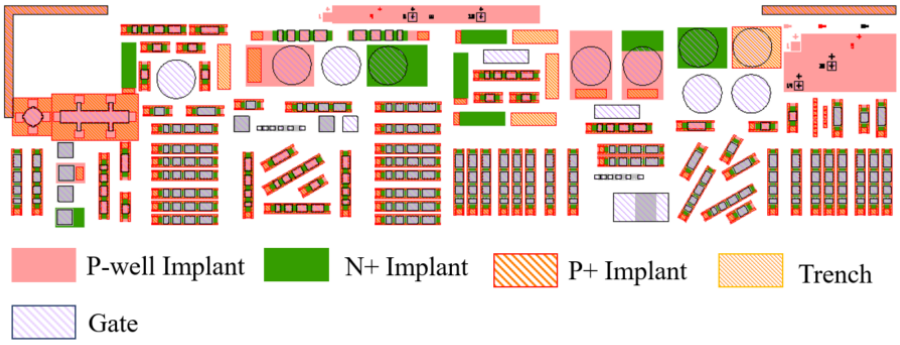
Mask Type: Dark

Resist: AZ9260 / AZ1518

Description: The inverse of the drawn features are exposed using optical lithography tool to protect the active area, which is already patterned and etched in the previous layer. At the same time, it also defines the gate patterns in the PCM region. A 10 µm overlap is used between this layer and the previous layer.



(a)



(b)

Figure 3.29. Gate optical lithography: (a) The active device area- the drawn area protecting the underneath layer and exposed polysilicon is etched, and (b) PCM region with poly gate mask defined.

3.4.14 Ohmic - Optical Lithography

Mask# 12

Layer# 81

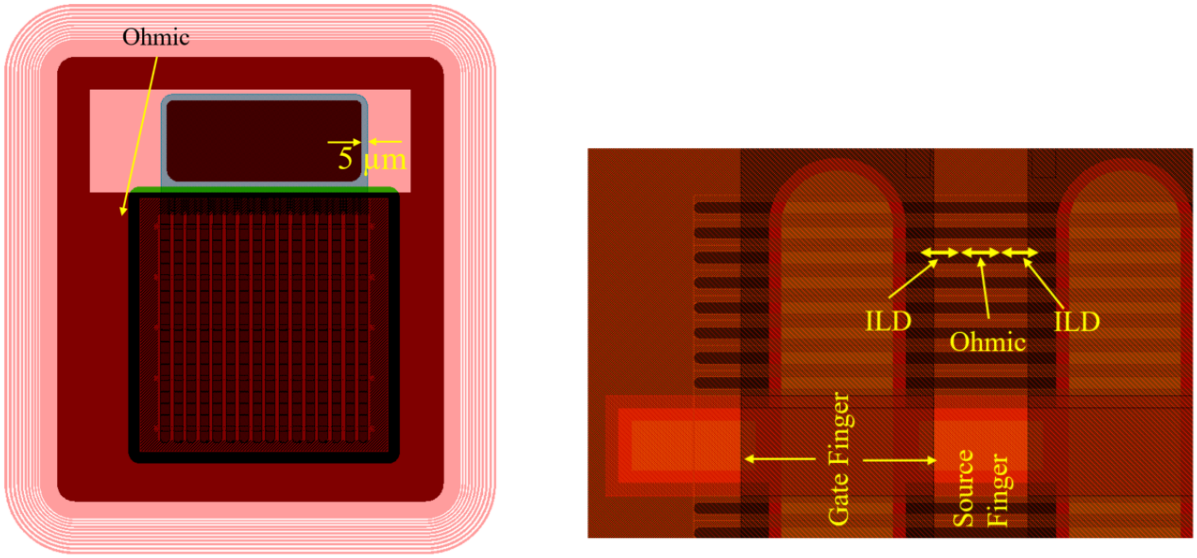
Layer name: Ohmic (Pyxis) / Ohmic (KLayout)

Mask Type: Light

Resist: LOR 3B + AZ1518 (positive tone)

Description: This layer is used to deposit an ohmic metal layer of nickel in a lift-off process.

The drawn area is exposed to open windows in the bi-layer resist for metal deposition. It should be noted that the drawn features in this gate pattern are not required if a gate silicidation process is not performed. The original design foresaw using the same silicide process for the gate contacts as for the SiC ohmic contacts. However, it was later decided not to use the polysilicon silicidation process, and this metal feature was thus placed on top of a 1 µm thick interlayer dielectric which does not react with nickel during the annealing process. Therefore the ohmic window feature on the gate pad can be omitted in the future. The ohmic layer is 5 µm inset of the gate pattern, and produces either 1 or 3 µm of source contact length in the active region.



(a) (b)

Figure 3.30. Ohmic optical lithography: (a) The device view - in the red highlighted regions the lifted off metal is annealed, and (b) Closer view of the region where ohmic contacts are formed.

3.4.15 ILD Etch - Optical Lithography

Mask# 13

Layer# 71

Layer name: GateContact (Pyxis) / ILD_etch_allow (KLayout)

Mask Type: Light

Resist: AZ9260 (positive tone)

Description: This layer is used to open a window in the gate pad region both in the active and PCM areas. Later, the top metal deposition produces a contact and a pad for gate probing or bonding. In the tri-gate device, the 10 µm wide ILD window is 15 µm inside of the gate pattern. The pattern is placed asymmetrically in the lower side of the gate pad so that probes can be placed in the upper area to prevent any unwanted mechanical damage.

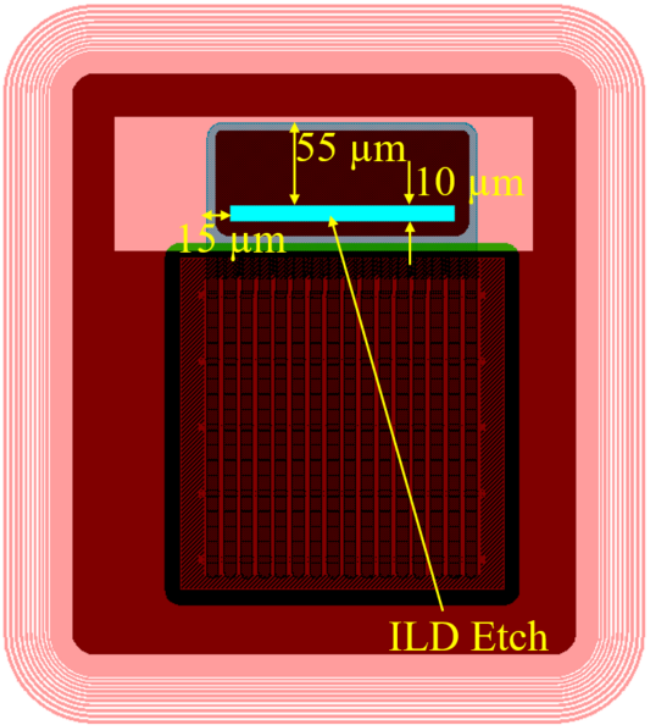


Figure 3.31. Inter Layer Dielectric (ILD) optical lithography - blue shaded region is opened in resist mask to allow a dry oxide etch.

3.4.16 Top Metal - Optical Lithography

Mask# 14

Layer# 91

Layer name: TopMetal (Pyxis) / TopMetal (KLayout)

Mask Type: Dark

Resist: AZ9260 (positive tone)

Description: This layer is used to open windows to etch a sputtered Ti/Au top metal film. A 6–10 µm thick AZ9260 is patterned for a wet etch mask in the contact areas both in the active and PCM regions.

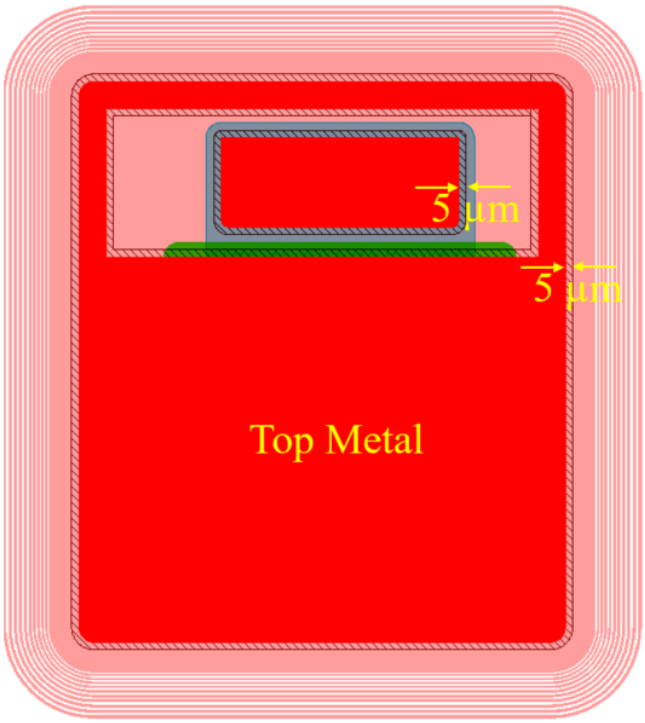


Figure 3.32. Top metal optical lithography - Red highlighted areas are the unopened regions in the resist mask used in the Ti/Au metal etch process.

This concludes the detailed description of the mask layout design of the tri-gate Gen-1 and Gen-2 devices. In the following chapter, a detailed description of the fabrication and processing flows which use this mask set will be presented.

4. TRI-GATE PROCESS TECHNOLOGY

The tri-gate SiC MOSFET, due to its structural innovation, produces an increased current density in the device without requiring a higher mobility at the semiconductor - dielectric interface. Thus it provides an alternative solution to a long-endured interface quality issue, and could have a widespread impact on the expansion of SiC power devices into the low to medium voltage market. However, the deep trenches associated with this novel device impose significant fabrication complexity. The challenges include high energy implantation and masking, high aspect ratio SiC etching, polysilicon gate planarization and patterning, etc. The major steps in the tri-gate device fabrication technology are shown in Fig. 4.1.

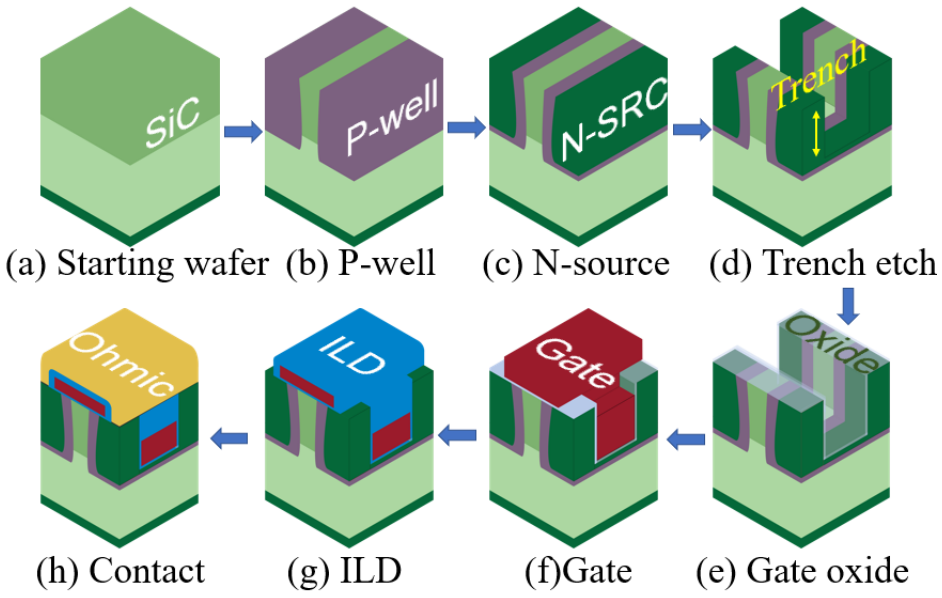


Figure 4.1. Major fabrication steps in the tri-gate device fabrication technology

The fabrication process is strategically divided into unit process steps, and each unit process is established by varying the associated parameters in an iterative fashion until the desired performance is achieved. In this chapter, detailed descriptions of the individual process recipe development are provided, and the integration of these unit steps into a unified tri-gate 4H-SiC MOSFET fabrication process will be discussed. Tri-gate devices were fabricated on diced quarters of 4″ (∼100 mm) production-grade 4° off-cut 4H-SiC wafers, purchased from Cree, Inc. The drift and current spreading layers (CSL) were grown

epitaxially, also by Cree. Two different drift layer thicknesses of 8.4 and 5.2 µm were used, both doped n-type, with nitrogen concentrations of 1×10^{16} cm^{-3} and 1.4×10^{16} cm^{-3}, respectively. These two structures are designed for parallel plane blocking voltages of 1300 and 900 V, corresponding to datasheet operating voltages of 900 and 650 V, respectively. This assumes a 30% derating factor to account for imperfect edge termination. On top of the drift layer, a 3.2 µm CSL has been included to reduce JFET region resistances. In some samples, CSL layer has been thinned to 2.6 µm for 2 µm trench devices to accommodate improved junction shielding in the off state. This will be discussed in more detail in the subsequent section. The complete list of processed Gen-1 tri-gate samples is given in Table 4.1. Each sample has been given a short name inscribed on the back (C-face) side by a diamond scriber for quick recognition.

Table 4.1. Tri-gate Gen-1 sample information

Wafer #	Manufacturer #	Drift layer thickness (µm)	CSL thickness (µm)	Short Name
PU 391	NE0256-28	8.3	3.1	1Q3
PU 397	GY1672-17	5.2	3.2	2Q4
PU 393	NE0256-30	8.5	2.5	3Q2
PU 399	NE0256-06	5.4	2.6	4Q2

4.1 Implantation – P-well

Gen-1 tri-gate devices were planned to include 2 µm deep trench fingers perpendicular to the gate or JFET fingers. This reveals the sidewall, in addition to top and bottom surfaces, for added current conduction without increasing the cell pitch. This reduces the channel specific on-resistance of the device. To accommodate the channel on all sides, the p-type base and n-type source implantation junctions must be deeper than the trench. An implantation profile for the p-type aluminum (Al) implanted base region was designed with a base-drift junction depth of 2.7 µm. The design includes 14 individual energies up to a maximum of 4.25 MeV. This multi-energy implant schedule has been developed using the analytical doping model described in [30], which has proven very accurate over a wide range of implant energies at room temperature. The design utilizes a retrograde profile, allowing the channel

to have a sufficiently low surface doping of $\sim 2 \times 10^{17}$ cm^{-3} to provide a low threshold voltage while providing adequate punch-through protection with a higher dose under the channel region. This has been accomplished with uniform doping through and below the fin, followed by a single energy deep implant of higher (2×10^{18} cm^{-3}) peak concentration as a punch-through block as shown in Fig. 4.2. The energy and dose information is provided in Table 4.2.

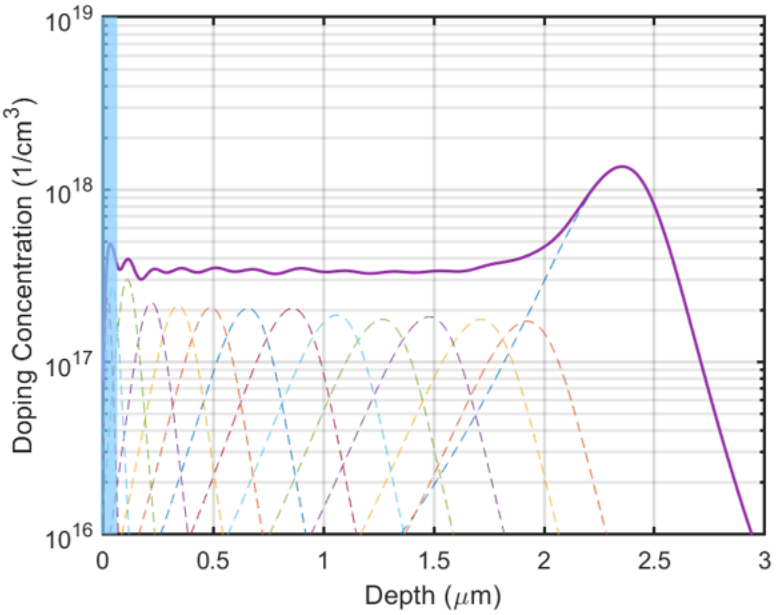


Figure 4.2. Aluminum p-well implant profile. The dashed line shows implanted concentration at each energy, and solid line shows the total implant concentration. The blue region indicates the screen oxide thickness used during the implant

Table 4.2. Gen-1 tri-gate – p-well aluminum implant profile

Energy (keV)	Dose (#/cm^2) $\times 10^{12}$
4248	60.0
3000	7.32
2500	7.32
2000	7.32
1600	6.80
1250	6.80
950	6.80
680	5.95
480	5.10
320	4.25
200	3.40
100	3.00
40	1.50
20	0.80

An LPCVD (Low Pressure Chemical Vapor Deposition) grown polysilicon layer was used as the p-well implant mask. The sample was first cleaned using a modified RCA process [31], and 30 nm of thermally grown oxide was formed at 1050°C. This oxide serves 3 purposes – (i) it acts as an etch stop during polysilicon etching, (ii) it prevents potential contamination to SiC surface during the implant process, and (iii) it absorbs the low energy doping tail near the surface. This screen oxide is shown as a blue shaded region in Fig. 4.2 without accounting for any ion scattering into the oxide. On top of this thin screening oxide, a 5.8 µm thick polysilicon layer was grown which acts as the implant mask during the process. The high energy Al implant also defines the floated field ring (FFR) regions for device edge termination, with a minimum line width of 1 µm. This low dimension lithography was not possible using optical lithography in the Birck Nanotechnology Center, so electron beam lithography was used to define the FFR and JFET regions. However, the throughput of standard PMMA or HSQ based e-beam resist is low, even at elevated beam currents (∼100 nA) in the Joel e-beam lithography system available in the Birck Center. Therefore two alternative schemes can be followed to face this challenge. In scheme 1, the FFR ring and JFET fingers are defined by negative tone FOX-16 HSQ based e-beam resist, while field area and the process control module (PCM) regions are defined by regular optical positive tone AZ9260 resist. In

scheme 2, all features are defined using high sensitivity All Resist CSAR-62 resist using e-beam lithography. The dose needed for CSAR-62 resist is approximately 5 times lower than PMMA or HSQ based resists which makes the exposure 5 times faster at a given current. Details of both process schemes are discussed below.

In scheme 1, the deposited polysilicon was oxidized to form a 200 nm film of SiO_2. Windows around the device active area, PCM, and alignment mark regions were opened in the oxide using photolithography and wet etching in a buffered oxide etch (BOE) solution. In order to align the subsequent e-beam lithography step, alignment marks were etched ∼1 µm in the polysilicon layer. This reduces the polysilicon implant mask thickness to ∼4.8 µm in the active area. According to Monte-Carlo simulations performed using TRIM [32], this thickness of polysilicon is sufficient to block the 4.25 MeV aluminum implant. The alignment mark etch step was done in an STS ASE ICP-RIE etcher using the Bosch process, with SF_6/O_2 as an etch species and C_4F_8 as a polymer deposition species. The detailed recipe is given in Table 4.3.

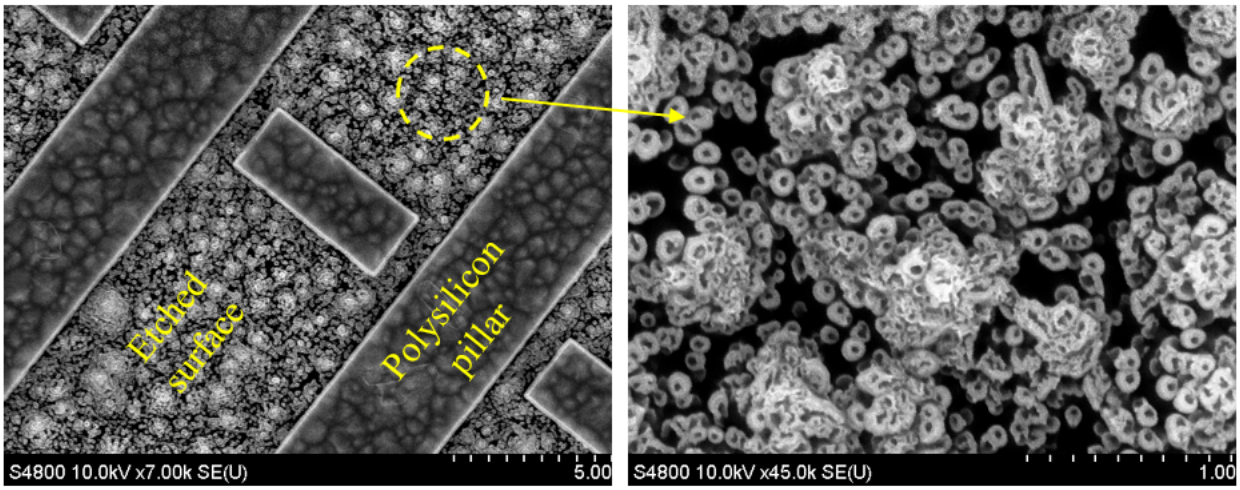
Table 4.3. Polysilicon etch recipe in the STS ASE ICP-RIE etcher

Parameter	Etch			Deposit
Gas (sccm)	SF_6/O_2 (130/13)			C_4F_8 (100)
ICP power (W)	500			600
Bias power (W)	20			0
Pressure (mT)	18			18
Cycle (sec)	5			5
	Si	SiC	SiO_2	PR/CSAR
Etch rate (nm/min)	700	19	< 22	< 44

This etch was followed by an e-beam lithography step that forms the JFET and FFR regions. Negative tone HSQ-based FOX-16 from Dow Corning is used as the e-beam resist. This is an inorganic compound composed of $[HSiO_{3/2}]_n$ clusters. Under electron irradiation, the material converts to SiO_2, thus resulting in an all-oxide mask for the polysilicon etch. The resist was handled with an appropriate plastic container and a plastic pipette to avoid contamination and resist crystallization. The resist was spun at 2000 rpm for 60 sec and soft baked at 120°C for 3 min. The resist was then exposed with a 900–1100 µC/cm^2 dose in a

Vistec VB6 e-beam lithography system at 100 kV and ∼100 nA current. The exposed resist was developed in a 25% TMAH based solution for 2 min. This resulted in a 600 nm thick SiO_2 patterned layer defined by e-beam lithography. The oxide-masked polysilicon was then etched in the STS ASE Bosch process ICP-RIE system in the same way the alignment mark was etched. The sample was mounted on a 6″ Si carrier wafer with crystal bond during the etch.

Instead of SF_6, a Cl_2 based plasma etch was also attempted for the polysilicon etch in an E-620 Panasonic etcher at 175 W ICP power, 50 W bias power with 100 sccm Cl_2 under 1.5 Pa of pressure. A Cl_2 based plasma etches silicon anisotropically, but the byproduct of the etch is mainly $SiCl_4$, which has a boiling point of 57.4°C [33]. This results in a relatively low vapor pressure and inefficient byproduct removal. The etch is therefore dominated by Cl_2 ion bombardment, which is desirable for anisotropic etching. However, the etch byproduct $SiCl_x$ has a high sticking coefficient on the surface which makes desorption difficult. Moreover, any pre-existent O_2 molecules in the chamber can oxidize the surface and act as an etch mask. These effects result in non-uniform polysilicon etching and micro-masking [34], [35]. The effect of micro-masking is reduced or eliminated if the etch is done in multiple short duration etch steps (∼30 sec).



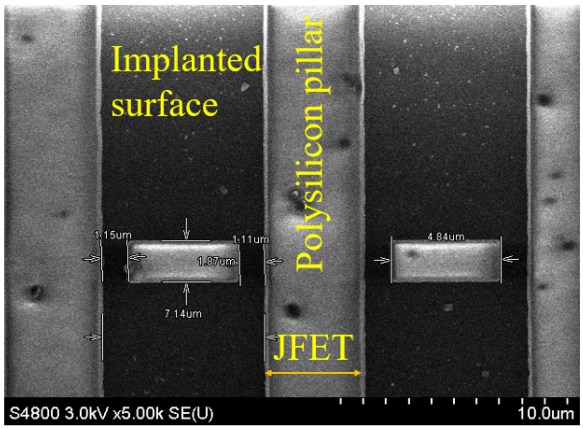
(a) Polysilicon etched in Cl_2 based plasma

(b) The effect of excessive passivation on surface

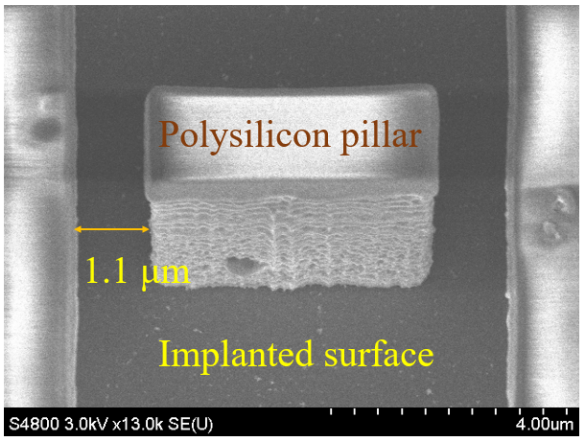
Figure 4.3. Polysilicon etch in Cl_2 plasma produces excessive surface passivation resulting in micro-masking.

We found the polysilicon etch in a Cl_2 plasma to be highly uncontrollable, so the process was changed to use SF_6. In an SF_6 based process, the main etch byproduct is SiF_4 which exhibits a very low boiling point of about -87°C [33], making it highly volatile. This results in an almost isotropic polysilicon etch, while a highly anisotropic etch is required. This challenge can be resolved by using the Bosch process, where a polymer is deposited for a specific time to protect the sidewall, followed by an SF_6 etch for a specific time, with this cycle repeated until the desired etch depth is achieved. The etch recipe is listed in Table 4.3.

Using the Bosch process, a very high polysilicon etch rate with good selectivity to both oxide and resist can be achieved. However, the multi-step etch and deposition process produces a rough sidewall with some mask undercut. The undercut has been observed to increase in samples mounted on SiO_2 coated wafers compared with those mounted on bare Si carrier wafers. The polysilicon etch rate also nearly doubles when the sample is mounted on an oxide coated carrier wafer. Both the extent of the undercut and the etch rate increase with the reduction in loading, since the SiO_2 carrier wafer etches much more slowly than a bare Si wafer. Therefore, it is recommended to use bare Si carrier wafers using a proper thermally conductive bonding material (e.g. Crystal Bond or Santovac oil) to obtain a more controllable etch rate and to minimize mask undercut. The polysilicon etch rate in the STS ASE ICP-RIE was also found to be highly dependent on tool condition. It has been observed that the etch rate gradually drops with system use to below 400 nm/min, and that performing a mechanical cleaning of the chamber restores the original etch rate. Figure 4.4 shows an SEM image of an etched polysilicon pillar, demonstrating a highly anisotropic etch with minimal mask undercut. The inherent sidewall roughness of the cyclic Bosch process is also apparent. The process flow of scheme 1 is illustrated in Fig. 4.5.



(a)



(b)

Figure 4.4. SEM image of polysilicon patterned as a mask for the p-well implant process: (a) Top view, and (b) Tilted view.

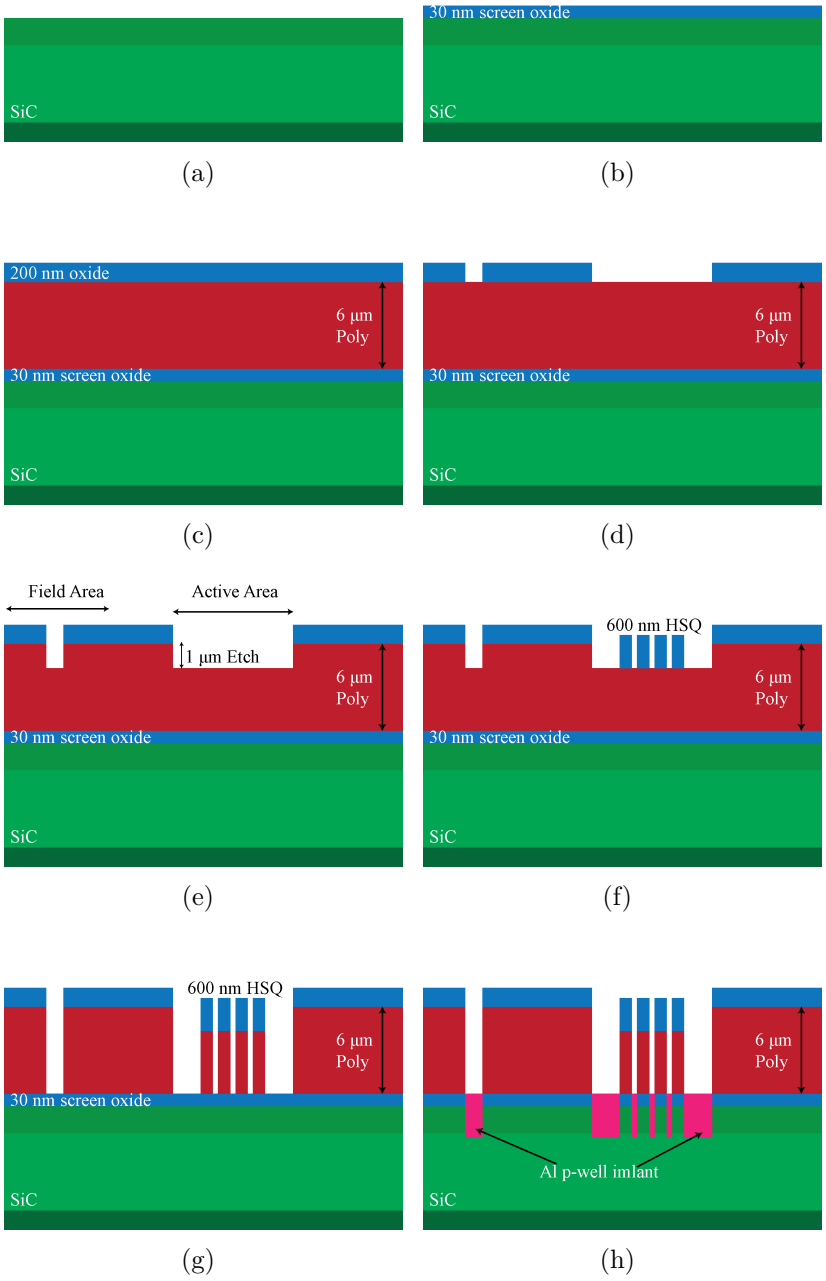


Figure 4.5. Aluminum p-well implant process flow - scheme 1: (a) SiC substrate and epi; (b) Screen oxide growth; (c) Polysilicon deposition and oxide mask growth; (d) Oxide mask pattern; (e) 1 (µm) Polysilicon alignment mark etch; (f) HSQ e-beam resist pattern; (g) Polysilicon etch, and (h) Aluminum p-well implant.

In scheme 2, an all e-beam defined resist-based polysilicon etch mask was implemented. This scheme eliminates oxide deposition and the two step lithography process as described above in scheme 1. A highly sensitive and high contrast e-beam resist from Allresist (AR-P 6200) was used. Due to its high sensitivity, the dose required is 5 times lower than that for HSQ-based FOX-16 resist, which improves the throughput proportionally. This enables a simple and efficient single step e-beam lithography process. This also eliminates the 1 µm of extra polysilicon required for alignment of the two step process. This scheme is implemented on the Gen-2 tri-gate samples to define the JFET fingers. In this scheme, a 5 µm thick polysilicon was first deposited, followed by an e-beam lithography step. A resist (AR-P 6200 CSAR) was spun on the sample at 4000 rpm for 60 sec. This resulted in a 400–450 nm thick resist layer after soft baking at 150°C for 3 min. The resist was then exposed in a JEOL JBX-8100 FS lithography system at an accelerating voltage of 100 kV and a beam current of 100 nA, with a dose of 280–310 µC/cm^2. After exposure, the resist was developed in Xylene for 70 sec, followed by a 60 sec rinse in IPA. The sample was then directly loaded on a 6″ Si carrier wafer with crystal bond, and loaded into an STS ASE etcher. The polysilicon etch was performed in the same way as described in the scheme 1 section. The etch parameters are listed in Table 4.3. The process flow of scheme 2 for completing the p-well implantation is shown in Fig. 4.6.

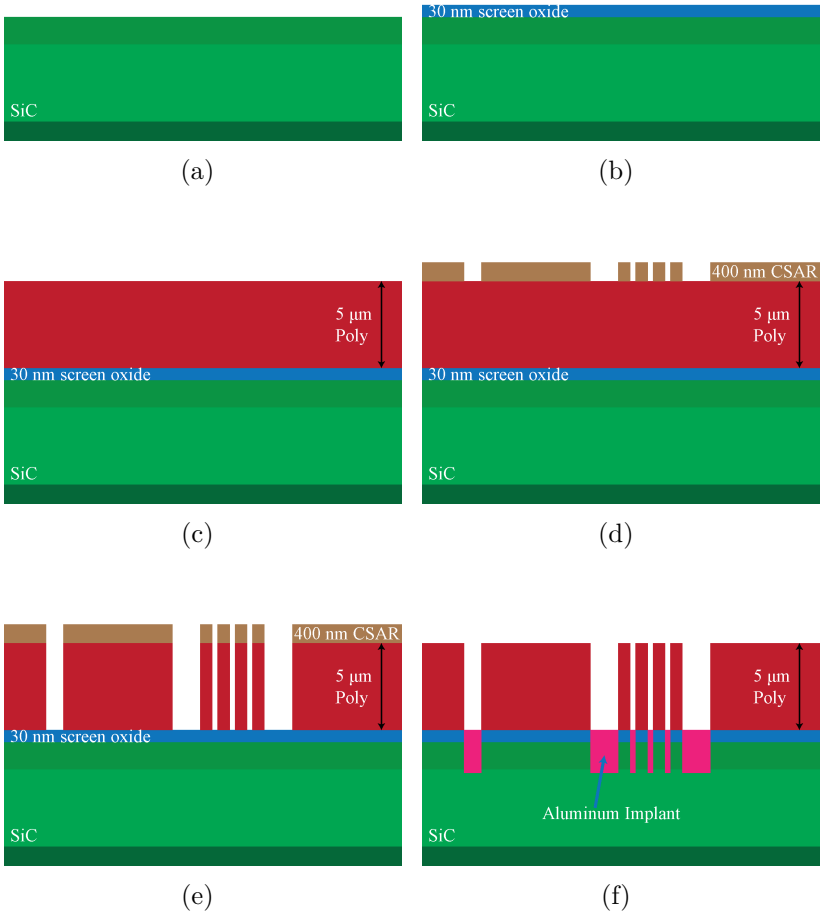
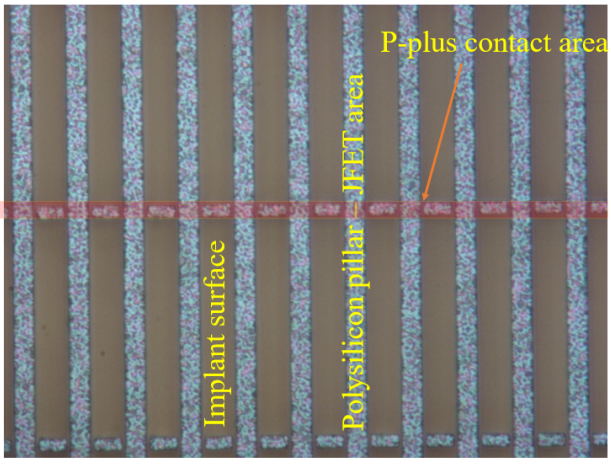
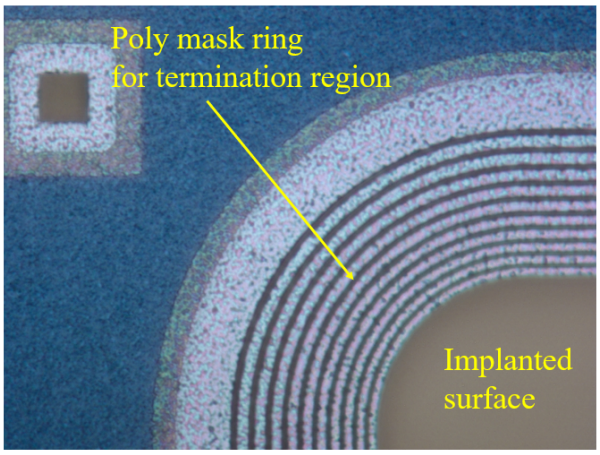


Figure 4.6. Aluminum p-well implant process flow - scheme 2: (a) SiC substrate and epi; (b) Screen oxide growth; (c) Polysilicon deposition; (d) E-beam CSAR resist pattern; (e) Polysilicon etch, and; (f) Aluminum p-well implant.



(a)



(b)

Figure 4.7. Optical images of the patterned polysilicon implant mask in (a) the active region, and (b) the termination region.

After the definition of the polysilicon mask, the Gen-1 tri-gate samples were loaded on a 5″ Si carrier wafer using carbon tape. The loaded wafer was sent to an outside commercial service provider for implantation, which was done in two steps. In step 1, high energy implants from 680–4248 keV were performed at Ion Beam Services (IBS), while in step 2, the shallow implant energies from 20–480 keV were performed at CuttingEdge Ions. All implantations were done at room temperature, with 0° tilt and twist angles.

4.2 Implantation – Source

After completion of the high energy aluminum implant, the source implantation process was pursued. The source implantation profile was also designed using the parameters provided in [30]. This is a multi-energy implant schedule of nitrogen with a target junction depth of 2.2 µm, which extends below the trench by 200 nm. The profile was carefully designed to have sufficiently high concentration to (i) counter-dope the p-well implant, (ii) provide sufficiently low resistivity to minimize source spreading resistance, and (iii) be sufficiently high concentration to provide a low contact resistance. According to [4], to obtain contact resistivity below $10^{-6}\ \Omega \cdot \text{cm}^2$ requires a source doping of approximately $2 \times 10^{19}\ \text{cm}^{-3}$. However, to achieve this and maintain the target junction depth, a box profile of the implant would require a dose of $4.4 \times 10^{15}\ \ \text{cm}^{-2}$, which exceeds the amorphization limit for room temperature implants [4]. To avoid this problem, a heated stage implantation was necessary, but no MeV implant supplier was located with this capability. Therefore, two adjustments were made to the profile. First, a shallow high dose box profile with a nominal concentration of $2.5 \times 10^{19}\ \text{cm}^{-3}$ was used to provide sufficiently low contact resistance. The dose and depth of this shallow profile are $9 \times 10^{14}\ \text{cm}^{-2}$ and 500 nm respectively. This was done at CuttingEdge Ions using a hot stage at 500°C. Secondly, the deeper implants with energies up to 3 MeV and a dose of $6.2 \times 10^{14}\ \text{cm}^{-2}$ were performed at room temperature at mi-2 GmbH. The combination of these implants keep the total dose below the amorphization limit, and still provide a shallow region with a sufficiently high concentration for low–resistance ohmic contacts. The nitrogen implantation profile of the source regions is shown in Fig. 4.8, with individual implant energies and doses provided in Table 4.4. The net implantation profile designed for the Gen-1 tri-gate devices is shown in Fig. 4.9, including the p-well and n-source

implant profiles, and the 1×10^{17} cm^{-3} doped CSL background. Figure 4.10 shows the SIMS analysis of the implantation performed on a test sample which was implanted along with the tri-gate samples, before the lower energy nitrogen implants. It shows good correspondence with the designed profile as shown in the dotted line. It also shows the extent of the p-well and n-source implants beyond the target 2 µm trench etch depth. However, the tail of the source implant falls less rapidly, and the deepest p-well implant peak is slightly shallower than the designed profile. This makes the p-well region narrower than designed, resulting in the total dose of 2.9×10^{13} cm^{-2}, a factor of 1.5 less than the designed profile. However, the resulting total dose is still about 2 times higher than the minimum dose required to prevent the p-well region punch-through.

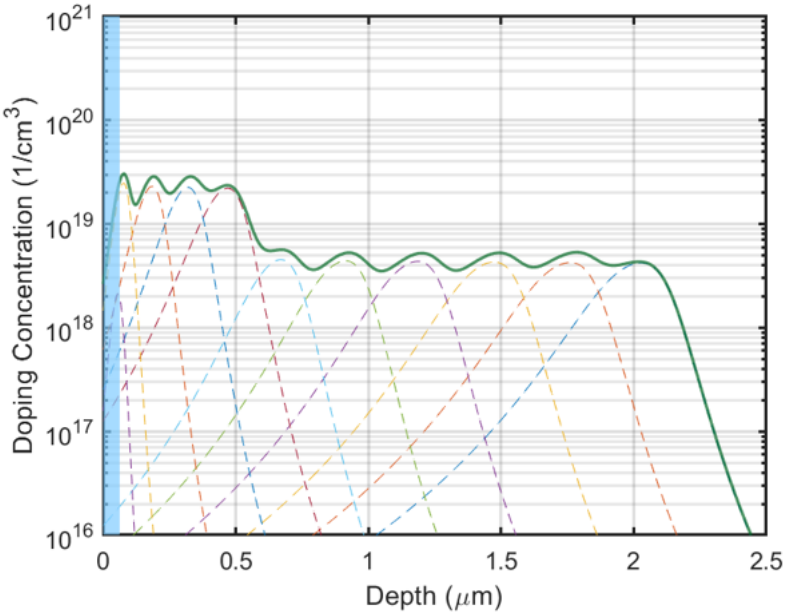


Figure 4.8. Nitrogen n-source implant profile. The dashed line shows the implanted dopant concentration at each energy, while the solid line shows the total concentration. The blue region near the surface indicates the screen oxide thickness present during the implantation process

Table 4.4. Gen-1 tri-gate – n-source nitrogen implant profile

Energy (keV)	Dose (#/cm^2) $\times 10^{14}$
3009.5	1.35
2412	1.32
1840	1.28
1336	1.22
923	1.13
604.5	1.02
380	4.19
235	3.49
123	2.63
47	1.53
33	0.10

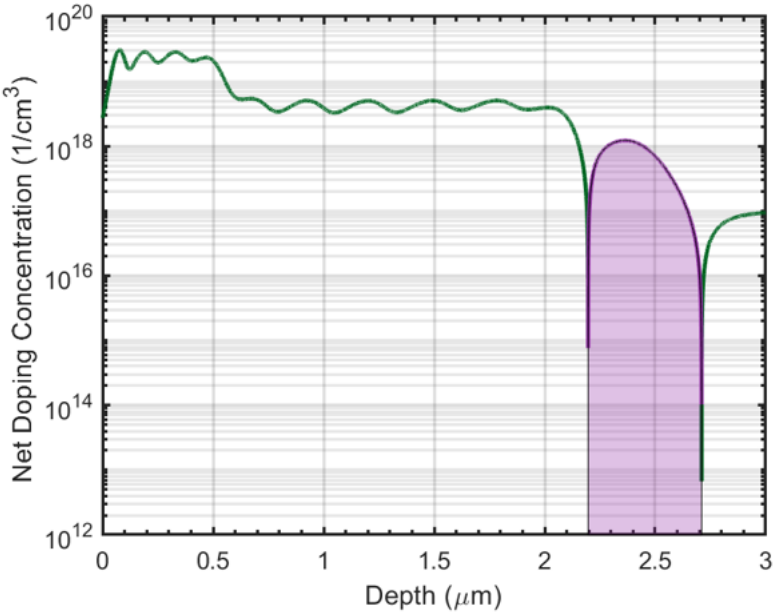


Figure 4.9. Net implantation profile from the analytical model. Shaded region highlights the designed dose in the p-well area

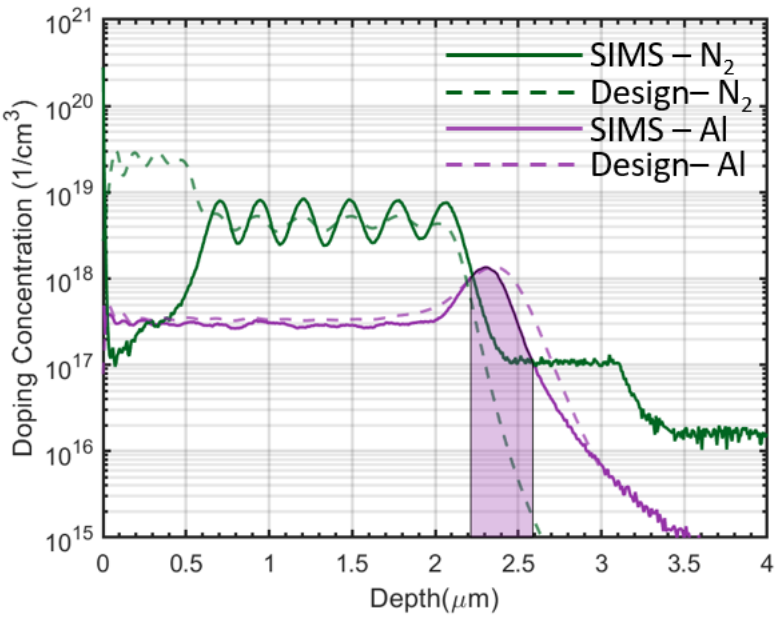


Figure 4.10. SIMS analysis on a test sample is shown in the solid line. The dashed line shows the designed profile. The shaded region shows the obtained dose in p-well region

According to a TRIM [32] Monte-Carlo simulation, a 3.4 µm of polysilicon layer is needed to block the highest N implant energy (3 MeV). This confirmed that the existing 5-6 µm polysilicon pillar on the sample was sufficient to block the source implant. To define the channel region, the polysilicon base implant mask was first oxidized 1.0 µm, expanding the mask laterally by 0.5 µm. In this way we formed a 0.5 µm long channel in a self-aligned way with no lithographic alignment tolerance. The oxidation was done in a wet pyrogenic furnace at 1050°C and atmospheric pressure. The vertical oxide growth rate was found to be higher than the lateral rate. This asymmetry in oxidation rates is possibly due to non-uniform source vapor transport around highly anisotropic features. The growth rate in the vertical direction can be as much as 44% higher than the lateral oxide growth rate [36]. The oxidation process was therefore carefully calibrated by oxidizing a polysilicon layer deposited on a test sample, and measuring the lateral expansion in an angled scanning electron microscopy (SEM) image. The vertical expansion was also observed using a stylus or optical profilometer for reference, but this measurement overestimates the actual channel length. Figure 4.11 shows SEM images of polysilicon pillars before and after oxidation.

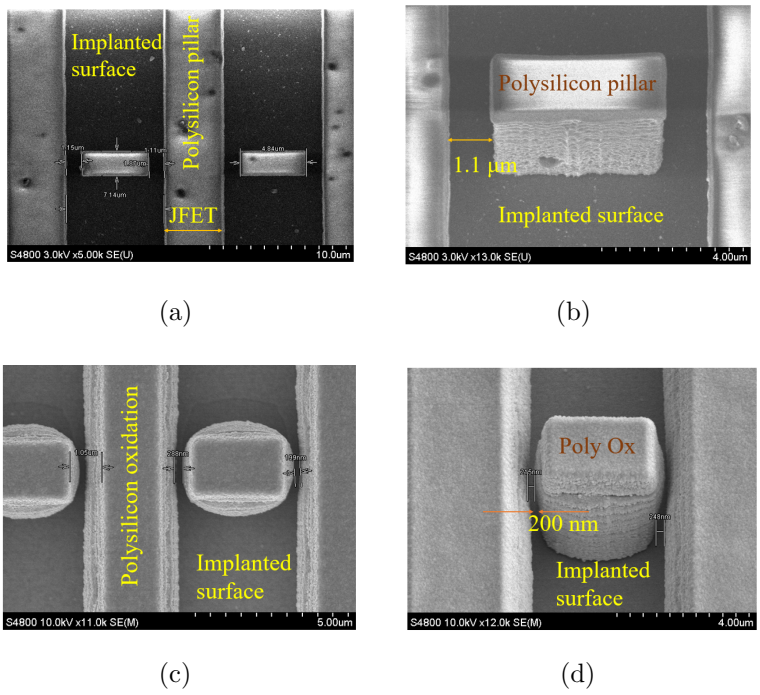


Figure 4.11. N-source implant SEM images: (a) Polysilicon pattern before oxidation; (b) Tilted view of polysilicon pattern; (c) Polysilicon oxidation SEM top view, and (d) Polysilicon oxidation SEM tilt view.

To block the high energy implants in the field area and process control module, a 2 µm thick nickel mask is necessary, based on a Monte-Carlo TRIM simulation [32]. To achieve this, a Ni electrodeposition process was used. This process requires the presence of a conformal conductive seed layer on the surface to act as a cathode terminal. Since the surface is oxidized, and thus is non-conductive, a bilayer of titanium (Ti) / gold (Au) is first deposited by sputtering. An initial test showed that a 100 nm thick Au layer sputtered at a pressure of 5 mTorr is insufficient to cover the polysilicon mask topology. This results in electrically isolated islands of seed metal in the trench bottoms that are disconnected electrically from each other, thus preventing electrodeposition in these areas. A short loop study revealed that a 500 nm thick Au layer is required to have sufficient coverage over the high aspect ratio polysilicon features. Alternatively, the sputter deposition can be done at higher pressure, but this carries a risk of non-uniform seed layer deposition and potential pinhole formation. After depositing the seed layer, optical lithography using 6-8 µm thick AZ9260 photoresist was performed, leaving the resist in the areas where the source implant is desired. This thick

resist acts as a mold during the electrodeposition process, preventing Ni deposition. The sample is then immersed in a custom made solution comprised of nickel sulphamate, nickel carbonate, boric acid, and DI water, and is connected to the cathode terminal. A bar of 99.9% purity Ni is used as the anode. For a quarter of 4″ sample, a current of 15 mA is used, which results in a Ni deposition rate of 1-1.3 µm/hr. A lower current 10 mA can also be used, but the deposition rate will fall proportionally. A detail procedure of Ni electroplating is provided in Appendix C. After the deposition, the photoresist is stripped in PG remover at 60°C for 1 hr. Finally, the Au layer is wet etched in a Transene GE-8148 Au etch solution which is compatible with both oxide and Ni. There is no available Ti etchant which is both compatible with oxide and Ni, so the Ti layer was left unetched. Since it is very thin, it does not perturb the implant profile significantly. A pictorial depiction of the source implantation process is shown in Fig. 4.12. Fig. 4.13 shows an SEM image of the electrodeposited sample.

After the definition of the source implant mask, the samples were mounted on a 5″ Si carrier wafer with carbon tape. The samples were then sent to mi2-GmbH to perform the high energy (604–3009 keV) nitrogen implants. After returning, they were then unmounted from the carrier wafer and sent to CuttingEdge Ions to perform the lower energy (33–380 keV) nitrogen implants on a 500°C heated stage.

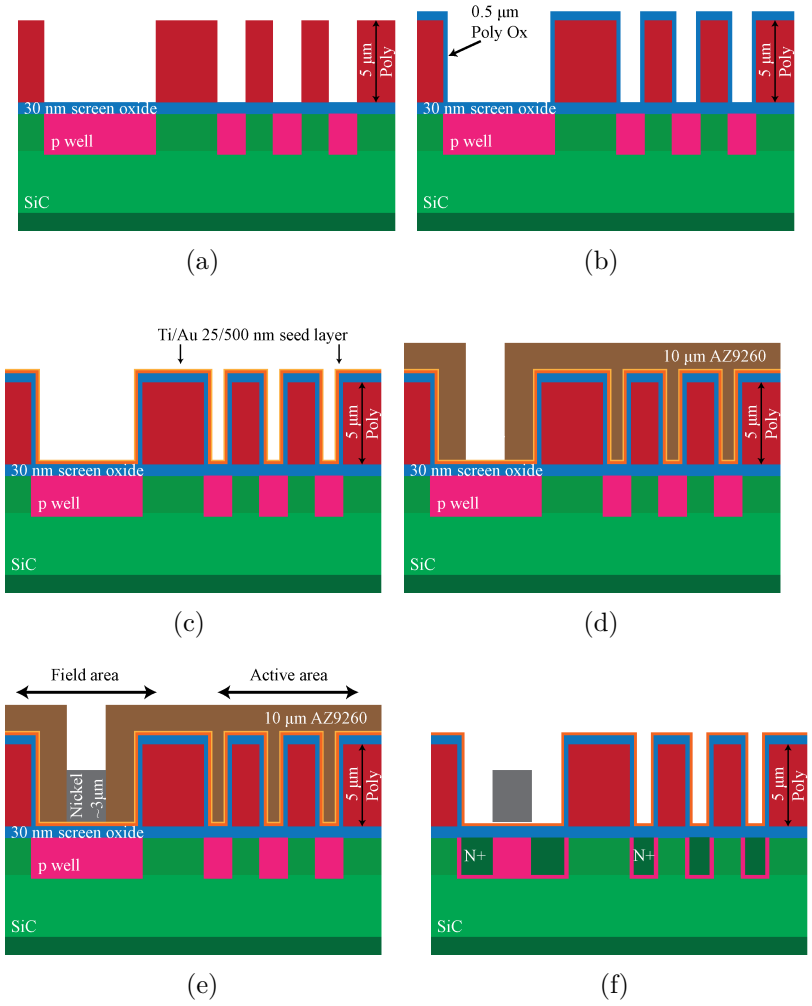
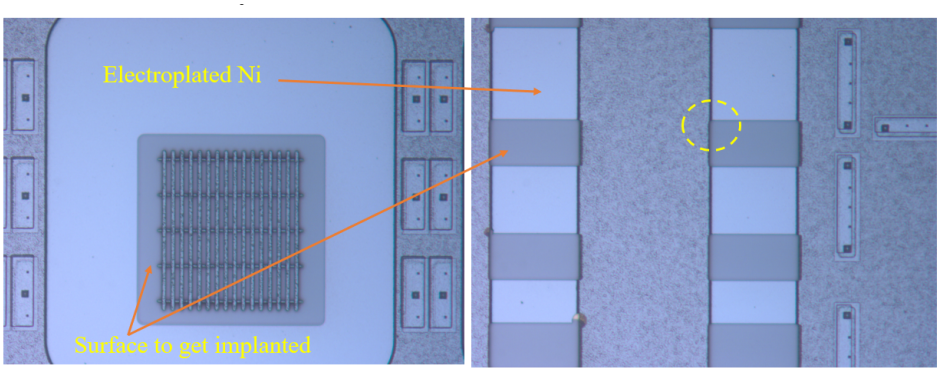


Figure 4.12. N-type source implant process flow: (a) CSL epilayer with p-well mask and implants; (b) 0.5 µm polysilicon oxidation to define the channel regions; (c) Ti/Au (10/500 nm) seed layer deopsition; (d) Photoresist mold formation; (e) 3-4 µm Nickel electrodeposition, and (f) N-type source nitrogen implant.



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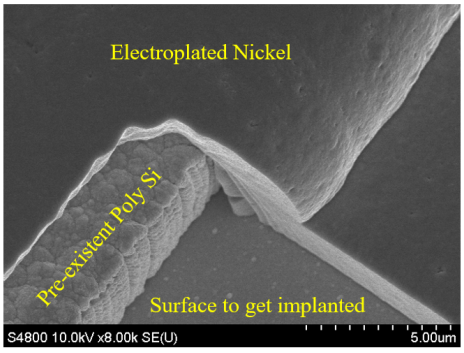
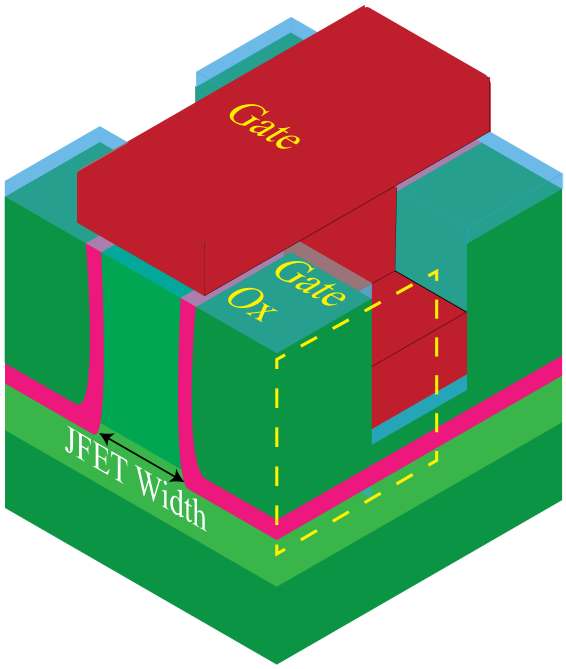


(b)

Figure 4.13. Image of nickel electrodeposition: (a) Microscope photo image of the electroplated Ni source implant block mask in a tri-gate active area and in a PCM lateral long channel MOSFET , and (b) SEM image of area in dashed yellow oval in (a)

4.3 Current Spreading Layer (CSL)

The basic structure for the half unit cell of the tri-gate MOSFET was simulated in 3D to identify an optimum design in terms of specific on-resistance and blocking voltage. The effect of JFET length and source contact length have already been discussed in the previous chapter. From the simulation study, it was revealed that the CSL thickness extending below the p-well / drift layer junction exhibits a lower than expected breakdown voltage. The unit cell shown in Fig. 4.14(b) should have a breakdown voltage of 930 V based on a planar one-sided step junction model, but the simulated breakdown voltage is only 740 V. This is because the higher doping of the CSL layer produces a steeper gradient in the electric field profile just below the p-base / CSL junction, resulting in a lower breakdown voltage. As a result, if the thickness of the CSL layer is reduced so that the bottom of the p-base forms a junction with the more lightly doped drift layer, the breakdown voltage should increase. A simulation study was also done on the reduced CSL thickness, and it was found that the blocking voltage rises to 1000 V as shown in Fig. 4.15. However, reducing the CSL layer thickness also impacts the overall device resistance. The thinner CSL is less efficient in spreading the current from the JFET region into the drift region compared to the original CSL design, increasing the specific on-resistance. This trade-off was investigated to find the optimum CSL thickness by maximizing the figure of merit $V_B^2/R_{ON.SP}$. Figure 4.15(a) shows the variation of $V_B^2/R_{ON.SP}$ vs. JFET width for different CSL thicknesses. A CSL that extends 0.6 µm below the trench bottom, given the p-implant profile as shown in Fig. 4.14(b), provides the highest figure of merit for nearly all JFET widths, as shown in Fig. 4.15(a).



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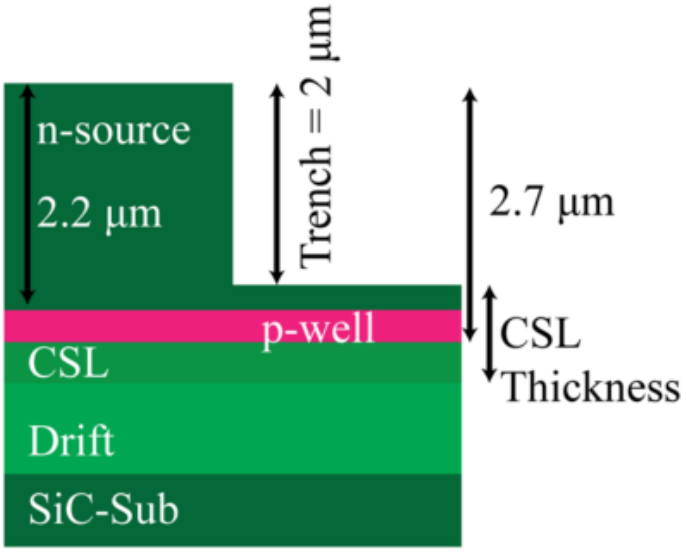
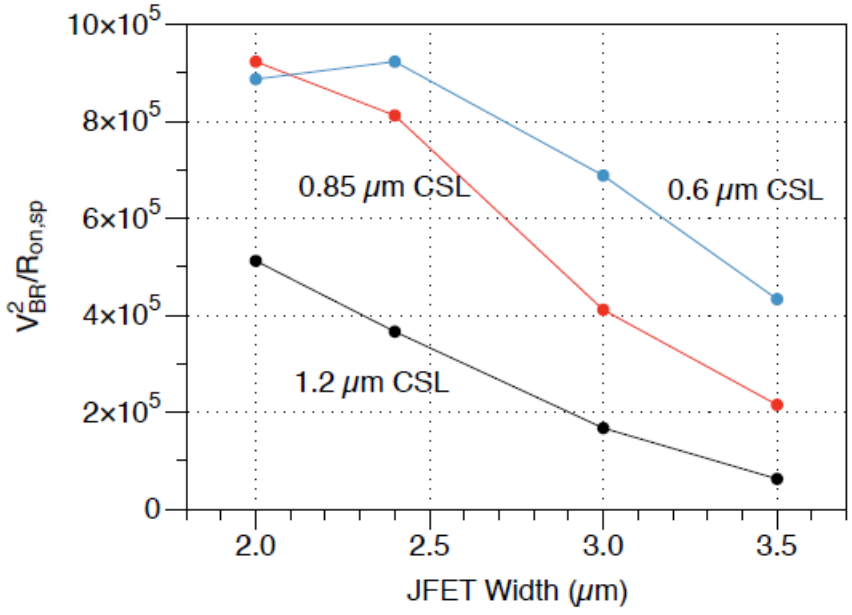
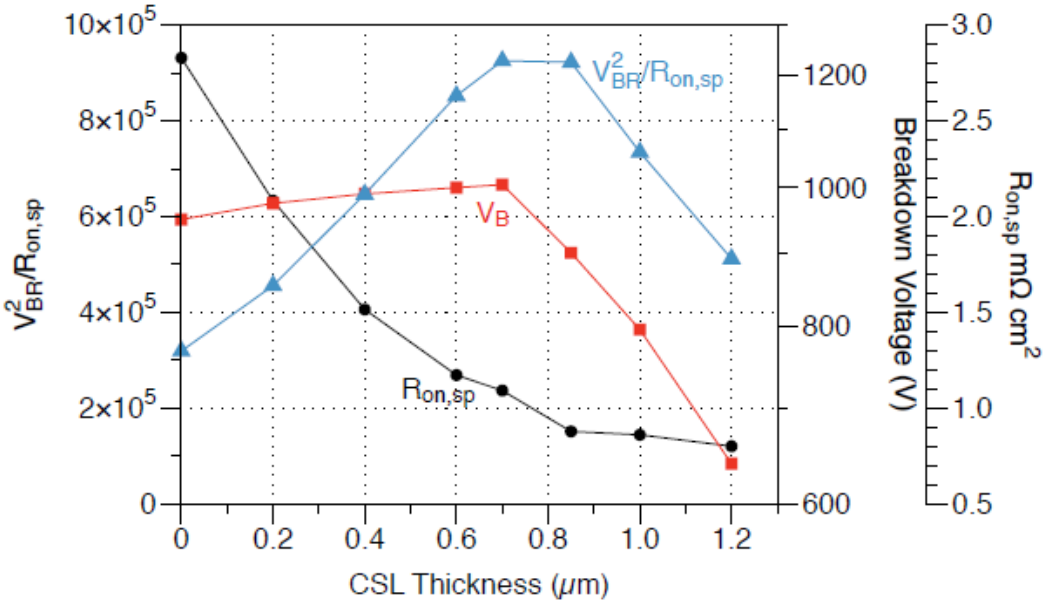


(b)

Figure 4.14. Impact of CSL thickness on the tri-gate device - Structural dimensions: (a) Isometric view of tri-gate device showing JFET region, and (b) Yellow highlighted cross section in (a), showing dimensions used in CSL study



(a)



(b)

Figure 4.15. Impact of CSL thickness on the tri-gate device - Performance (a) Variation in figure-of-merit with JFET width for different CSL thicknesses, and (b) Variation in figure-of-merit, breakdown voltage, and specific on-resistance with CSL thickness for a 2 µm wide JFET.

In accordance with the study, a split in the fabricated tri-gate devices was planned to have samples with both a 2.6 µm thick CSL layer, which requires a 0.6 µm blanket etch, as well as the original design with a 3.2 µm thick CSL. The blanket etch on the tri-gate sample was performed in an E-620 Panasonic ICP-RIE etcher with the recipe noted in Table 4.5. To monitor the etch rate and depth, three 1×1 cm^2 SiC control samples are attached with the tri-gate sample in the 6″ Si carrier wafer as shown in Fig. 4.16. Unlike the tri-gate sample, the control samples are patterned with a light field Ni mask defined by a metal lift-off process. The light field mask tone ensures the minimization of loading and aspect ratio dependent etching effects. The etch was done in a number of small steps to accurately control the etch depth. However, this does not account for any radial non-uniformity in the etch process. Such non-uniformity has not been observed in prior etches on patterned SiC test samples. The high energy ion bombardment and etching roughens the surface, which could be detrimental for the channel interface. Considering these uncertainties and potential damage associated with this blanket etch, the processed wafers include samples that are not etched, where the process is done on the full 3.2 µm thick CSL layer. The CSL layer thicknesses of the fabricated Gen-1 tri-gate samples is noted in Table 4.1.

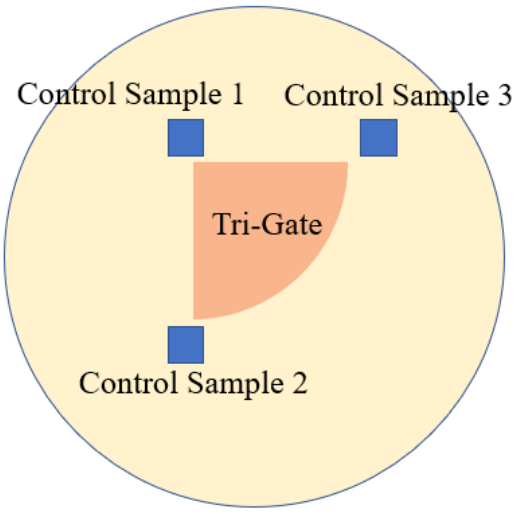


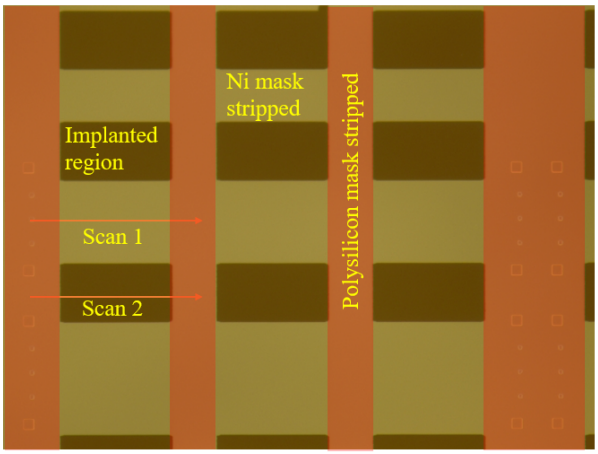
Figure 4.16. Tri-gate sample loading strategy for blanket CSL thinning etch with small SiC control samples

Table 4.5. SiC etch recipe in E-620 Panasonic

Parameter	Etch	
Gas (sccm)	SF_6 (20)	
ICP power (W)	600	
Bias power (W)	200	
Pressure (Pa)	3	
	SiC	Ni
Etch rate (nm/min)	170	5

4.4 Implant Swelling

High energy implant related swelling was observed in the tri-gate devices. Figure 4.17 shows a long channel MOSFET PCM device in a tri-gate sample after the high energy p-well and n-source implants were accomplished, and the implant mask was stripped. The roughness caused by the high energy ion impingement usually reveals the implanted areas under optical microscopy. Stylus profilometer scans were taken over the implanted region (scan 2 in 4.17(a)) which shows a swelling of the SiC surface of around 9 nm, as shown in Fig. 4.17(c). At the same time, a scan (scan 1 in 4.17(a)) was taken over the area across the window of p-well implanted surface to the poly mask region in the long channel MOSFET as shown in Fig. 4.17(b). It shows a depression of around 3 nm in the SiC, which can be interpreted as an etch of the SiC surface which occurred at the end of the polysilicon implant mask etch. It suggests either the screen oxide was thinner than expected, or the oxide selectivity under the polysilicon trench area is less compared to the selectivity of the oxide on the top of the poly layer due to insufficient polymer deposition in the high aspect ratio polysilicon etch. Nevertheless, the exhaustion of the insufficiently thick screen oxide results in a slight SiC etch, and thus it is recommended that a thicker (∼50 nm) screen oxide should be grown. The data also suggest that the implant swelling has happened mainly due to the higher dose nitrogen implant.



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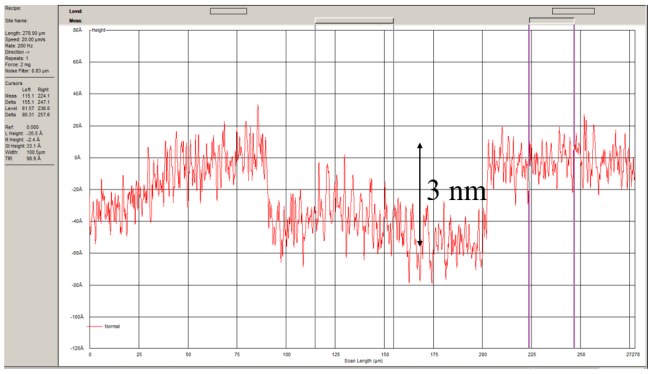

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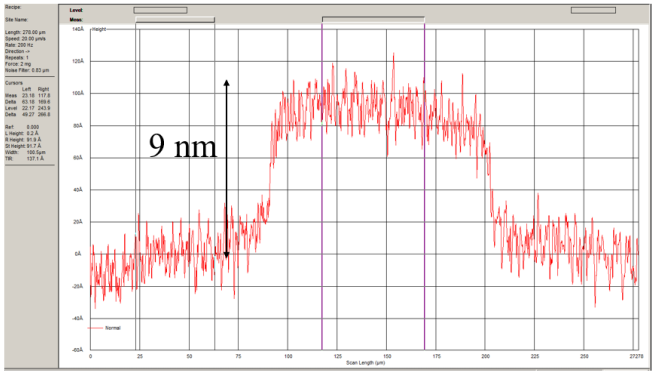


(c)

Figure 4.17. Implant swelling after p-well and n-source implants prior to the implant anneal: (a) Optical image of long channel MOSFETs after p-well and n-source implant with mask been stripped. Red highlighted areas represent the placement of the poly implant mask, while the lighter green areas represent the electroplated Ni; (b) Possible etch of SiC during the polysilicon mask patterning process, and (c) Possible surface swelling during the high energy implant process.

4.5 Implantation – P^+ Well Contact

In a typical power MOSFET, the p-well and n-source are connected together. To accomplish this, a highly doped p-type aluminum implant is needed at the surface of the p-well layer to form an ohmic contact. This contact is then shorted to the source region by a common metal, in this case Ni, deposited over both. Good ohmic contact between Ni deposited on aluminum doped p-type regions is not optimal in SiC, and the process used in this thesis leads to a Schottky contact over the p-well region as seen in the I-V measurements shown in Fig. 4.18. This is not desirable for robust transient operation of the device. However, in order to initially demonstrate the efficiency and benefits of this novel tri-gate structure, quasi-steady-state operation is sufficient. The profile for a heavily doped p-type aluminum implant was designed according to the empirical model reported in [30]. The profile is shown in Fig. 4.19, where a box profile implant with a nominal aluminum doping concentration of 2×10^{19} cm^{-3} over a range of 300–350 nm was implemented. The implant profile energy and dose information are provided in the Table 4.6.

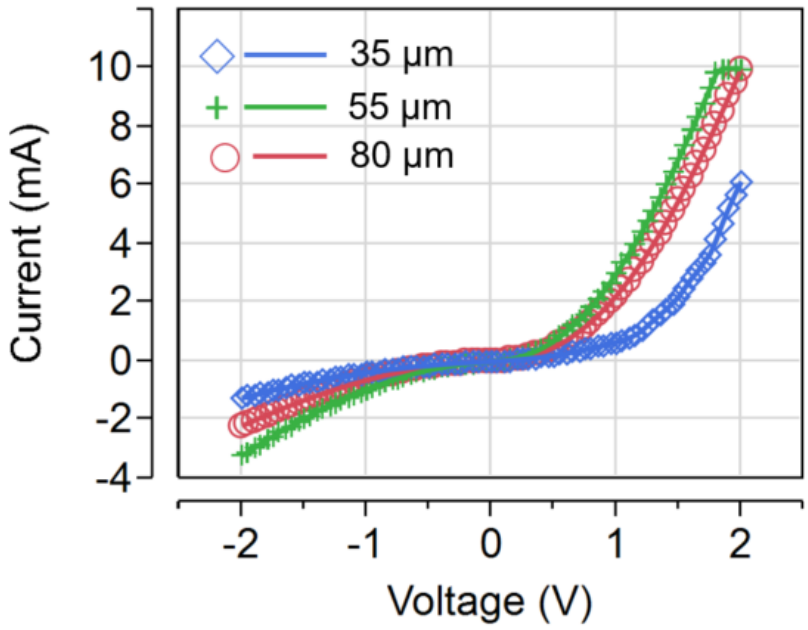


Figure 4.18. I-V data on a P+ TLM pattern with pad spacings of 35 µm, 55 µm, and 80 µm .

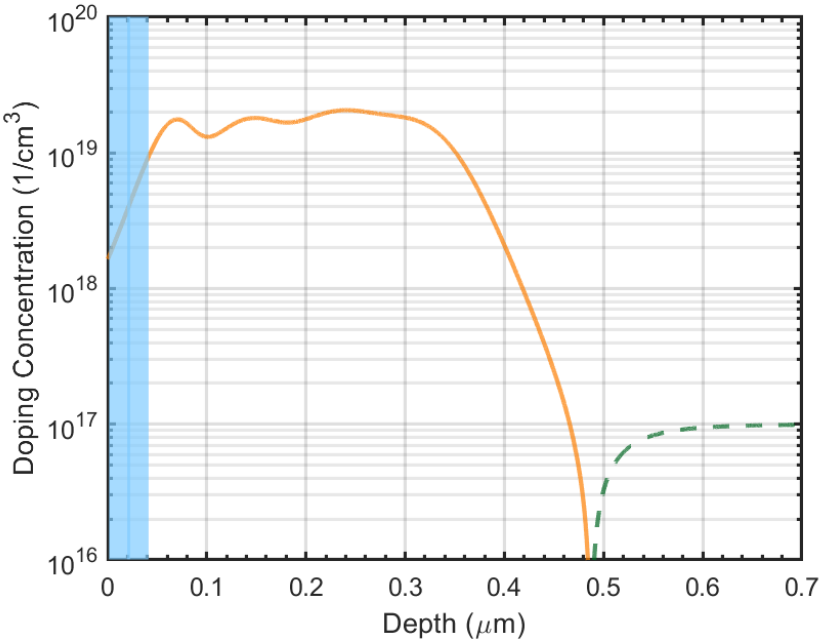


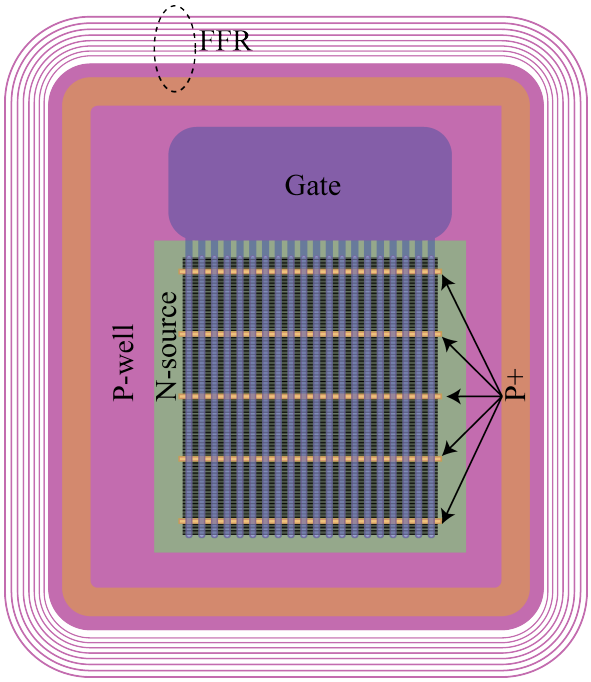
Figure 4.19. Net implantation profile in the p^+ base contact region. The orange solid line is the implanted aluminium concentration, and dashed green line is the background n-CSL doping. The shaded blue region highlights the screen oxide present on the surface during the implantation.

Table 4.6. Gen-1 tri-gate – p^+ implant profile

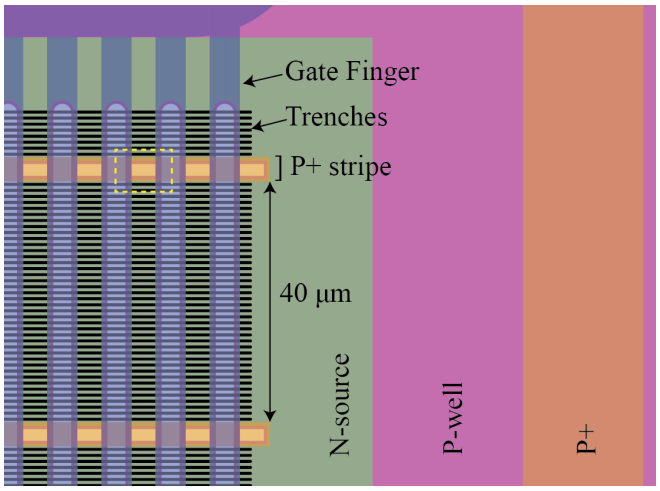
Energy (keV)	Dose (#/cm^2) $\times 10^{14}$
40	0.70
87	1.32
150	1.28
220	1.22

Fig. 4.20(a) shows the mask layout of a tri-gate device, highlighting the p^+ base contact implants in both the field and active areas. In the field area, an 18 µm wide p^+ ring provides base contact around the periphery, and carries any avalanche current which might occur in the termination region. In addition, within the active area a series of 4 µm wide p^+ contact stripes provide local base contacts to enhance transient robustness. Along these stripes there are no active transistors, so the number and size of these stripes should minimized. In our design, the adjacent stripe spacing is 40 µm, and there are five p^+ stripes in the 0.04 mm^2 (200 µm × 200 µm) active area as shown in Fig. 4.20(b). The contact areas in

each stripe are defined by the p-well implantation step. The process used to achieve a p^+ contact is illustrated in Fig. 4.21, which is the region highlighted by the yellow dashed line in Fig. 4.20(b). In Fig. 4.21(a), the polysilicon p-well implant mask defines the JFET region. In the same lithographic step at the intersection of the p^+ stripe and the source finger, an isolated polysilicon post has been patterned. The distance between the JFET finger and the polysilicon post is 1 µm, as shown in Fig. 4.21(a). The space between the polysilicon post and the JFET finger is filled with thermally grown oxide during the self-aligned source process used to define the channel. Since the n^+ source implant is blocked around the periphery of this post, contact to the p-well can be accomplished with a shallow, heavily doped Al implantation. This scheme to form the p-well contact is shown in Fig. 4.21(b) and (c). The shaded region in Fig. 4.21(d) shows the contact area to the p-well layer. Cross-sections in Fig. 4.22 shows the overlap of the heavily doped p-implant with the p-well layer, which forms the base contact. The ohmic and top metal layers connect the source and p-well contact regions together. In the JFET regions shown in Fig. 4.22, the p^+ implant is all that separates the source ohmic contact from the CSL layer. It is therefore important to design the p^+ to CSL junction depth to accommodate any SiC material consumption which occurs in the various preceding processes like oxidation or etching, to prevent source to drain electrical shorts.



(a)



(b)

Figure 4.20. Base contact p^+ implant: (a) Mask layout, and (b) p^+ implant strip in the active region.

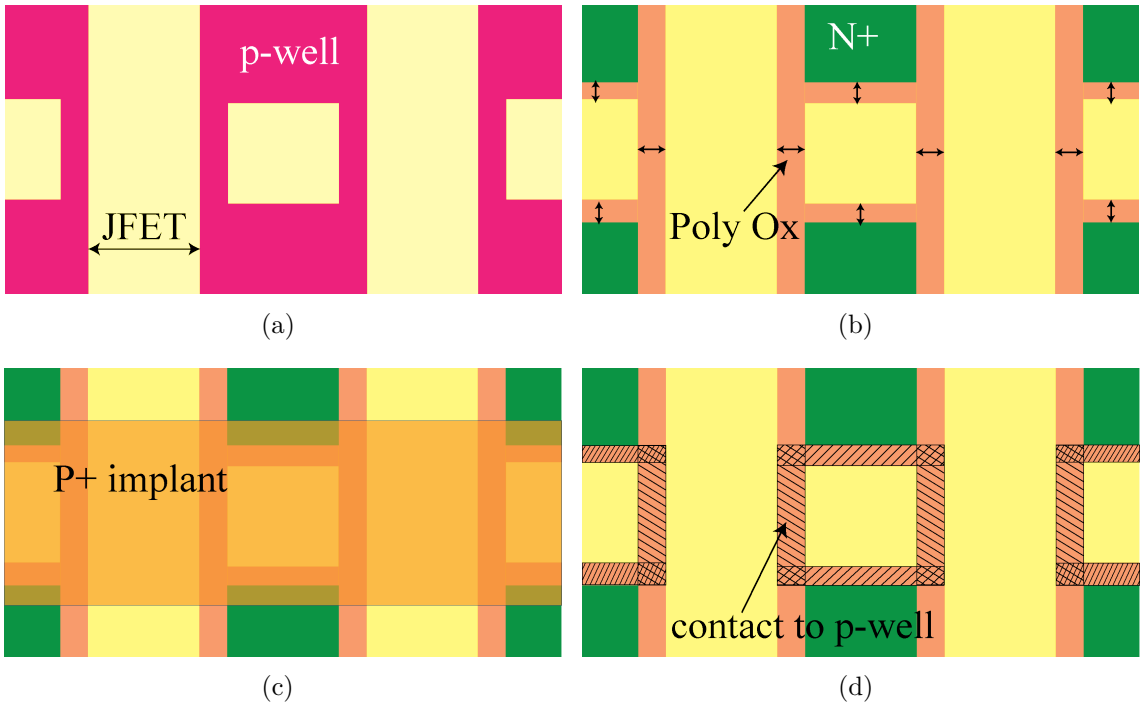


Figure 4.21. Base contact P^+ implant formation (a) p-well implant and JFET regions; (b) self-aligned 0.5 µm poly oxidation and source implantation; (c) P^+ implantation, and (d) base contact area.

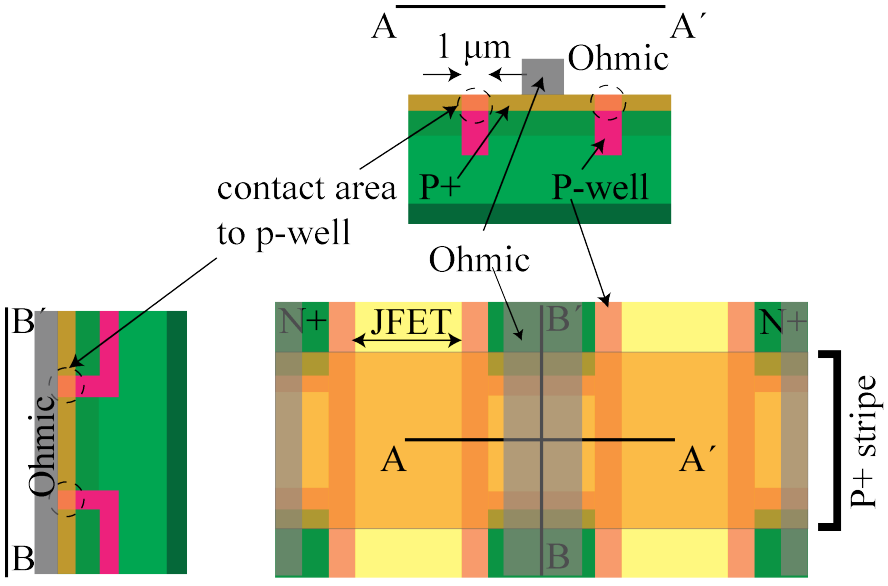


Figure 4.22. Base contact P^+ implantation and cross-section views of showing formation of contact

According to a TRIM Monte-Carlo simulation, a 320 nm thick Ni layer is needed to block the highest energy in the p^+ implantation profile. A 10/500 nm thick Ti/Ni layer was deposited by e-beam evaporation and patterned with lift-off in both the field and active areas. In the field area, as shown in Fig. 4.20(a), the p^+ ring is 18 µm wide, which is large enough to use an optical lithography process using an MJB3 SUSS mask aligner. However, in the active region, the critical dimension is 2 µm which is challenging to reproduce with typical contact/proximity optical lithography. Therefore the design rules developed require features less than 4 µm wide to be patterned using e-beam lithography, and were initially performed using the Vistec VB6 at 100 kV energy. However, the more recent availability of the high resolution mask-less MLA-150 aligner from Heidelberg, this process can be done in a singe optical lithographic step. This method was used for Gen-2 tri-gate device fabrication. In this section, both the dual e-beam / optical process (scheme 1) and the single optical process (scheme 2) are discussed.

In scheme 1, e-beam lithography was first performed with an e-beam resist bi-layer consisting of 800 nm of copolymer EL11 and 200 nm of 950K PMMA A4. Each resist layer was baked at 180°C for 3 min. The resist stack was then exposed in the Vistec VB6 e-beam lithography system at 100 kV and 122 nA, with a dose of 700 µC/cm^2. The resist was developed in a MIBK:IPA (1:3) solution for 1 min, followed by an IPA rinse. Since the copolymer resist is more sensitive than the upper 950K PMMA A4 resist layer, an undercut resist profile is thus achieved as shown in Fig. 4.23, which is ideal for the metal liftoff process. Any resist residue was removed in a Branson resist ashing system using an Ar/O_2 plasma at 100 W power for 20 sec. A 10/500 nm Ti/Ni layer was then deposited and lifted off in a bath of hot PG remover solution, and the resulting pattern is shown in Fig. 4.24(a). The outer p^+ ring as shown in 4.20(a), as well as the p^+ regions in the PCM were defined by an optical lithography and metal lift-off process. This was accomplished using an optical resist bi-layer of LOR 3B and AZ1518. The liftoff resist LOR 3B was spun twice at 2000 rpm to obtain an 800 nm thick undercut layer for effective lift-off of a 500 nm metal layer. In each step, the LOR 3B resist was soft baked at 190°C for 5 min. A film of AZ1518 was spun on top of the LOR 3B layer at 4000 rpm for 40 sec and baked at 120°C for 2 min. This bi-layer resist stack was then exposed in the MJB-3 proximity aligner with a power density of 10 mW/cm^2 for

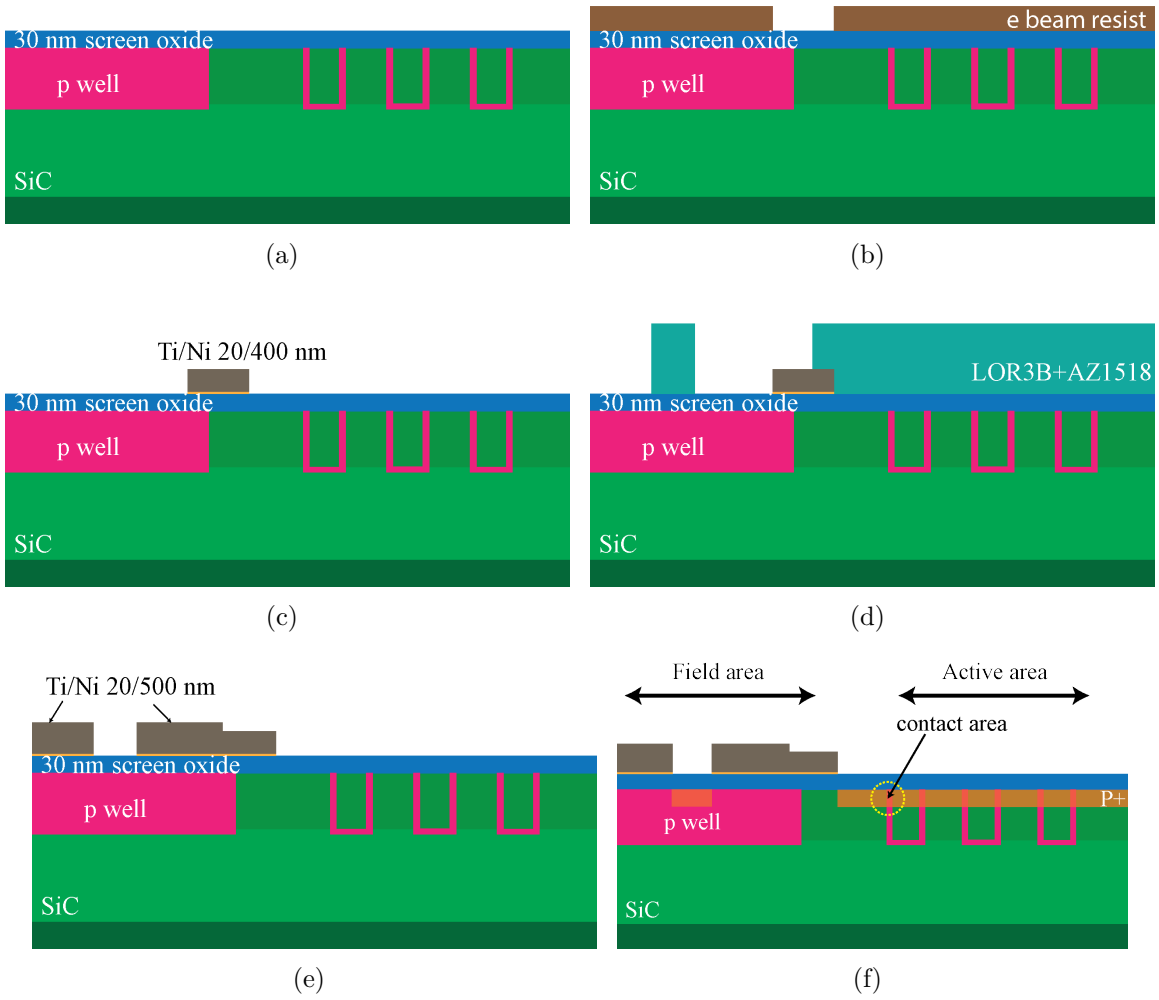
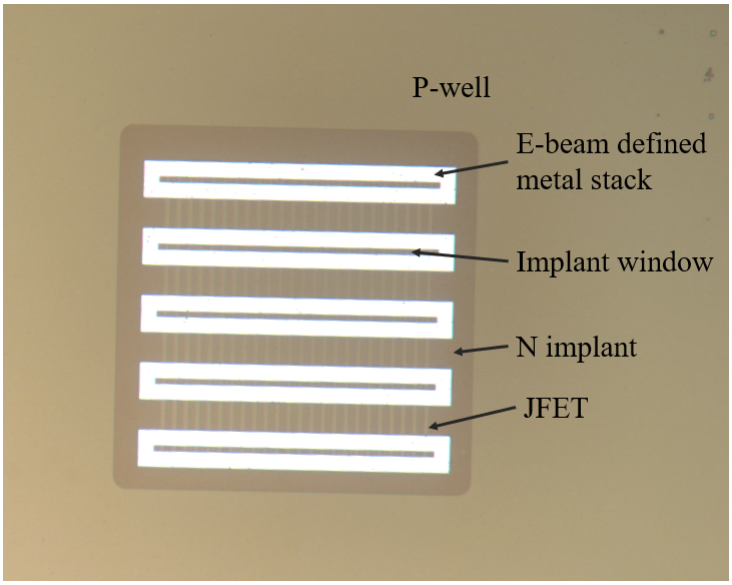
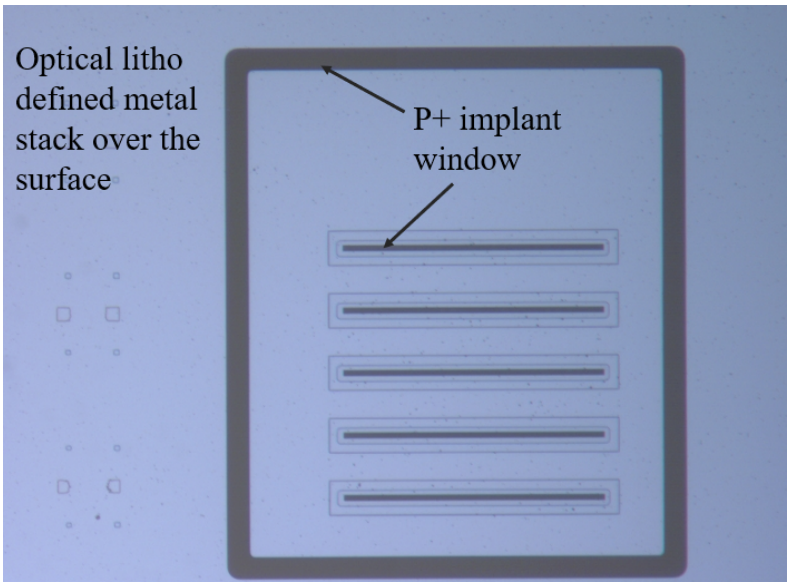


Figure 4.23. p^+ base contact aluminum implant process flow 1: (a) SiC epi with p-well; (b) Bilyaer e-beam resist pattern (copolymer EL11 and 950 K PMMA A4); (c) Ti/Ni (10/400 nm) metal lift-off; (d) Optical photoresist pattern; (e) Ti/Ni (10/500 nm) metal lift-off; and (f)p^+ aluminum implant.

18 sec. The resist was then developed in MF26A for 30 sec, followed by ashing in an Ar/O_2 plasma at 100 W power for 1 min to remove residue. The developed resist was then used to lift-off a 10/500 nm Ti/Ni e-beam evaporated layer in a bath of hot PG remover. The optically defined metal lift-off feature is shown in Fig. 4.24(b), which overlaps the e-beam defined feature by 5 µm.



(a)



(b)

Figure 4.24. p^+ base contact aluminum implant process flow 1.: (a) E-beam defined Ti/Ni (10/400 nm) lift-off, and (b) Optically defined Ti/Ni (10/500 nm) lift-off.

In scheme 2, a single optical lithography step can be performed using the high resolution mask-less MLA-150 optical aligner from Heidelberg to define the p^+ implant. Similar to the optical lithographic process of scheme 1, a bi-layer optical resist of LOR3B and AZ1518 were used. The 800 nm thick LOR 3B and 1.8 µm thick AZ1518 resist layer was exposed in the Hidelberg with a dose of 200 mJ/cm^2. It was found that the required high resolution pattern cannot be achieved using the pre-made MF26A developer, and that a solution of AZ400K:DI water (80:300 ml) for 30 sec provides better results. The developed resist residue was removed in a Branson resist ashing system using an Ar/O_2 (120/6 sccm) ambient at 100 W for 1 min. The resist ash is followed by the deposition of 10/500 nm of Ti/Ni and lift-off in a hot bath of PG remover at 60°C for ∼8–10 hr. An optical microscopy image of the resulting pattern is shown in Fig. 4.26. This simplified and efficient implant block mask technique was used in fabricating the Gen-2 tri-gate devices.

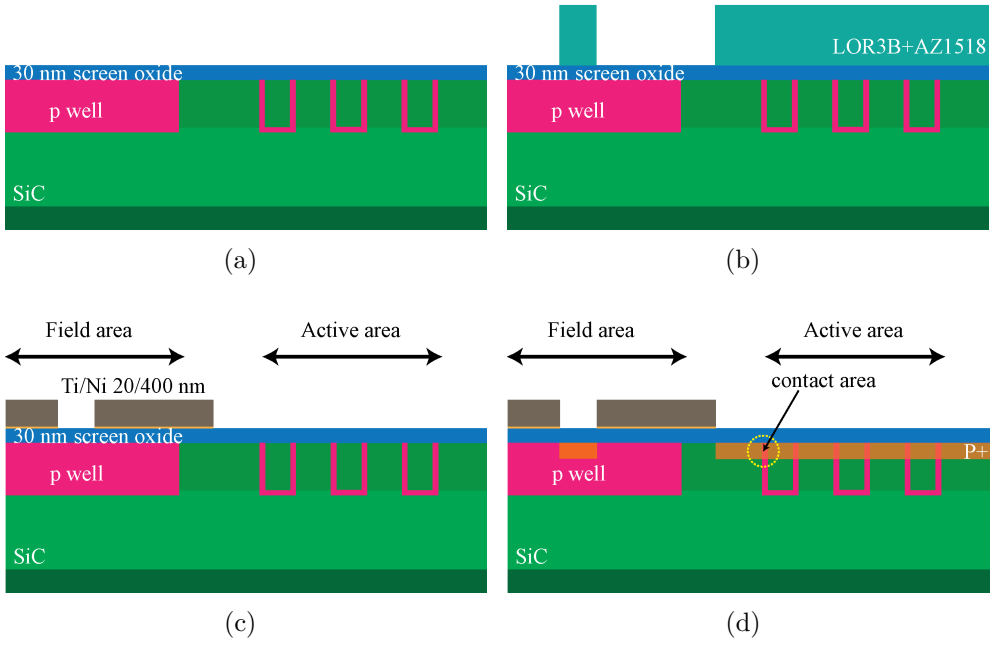


Figure 4.25. Aluminum P^+ implant process flow 2: (a) SiC epi with p-well; (b) Optical resist pattern; (c) Ti/Au (10/500 nm) metal lift-off, and (d) Aluminum p^+ implant.

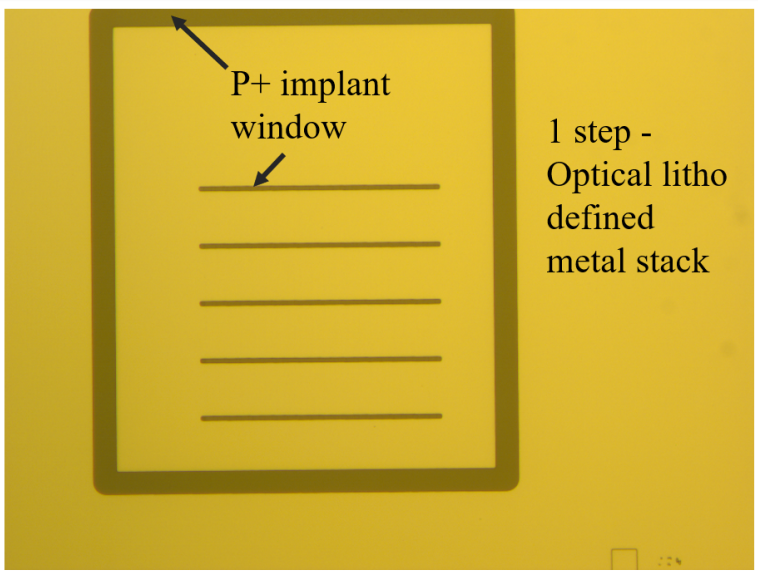
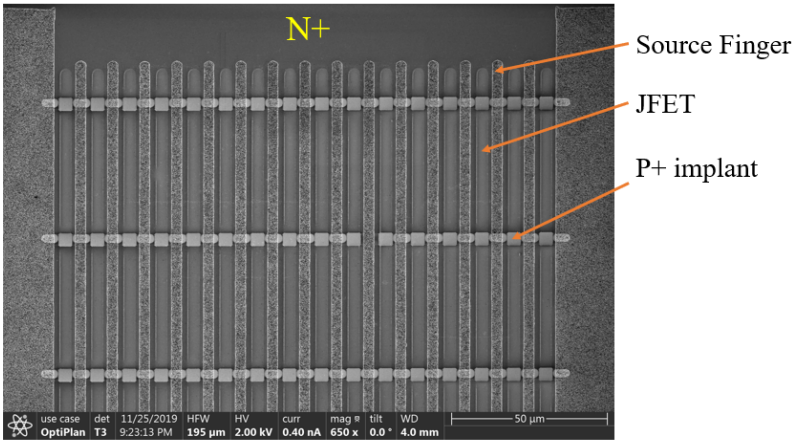
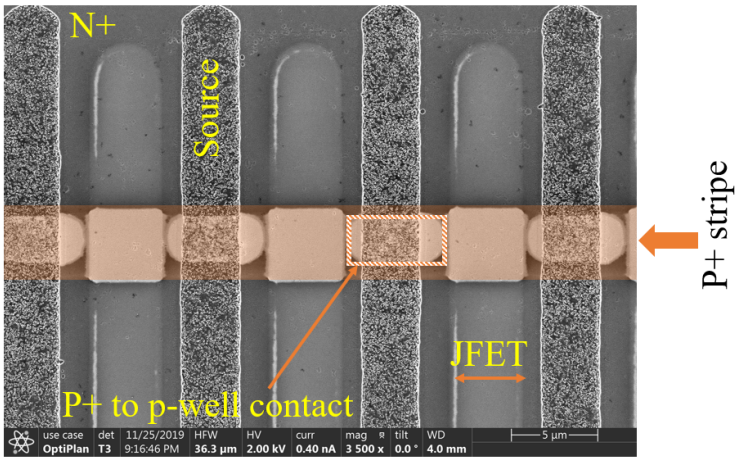


Figure 4.26. Base contact implant mask Ti/Ni (10/400 nm) liftoff in the 1 step optical lithography.

The patterned samples were then shipped to CuttingEdge Ions to perform implantation of Al at 500°C with 0° tilt and twist angle. An SEM image of the resulting p^+ implant using secondary electron potential contrast (SEPC) is shown in Fig. 4.27.



(a)



(b)

Figure 4.27. SEM images showing the p+ implant contact area in a finished device.

This is the last implantation required in the tri-gate MOSFET fabrication. After completion, an implant activation anneal was conducted. The detail of the annealing process can be found in [37]. In brief, a photoresist layer was first deposited on the wafer. The resist was carbonized at high temperature (600-700°C). This forms a capping layer to prevent any Si sublimation and step bunching on the SiC surface during high temperature annealing. The wafer was then annealed at 1700°C in the Epigress VP-508 SiC epitaxy reactor to activate the implanted dopant. After the activation anneal was completed, the carbonized resist was stripped in presence of O_2 at 900°C.

4.6 Trench

The Gen-1 tri-gate devices feature 2 µm deep trenches to reveal sidewalls for additional current conduction paths. The trench etch process therefore plays a crucial role in device performance. A significant experimental effort was done to develop a stable SiC trench etch process. In this section, the details of this study will be covered, highlighting the etching strategy, mitigating non-ideal effects, and achieving a highly anisotropic profile.

SiC, a highly anisotropic material, shows different electron mobility properties on different faces and in different directions. The a-face mobility is reported to be higher than the mobility on the Si-face [38], [39]. Based on a literature review, the field effect electron mobility in on-axis $\{11\bar{2}0\}$ (a-face) channels can be as high as 120 $cm^2/(V \cdot s)$, while the mobility on the $\{0001\}$ Si-face is typically $\sim$35 $cm^2/(V \cdot s)$ with a p-well doping concentration of 1×10^{16} cm^{-3}. According to these findings, the tri-gate device structure facilitates enhanced carrier conduction in the channel not only by the increase in effective channel width, but also with potentially higher mobility on the sidewalls. The literature suggests the $\{11\bar{2}0\}$ face of 4H-SiC exhibits the maximum channel mobility. The mask layout is therefore designed such that the trench etch process reveals the a-face on the sidewall of the tri-gate trench structure. In order to implement the design, the trench fingers are directed perpendicular to the major flat of the wafer, which is in the $[11\bar{2}0]$ direction. To accommodate that the JFET finger mask and gate runners are aligned parallel to the $[11\bar{2}0]$ direction. The mask alignment and direction of different levels are shown in Fig. 4.28.

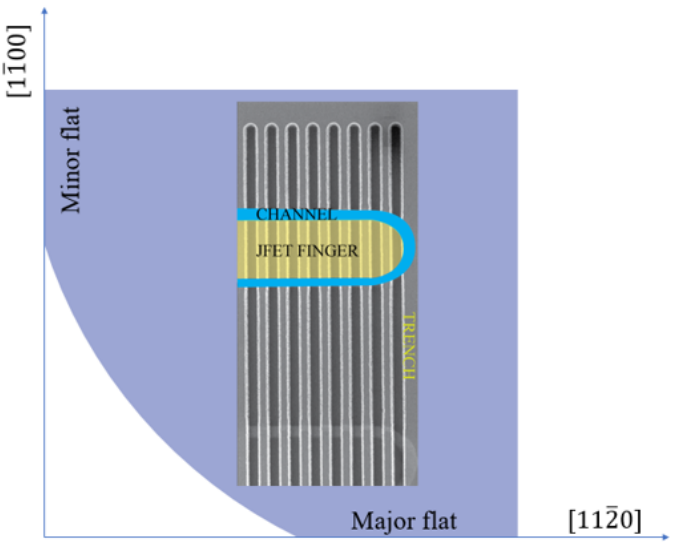


Figure 4.28. The orientation of the trench and gate runners in the tri-gate MOSFET with respect to wafer flats and crystallographic directions.

However, the tri-gate device fabrication is done on epitaxial layers grown on 4°off-cut 4H-SiC wafers. Unlike an on-axis wafer, the surface of off-cut wafers deviates from the primary crystallographic directions by the angle of this cut from Si-face towards the [$\bar{1}\bar{1}$20] direction. Due to this deviation, the mobility on the a-face sidewall may not be as high as reported in [38], [39].

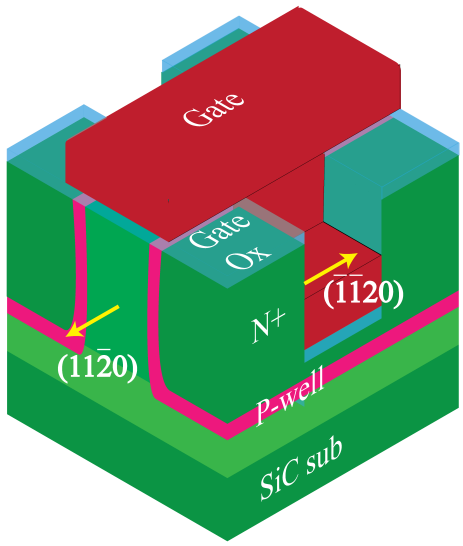


Figure 4.29. Isometeric diagram of tri-gate device showing the directions of exposed sidewalls.

As a result, the effective sidewall mobility of a finished tri-gate device may not be as high as 4× compared to that of the Si-face as seen in an on-axis wafer [39]. But even a conservative assumption of 2× mobility improvement on the sidewall would produce a 9× reduction in channel specific on resistance in a 2 µm deep trench tri-gate device compared to a planar DMOSFET with similar technology. Thus, higher sidewall mobility would result in an added advantage for the tri-gate structure.

As mentioned earlier, the trench sidewall mobility may be reduced by any deviation of the orientation of the sidewall surface from the desired a-face. The a- and m-faces cannot be accurately identified from the wafer major or minor flat orientation, as the potential error in flat orientation from the primary crystallographic directions is in the range of ±5° [40]. So precautionary measures can only be taken to prevent any further deviations which may result from a number of processes, including an angle in the trench profile, wafer dicing alignment, JFET and trench lithography rotation, etc. In the wafer dicing process, the deviation of the cut from the major or minor flat direction was measured in an SEM to be below 1°. In the e-beam lithography process, both in the JFET and trench layers, the deviation was lower than 0.5°.

Trench etch anisotropy also plays a role in the degree of the deviation of the sidewall surface from the principal crystallographic directions. A deviation of 4° will be obtained on both surfaces with a perfect 90° anisotropic etch profile due to the wafer off-cut angle. Perfect anisotropy in the etch profile is not necessary in the tri-gate device, since as seen in Fig. 4.30 a trench angle will move the crystallographic $(11\bar{2}0)$ face more towards the true on-axis surface, which may increase the electron mobility, while the face of the opposite sidewall on $(\bar{1}\bar{1}20)$ will move away from the on-axis surface, possibly decreasing the mobility. The net increase or decrease in electron mobility will depend on the amount of mobility change on each sidewall face, but is likely to be small since the changes are opposite in nature. This is an advantage of tri-gate device over UMOS [41] or IMOS [42] device which requires a nearly perfectly vertical etch profile to prevent unwanted sidewall channel doping from the trench oxide shield implant. The most important factor in developing this process is to prevent or minimize any non-ideal etch effects, including micro-trenching, micro-masking, sidewall bowing, etc. In this work, a nearly anisotropic etch process has been established, essentially free from these effects, which also can be used in other SiC trench MOSFET device fabrication.

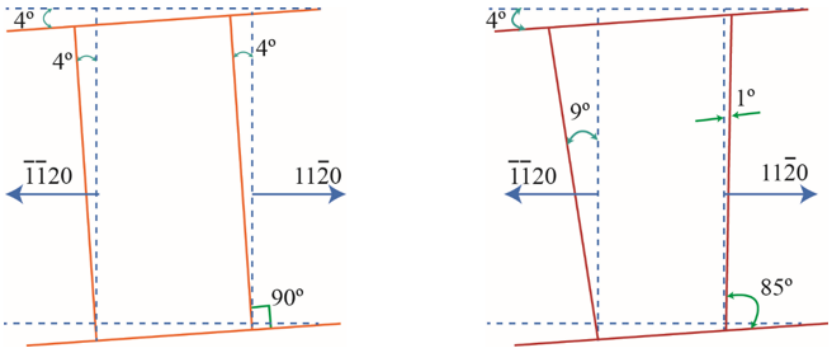


Figure 4.30. Deviation of trench sidewalls with respect to principal crystallographic directions on a 4° off-cut wafer.

Other factors which may potentially introduce undesirable defects such as surface damage during high energy ion bombardment, insufficient removal of sidewall surface contamination or etch mask residue deposited on the sidewall were not studied extensively in this thesis. These unwanted defects may limit the channel mobility of the final tri-gate device. However,

to mitigate these non-ideal effects, a sacrificial SiC oxidation and removal step was performed after the trench etch process. Alternatively, a hydrogen etch process can be used to remove the plasma etch damage and passivate the sidewall surface [43] . Additionally H_2 anneal/etch process helps by rounding the sharp corners of trench features which prevents field crowding at both the top and bottom corners of the trench.

In order to establish a stable trench etch process and for fine-tuning of various parameters, a number of iterations were done on 1×1 cm^2 SiC test samples. The samples were diced from a standard 4″ SiC n-type doped substrate in a Disco Dad 2H/6 dicing saw using a resin blade. Although these test samples differ from the tri-gate material in terms of size and doping profile, the etch results were found to be reproducible on the tri-gate material cut into quarters of a 4″ wafer except for a slight loading issue which required etching slightly longer to achieve the desired etch depth.

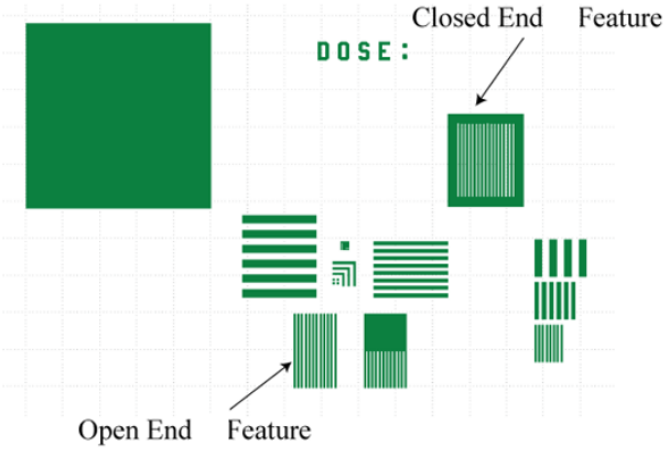
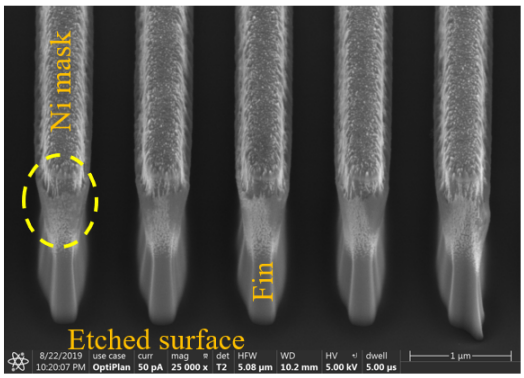


Figure 4.31. Mask layout template for test SiC sample trench etch .

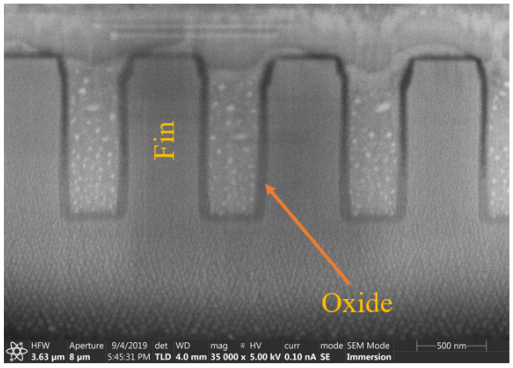
A simple mask layout as shown in Fig. 4.31 was used for these short loop experiments to develop the SiC etch process. This layout includes a series of arrays of fingers with both open and closed ends as shown in the figure. The width of these fingers were varied from 0.5 to 2 µm and the length is kept at 20 µm. A 50 µm square box for performing stylus profilometer measurements is also included in the design layout. All features were defined in a 100 kV

30 nA e-beam lithography system. The choice of mask material and its shape also play an important role. A highly selective and a vertical mask is desirable to get an anisotropic etch in SiC. In this case, a Ti/Ni (20/200 nm) bi-layer metal stack was used as the masking material which is highly selective in 4H-SiC trench etch. The selectivity of the metal hard mask was found to be in a range of 30-42 depending on the plasma condition. The shape and line edge roughness of the mask was optimized by performing a dose test experiment with proximity effect corrections enabled on the e-beam lithography system. The features were defined by 400 nm thick 950K PMMA A6 e-beam resist exposed in a 100 kV e-beam lithography system at 30 nA current and a dose of 1200 µC/cm^2. The exposed patterns were then developed in MIBK: IPA for 1 min followed by a 1 min rinse in isopropyl alcohol (IPA). The resulting resist pattern was then barrel etched in a Branson asher at 50 W for 20 sec in an ambient of Ar/O_2 with a flow rate of 120/6 sccm. This was then followed by the e-beam evaporation of Ti/Ni (20/200 nm) and lift-off in hot (60°C) PG remover overnight (∼8-10 hr). After performing a solvent clean, the samples were ready to etch in the plasma etchers.

The etches were performed in a multi-step process, and at each step the etch depth and rate were determined from the stylus profilometer measurements performed on a large 50 µm square box feature. This may not accurately represent etch depths for 0.5 µm wide features due to aspect ratio dependent etch rates which occur because of lag in reactive ion transport in narrow features. To obtain the correct etch depth and etch profile in high resolution features, an angled SEM or FIB cross-section SEM analysis is required. The SEM analysis of an etched SiC sample revealed that the etch profile not only depends on the plasma condition but also on the shape and dimensions of the pattern. The SEM image of such a test etch in an STS AOE ICP-RIE tool is shown in Fig. 4.32. The etch parameters are listed in Table 4.7.



(a)



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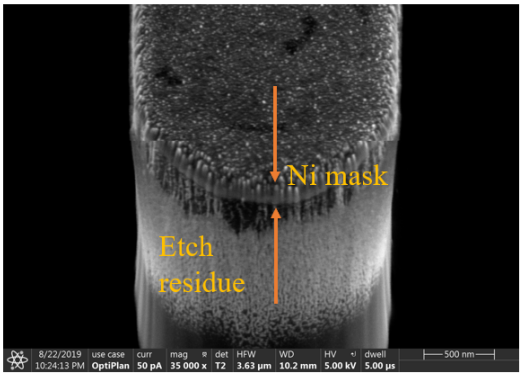


(c)

Figure 4.32. SEM image of trench etch process applied to a SiC test sample with the mask layout shown in 4.31: (a) Open end features; (b) FIB cross-section after oxide deposition, and (c) Close-up of highlighted region in 4.32(a).

Table 4.7. SiC etch recipe in an STS-AOE ICP-RIE

Parameter	Etch
Gas (sccm)	SF_6/Ar (20/10)
ICP power (W)	2800
Bias power (W)	100
Pressure (mtorr)	2

	SiC wide feature	SiC narrow feature
Etch rate (nm/min)	274	150

The images in Fig. 4.32(a) and (b) show the differences in the etch profile produced under the same plasma conditions in open and closed end features, respectively. The open end etch image was taken in an angled stage SEM tool, and the image of the closed end features was

taken by cutting a cross-section in a FIB tool. In the open end features, the edges are exposed to the high density ion flux, which results in different etch profiles compared to closed end features and does not represent the tri-gate trench layout. Therefore process development was done based on FIB cross-section images rather than on analysis of the open end test structures. Figure 4.32(c) shows a close-up of the highlighted region in the Fig. 4.32(a), which reveals etch residue which built up during the etch process. We attempted to clean this etch residue using successive SiC sacrificial oxide growth and stripping, but have not yet evaluated its effectiveness.

Three different ICP-RIE etching tools have been used in the process of establishing a SiC trench etch recipe. These tools are: Panasonic E620, STS AOE, both in the Birck facility, and an Oxford PlasmaPro 100 at Notre Dame University. The specifications of the Oxford PlasmaPro and the STS AOE etch tools allow high density plasma etching with high ICP power (maximum 3 kW) and bias power (300 W). On the other hand, the Panasonic E620 is limited to a maximum ICP power of 1.2 kW. High ICP power (>2 kW) is required to achieve micro-trenching free anisotropic SiC etch profiles, as an evident from a short loop experiment conducted using the Plasmapro. The result of the experiment, shown in Fig. 4.33, suggests that high ICP power (∼2500 W) reduces micro-trenching at the bottom trench corner. This is also achievable with the STS-AOE tool in the Birck Center. An etch performed with the parameters listed in Table 4.7 is shown in Fig. 4.32(b). The SEM analysis shows a nearly perfect 90° anisotropic profile. However, due to STS AOE tool downtime, all Gen-1 tri-gate etch processing was done in the PlasmaPro tool. The SiC short loop etch experiment done in the PlasmaPro tool is discussed next.

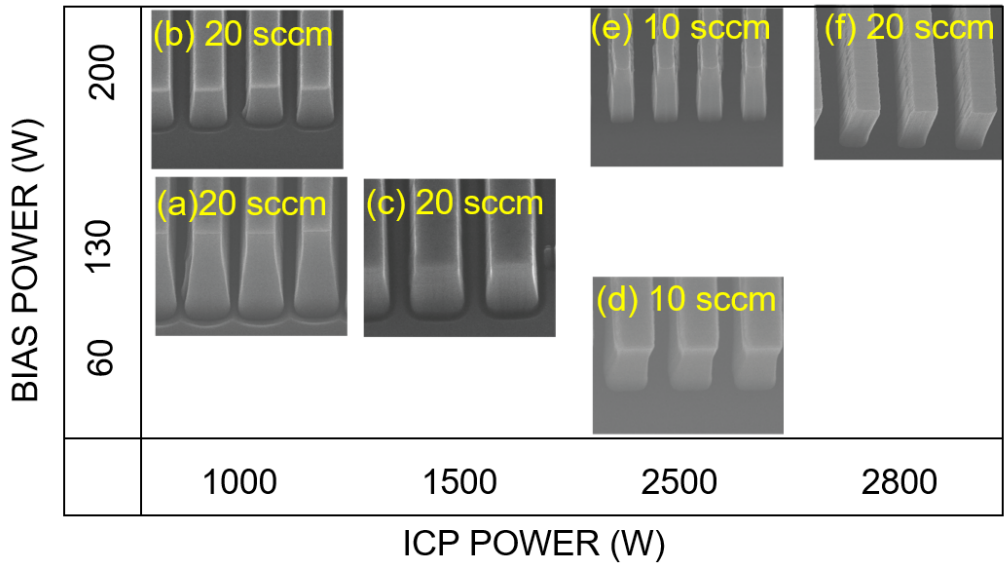


Figure 4.33. Results of a SiC etch study using an SF_6 plasma at a pressure of 5 mTorr with 10 or 20 sccm flow as mentioned in the image. All etches were done in an Oxford PlasmaPro 100 ICP-RIE system at Notre Dame University's nanofabrication facility

In the first iteration of the short loop experiment, a number of 1×1 cm^2 SiC samples were etched in SF_6 plasma with variations in ICP power, bias power, and pressure. It was observed that there was a weak correlation between the etch profile and pressure. The pressure was varied from 2–15 mTorr with almost no effect in the resulting trench shape. In the next short loop experiment, the pressure was held fixed at 5 mTorr pressure. The SF_6 gas flow was also maintained at 10-20 sccm. While keeping these two control parameters fixed, ICP and bias power were varied to optimize the trench etch process. A summary of the experiment is shown in Fig. 4.33. As shown in Fig. 4.33(a), significant micro-trenching was observed in the bottom of the trench at the 1000 W ICP and 130 W bias condition. The micro-trenching is an effect of charged ions attracted to the vicinity of the trench corner, or to the reflection of ions from the sloped sidewall profile. This produces a very sharp corner on the bottom of the trench which can cause undesired oxide breakdown and other reliability issues. The etch process in Fig. 4.33(a) also exhibits a tapering in the profile due to insufficient ion transport into the trench. This effect was alleviated with an increase in bias power to 200 W as shown in Fig. 4.33(b), but the micro-trenching effect was still present. In Fig. 4.33(c),

the micro-trenching was reduced but not eliminated at 1500 W ICP/130 W bias. With continued increasing of ICP power to at or above 2500 W as shown in Fig. 4.33(d), (e), and (f), the micro-trenching was eliminated. With the increase in ICP power the density of radicals increase, and this dilutes the effect of physical ion etching which helps reduce the micro-trenching effect. The slight bowing in trench shape noted in Fig. 4.33(d) can be reduced by increasing the bias power as shown in Fig. 4.33(e) and (f).

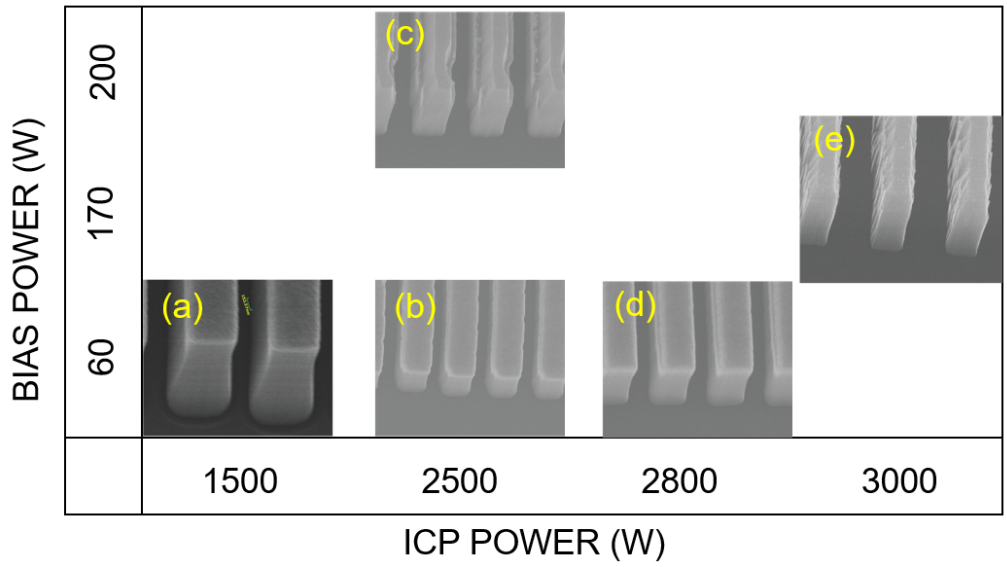


Figure 4.34. Results of a SiC study using an SF_6/Ar (10/20 sccm) plasma at a pressure of 5 mTorr. All etches were done in an Oxford PlasmaPro 100 ICP-RIE system.

Another round of experiments were performed adding Ar to the SF_6 plasma. An advantage of including Ar in the plasma is two-fold: it helps to produce the stable plasma essential for uniform etching, and it etches the sidewall residue to some degree in a physical nature. The inclusion of Ar also dilutes the fluorine, reducing the chemical reaction rate with SiC, thus reducing the etch rate. In this study, the SF_6/Ar flow was kept constant at 10/20 sccm at a pressure of 5 mTorr. Similar to the first split, the ICP and bias power were varied to optimize the trench etch process. A similar trend has been observed in terms of the micro-trenching effect which reduces with the increase of ICP power as shown in Fig. 4.34 (a)-(e). The initial Ni hard mask was not well-defined in Fig. 4.34(c) and (e), which caused the rough trench shape; this should not be confused with the mask erosion caused by the etch process.

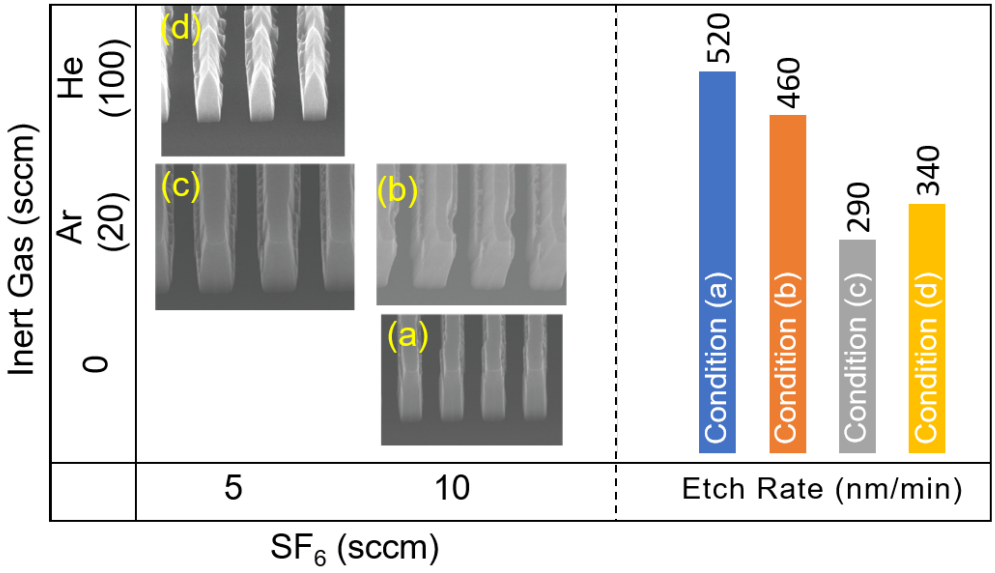


Figure 4.35. Results of a SiC etch study using SF_6 and inert gas plasma at 5 mtorr pressure and 2500/200 W ICP/bias power. All etches were done in an Oxford PlasmaPro 100 ICP-RIE system.

One additional set of experiments was performed to observe the effect of inert gas inclusion in the SF_6 plasma. Figure 4.35(a) shows the trench etch with only SF_6 at a pressure of 5 mTorr and 2500/200 W ICP/bias power. Figure 4.35(b) and (c) show the trench profile with the inclusion of 20 sccm of Ar and either 10 or 5 sccm of SF_6 respectively. In all of the samples shown in Fig. 4.35(a)-(d), the Ni hard mask was not well defined, which introduced some non-uniformity in the profile. However, from this experiment, it can be noted that mask erosion occurs with the inclusion of inert gases at 2500/200 W ICP/bias power condition. An extreme example of this effect is shown in Fig. 4.35(d) where 100 sccm of He is added with 5 sccm SF_6. This is the effect of a highly energetic physical etch charactertistic of inert ions which do not contribute to a chemical reaction. The etch rate was also reduced with the inclusion of inert gas as shown in Fig. 4.35, mainly due to the dilution of the flourine radicals which react with and chemically etch the SiC surface. However, with a similar inert gas flow but with decreased bias power, mask erosion can be prevented as shown in Fig. 4.32(b) which was done in the STS-AOE tool with 2800/100 W ICP/bias power at a pressure of 2 mTorr in SF_6/Ar (10/20 sccm). The detailed etch recipe is listed in Table 4.7.

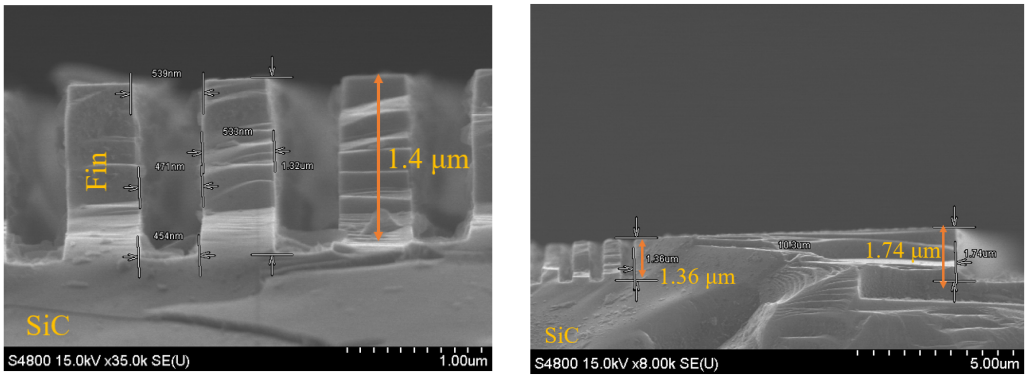
Based on these experiments, all of the Gen-1 tri-gate samples were etched in the Oxford Plasmapro 100 ICP-RIE system in a pure SF_6 plasma as shown in Fig. 4.33(f). The parameters of the etch process are listed in Table 4.8. The tri-gate samples were etched in 2 splits. Samples 1Q3 (thick epi, thick CSL) and 4Q2 (thin epi, thin CSL) were etched in the first split. The other two samples, 2Q4 (thin epi, thick CSL) and 3Q2 (thick epi, thin CSL) were etched in the second split. The split was done intentionally to monitor the trench etch behavior. During these two splits, there was a long downtime for both the in-house STS-AOE and the Oxford PlasmPro at Notre Dame. After the maintenance on the Oxford etcher was completed, the second split of tri-gate samples was etched in similar parameters as shown in Table 4.8, but at a chuck temperature of 20°C for stable tool operation, although the same results were obtained as the first split (performed at 10 °C), in terms of both etch profile and etch rate.

Figure 4.36 shows the cross-section SEM image of a test sample trench etch with the same parameters as listed in Table 4.8. This sample was etched just before the tri-gate sample to monitor the tool before dedicating the tri-gate samples. It shows a significant aspect ratio dependence, as the etch rate in the field area is 500 nm/min while the etch rate in the 0.5 µm wide features is only 357 nm/min. This is mainly due to the lag in transport of ions into the finer featured areas, which correspond to the active region in the tri-gate device. This RIE lag is an inherent issue with plasma etching which can be mitigated to some extent by increasing the pressure during the etch.

Table 4.8. SiC etch recipe in an Oxford Plasmapro 100 ICP-RIE

Parameter	Etch
Gas (sccm)	SF_6 (10)
ICP power (W)	2800
Bias power (W)	200
Pressure (mtorr)	5
V_{DC} (V)	255
Temperature (C)	10°

	SiC wide feature	SiC narrow feature (0.5 µm)
Etch rate (nm/min)	500	357



(a) (b)

Figure 4.36. Cross-section SEM image of the trench etch process in a test SiC sample etched with the parameters listed in Table 4.8: (a) The etch profile in a dense 0.5 µm pattern, and (b) Aspect ratio dependence or RIE lag effect in the etch recipe.

In some iterations of the trench etch experiment, the samples were etched at a higher (15 mTorr) pressure, but no observable difference is found in terms of RIE lag. The pressure was not further increased as it may affect the trench shape anisotropy. The RIE lag effect only affects a few features in the process control module in the tri-gate device mask set. If a full 2 µm deep etch were performed in the 0.5 µm dense patterns, the 1.7×0.7 mm^2 area containing test MOSCAPs would be sacrificed. There are also a few features narrower than 0.5 µm which are also affected. Therefore the RIE lag issue in the trench etch process is not a major concern. However, in the first split, the tri-gate samples (1Q3 and 4Q2) were etched to only 1.5 µm in the active area to preserve the wide trench areas in the PCM. As a result, the increase in effective channel width is compromised. On the other hand, in the second split the tri-gate samples (2Q4, 3Q2) were etched a little longer to achieve a trench depth of nearly 2 µm, while potentially etching the larger areas beyond the n-source (2.2 µm) or p-well (2.7 µm) junction depths which results in losing a few test devices in PCM region. The trench depth information on different tri-gate devices is listed in the Table 4.9.

Table 4.9. Tri-gate Gen-1 sample trench depth

Wafer #	Drift layer thickness (µm)	CSL thickness (µm)	Given Name	Trench depth (µm)
PU 391	8.3	3.1	1Q3	1.5 µm
PU 397	5.2	3.2	2Q4	1.9 µm
PU 393	8.5	2.5	3Q2	1.9 µm
PU 399	5.4	2.6	4Q2	1.5 µm

Figure 4.37 illustrates the process flow of the SiC ICP-RIE plasma etch. The tri-gate sample was etched after the n-source, p-well, and p+ implants were done and the implant anneal completed. Prior to etching, the sample was cleaned in 3 solvents (toluene, acetone, and methanol) and a full RCA [31] clean was performed. A thin layer of oxide was grown on the SiC surface to prevent any unwanted surface contamination from the nickel hard mask. An e-beam and optical dual lithography was performed to create the trench pattern. First e-beam lithography with a 400 nm thick 950K PMMA A6 e-beam resist was done, and an e-beam evaporated Ti/Ni (20/200 nm) metal layer was lifted-off. The samples were first cleaned in the same 3 solvents and dehydrated at 180°C for 2 min. The e-beam resist was spun at 4000 rpm for 45 sec with a 2 sec ramp to achieve 400 nm thick resist. Then the resist was soft baked at 180°C for 3 min. The baked resist was exposed in the JEOL JBX 8100FS e-beam lithography system at an energy of 100 kV and a beam current of 30 nA for a base dose of 1300 µC/cm^2. A proximity effect correction was applied to obtain an accurate and uniform pattern. The exposed resist was developed in a pre-made solution of MIBK:IPA (1:3) for 1 min, followed by rinsing in IPA for 45 sec. The developed resist was then loaded in the Branson barrel etcher tool for resist ashing in an Ar/O_2 plasma (120/6 sccm) at 100 W for 20 sec. This was followed by the deposition of a 15/200 nm thick Ti/Ni metal stack in a standard e-beam metal evaporation chamber. The metal was lifted off in a hot bath of PG remover for 6-8 hr. PG remover residue was cleaned in acetone and IPA by soaking the sample in each solution for 10 min. Another 3 solvent clean was performed, and after sample dehydration, a 10 µm thick AZ9260 resist was deposited (∼2000 rpm spin for 30 sec). The resist was then exposed in an MJB3 proximity contact mask aligner at an optical power density of 10 mW/cm^2 for 1 min. The exposed resist was then developed in an AZ400K:DI water (80:300 mL) solution for 3 min 30 sec. The developed photoresist was then loaded

in the Branson ashing system for 1 min to clean any resist residue. The sample was then bonded to a 4″ Si carrier wafer with Santovac on a 70°C hot plate. The viscosity of Santovac is very low, so a few drops of Santovac is sufficient to cover the entire back side. The sample was then loaded into the Oxford PlasmaPro 100 ICP-RIE tool and etched in a multiple short duration steps. The etch parameters are listed in Table 4.8, and a cross-section FIB image of tri-gate sample 4Q2 is shown in Fig. 4.38.

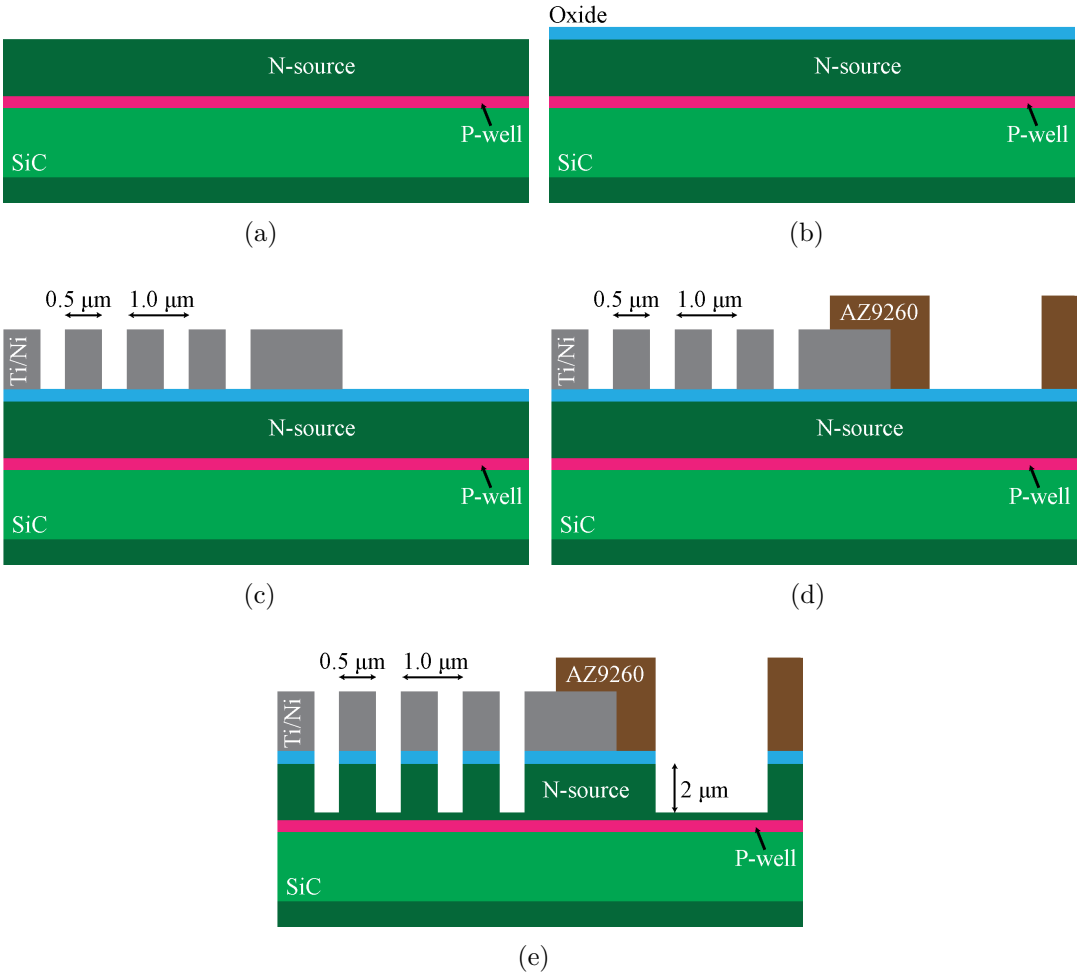


Figure 4.37. Trench etch process flow: (a) Wafer with n-source and p-well implant; (b) Thin layer of thermally grown oxide; (c) E-beam lithography and Ti/Ni (10/200 nm) metal lift off in the active region; (d) 8–10 µm thick AZ9260 photoresist pattern in the field and PCM regions; (e) SiC plasma etch.

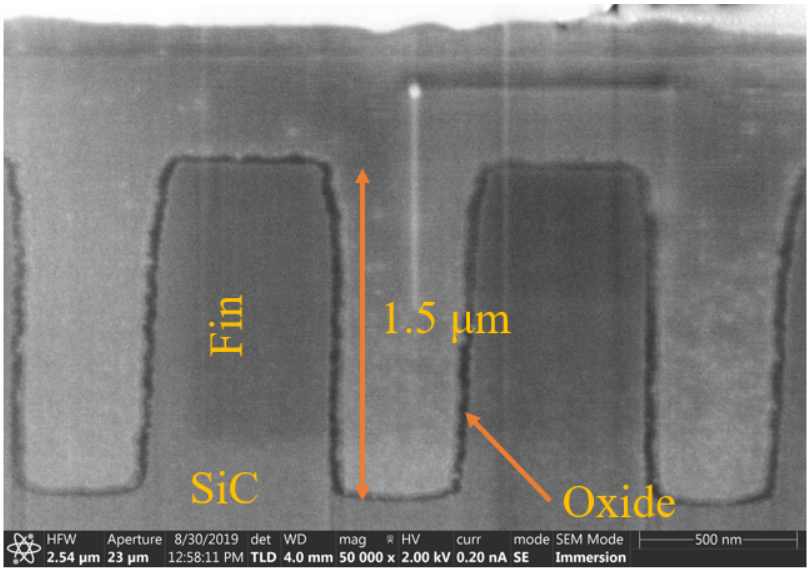


Figure 4.38. Cross-section FIB image of the trench profile in the 4Q2 tri-gate sample.

4.7 Field Oxide

The trench etch process was followed by the growth of a 1 µm thick field oxide. Field oxide is an important feature that protects the wafer from physical and chemical contamination. Random electrically active chemical impurities can affect the device in many ways such as surface inversion of the p-well area in the field area to produce an parasitic electrical path between source and drain, etc. The effect of these impurities can be minimized by the formation of a thick field oxide. In addition, the presence of a thick field oxide underneath the gate pad makes it mechanically robust during probing or wirebonding, and prevents scratches on SiC surface in the field area. However, the formation and patterning of field oxide is not trivial in the tri-gate device, mainly because of the high aspect ratio gate trenches.

The formation of a field oxide was performed by multiple steps of polysilicon growth and full oxidation. First, the sample with trenches was RCA cleaned [31]. Then polysilicon was grown at 630°C (∼580 mTorr pressure) for about 12 min. The polysilicon growth rate under these conditions was about 13 nm/min, forming around 150 nm of polysilicon in 12 min. This poly was then oxidized in a high temperature furnace running at 1050°C in a wet pyrogenic chamber. The oxidation time was calibrated prior to this run by performing a polysilicon deposition and oxidation experiment. To ensure full oxidation of this polysili-

con layer, the oxidation time used was longer than required. This formed a ∼320 nm thick oxide on the surface. This process of polysilicon growth and oxidation was repeated 2 more times to achieve a total oxide thickness of ∼1 µm. The first two cycles of the polysilicon oxidation process were followed by a 2 hr NO anneal at 1175 ℃ to ensure a good quality oxide-semiconductor interface which is required to achieve good off-state operation. The multi step polysilicon deposition and oxidation process was done mainly to ensure complete oxidation of the polysilicon layer, which is harder than the one step 1 µm polysilicon oxidation process. But later it was found that even in the 3 step process, there was a trace of unoxidized polysilicon. Therefore this field oxide process was not used after the first run of Gen-1 tri-gate sample fabrication. However, if a reliable thick oxide deposition tool such as PECVD were to become available in the facility, a full 1 µm thick oxide could be grown, but patterning the oxide would still be challenging due to the presence of trenched structure.
After the field oxide deposition, a thick AZ9260 photoresist was patterned and the oxide was etched in a BOE solution. The complete process flow is shown pictorially in Fig. 4.39.

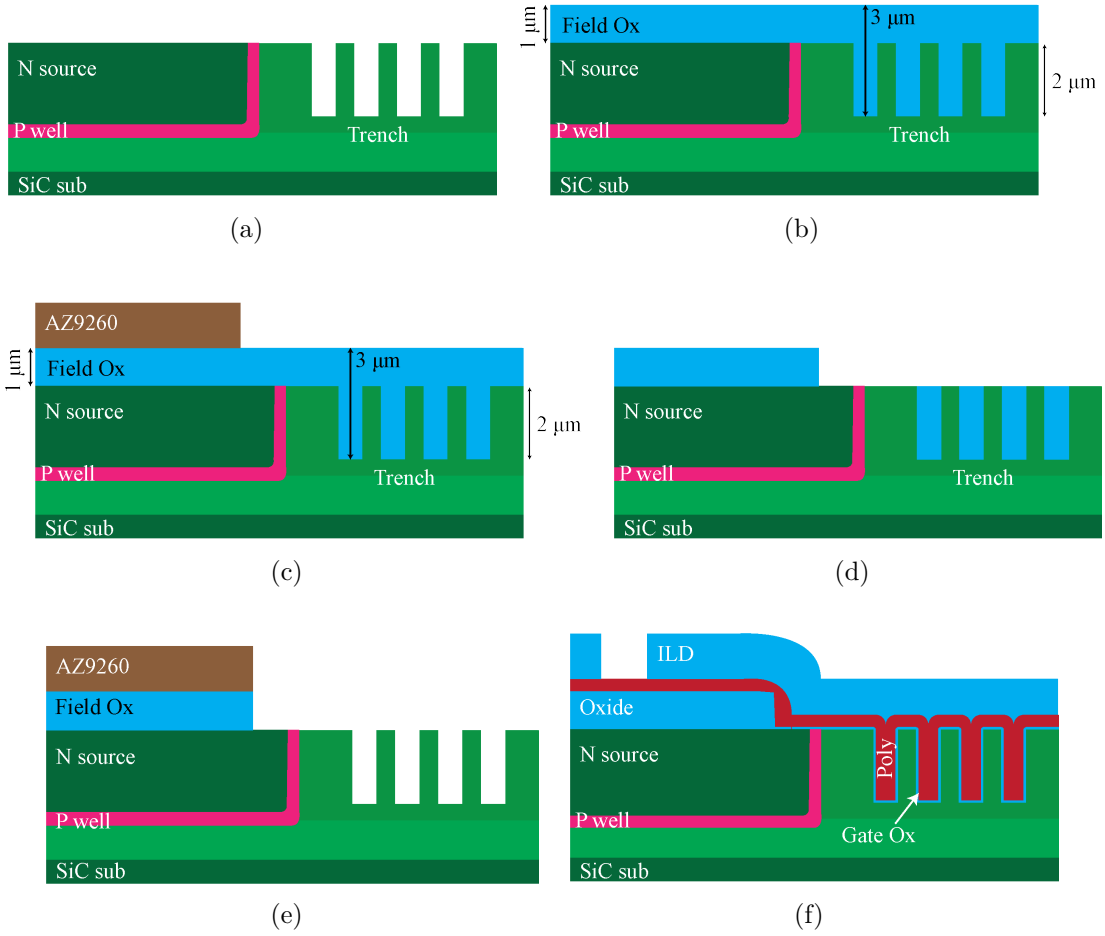


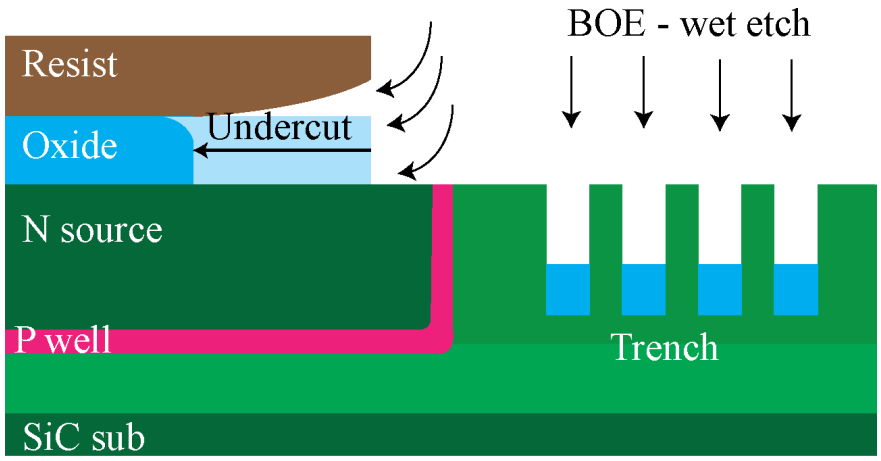
Figure 4.39. Field oxide process flow: (a) The tri-gate sample with trench features; (b) Depostion of a 1 µm thick field oxide; (c) Photoresist patterning; (d) Field oxide etch (either wet or dry); (e) Field oxide etch continuation to clear oxide in the trench, and (f) The device after gate oxide and poly deposition, and after ILD formation

Table 4.10. SiO_2 etch recipe in E620 Panasonic ICP-RIE

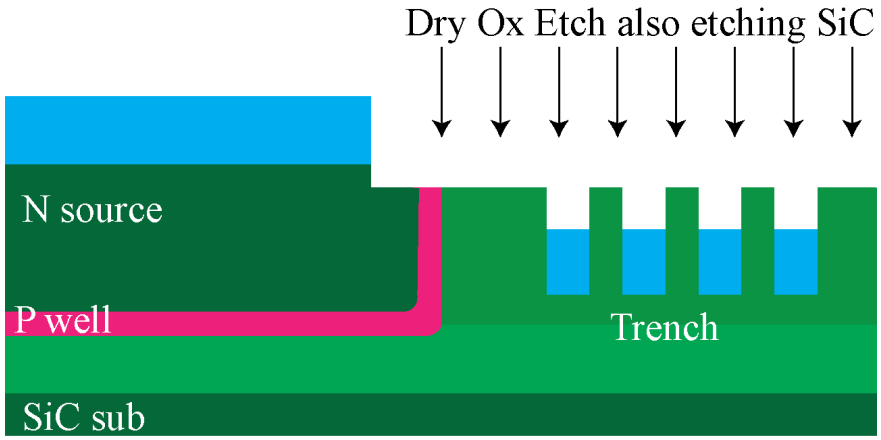
Parameter	Etch
Gas (sccm)	CF_4/CHF_3 (10/40)
ICP power (W)	650
Bias power (W)	50
Pressure (Pa)	1

	SiO_2	SiC	Si	Photoresist
Etch rate (nm/min)	87	14	22	56

However, resist patterning and etching the field oxide over a high aspect ratio trench feature is not trivial. Deposition of a 1 µm thick oxide layer in the field area forms a 2.5 µm thick oxide layer over the 1.5 µm deep trenches. To chemically etch this thickness of oxide, a 40 min soak in a BOE solution is required, which etches oxide at a rate of ∼70-80 nm/min. Photoresists such as AZ1518 or AZ9260 show very high selectivity to this etch, but can suffer from poor adhesion to the underlying surface. This can allow the etchant to diffuse underneath the resist and eventually peel the layer off [44]. This also etches the oxide in the protected area as shown in Fig. 4.40(a) and Fig. 4.41. The effect was not significant while etching 0.5–0.7 µm of oxide, but becomes pronounced when etching over 1 µm thick oxide. In an attempt to solve this problem, different cleaning procedures, hard baking conditions, and surface adhesion promoter (HMDS) application methods were attempted, without success. The surface promoter HMDS has traditionally been spun on the surface and soft-baked like photoresist. A vapor deposition process in a desiccator would be more appropriate since the setup is not currently available in the facility this has not yet been tried. Another option is an AZ1500 series surface promoter from Microchemical. Another approach to solve this problem would be to etch the oxide in 2 step process. A significant portion of the etch can first be done using a dry plasma process, followed by a short wet etch in BOE as a soft landing to prevent plasma related damage to the surface. To develop this process in a tri-gate device requires about 2 µm of oxide RIE etch followed by a wet 0.5 µm chemical etch. However the SiC surface on top of the fin is uncovered after 1 µm of oxide etching, exposing SiC the plasma which etches SiC at a rate of 14 nm/min assuming the parameters listed in Table 4.10. As a result, to etch 2 µm oxide in the plasma condition, ∼170 nm of SiC would be consumed. This issue is depicted in Fig. 4.40(b). This not only would reduce the trench depth, but would also thin the highly doped implanted source n^+ and p^+ regions which might result in an increased contact resistance or to an extreme a drain–source electrical short with exhaustion of p^+ region in the area where it separates the CSL and source regions.

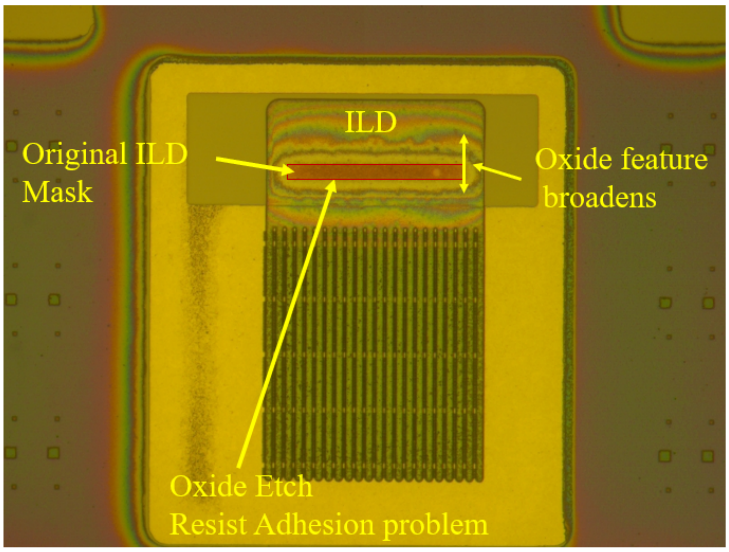


(a)

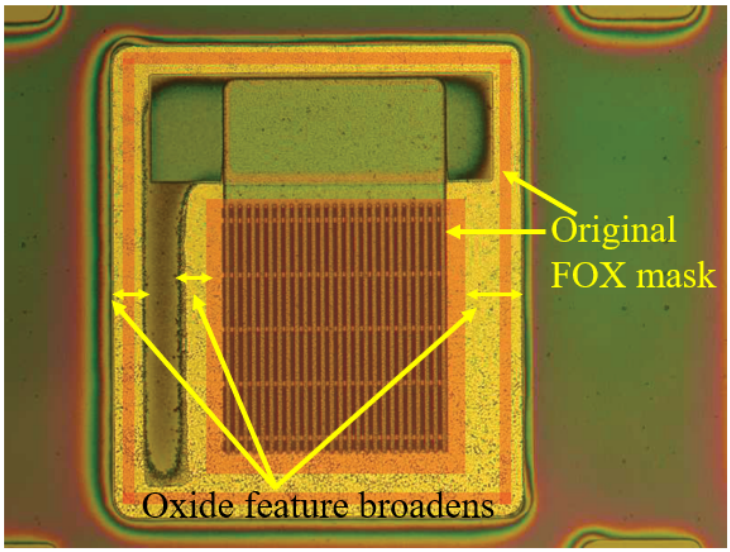


(b)

Figure 4.40. Field oxide process concern: (a) BOE wet etch resist to surface adhesion issue - aggressive undercut in the pattern, and (b) Field oxide dry etch according to the Table 4.10 consumes SiC.



(a)



(b)

Figure 4.41. Wet etch of thick oxide with Photoresist mask shows oxide undercut: (a) FOX pattern and etch, red region shows original mask position, and (b) ILD pattern and etch, red region shows original mask position.

Due to these complexities, field oxide was not used in the second fabrication run of the tri-gate devices (sample 2Q4) . As a result, the field area is only protected by a 50 nm oxide deposited during the gate oxide process. A complete cross-section diagram with and without field oxide in samples 4Q2 and 2Q4, respectively, is shown in Fig. 4.42.

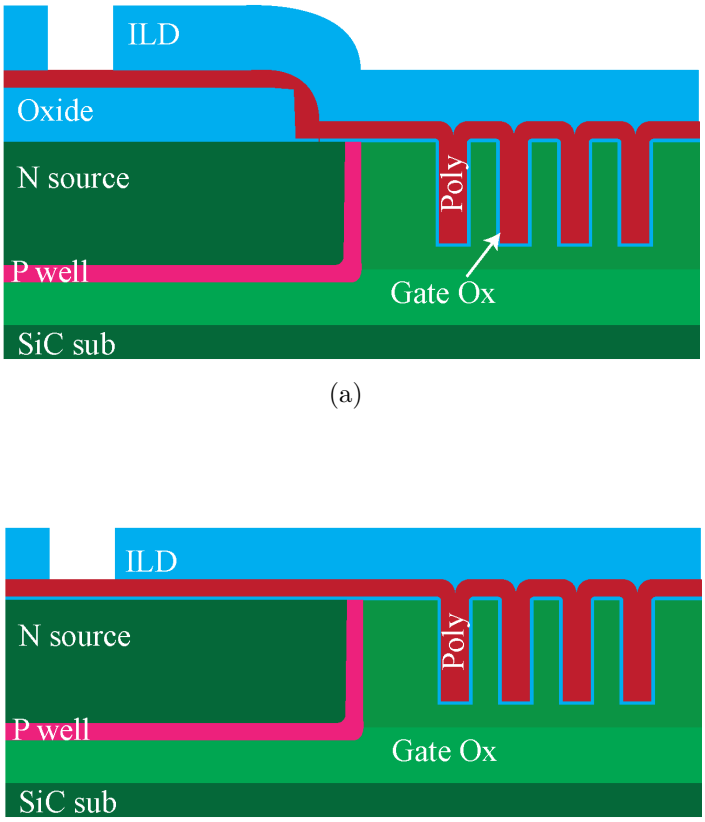


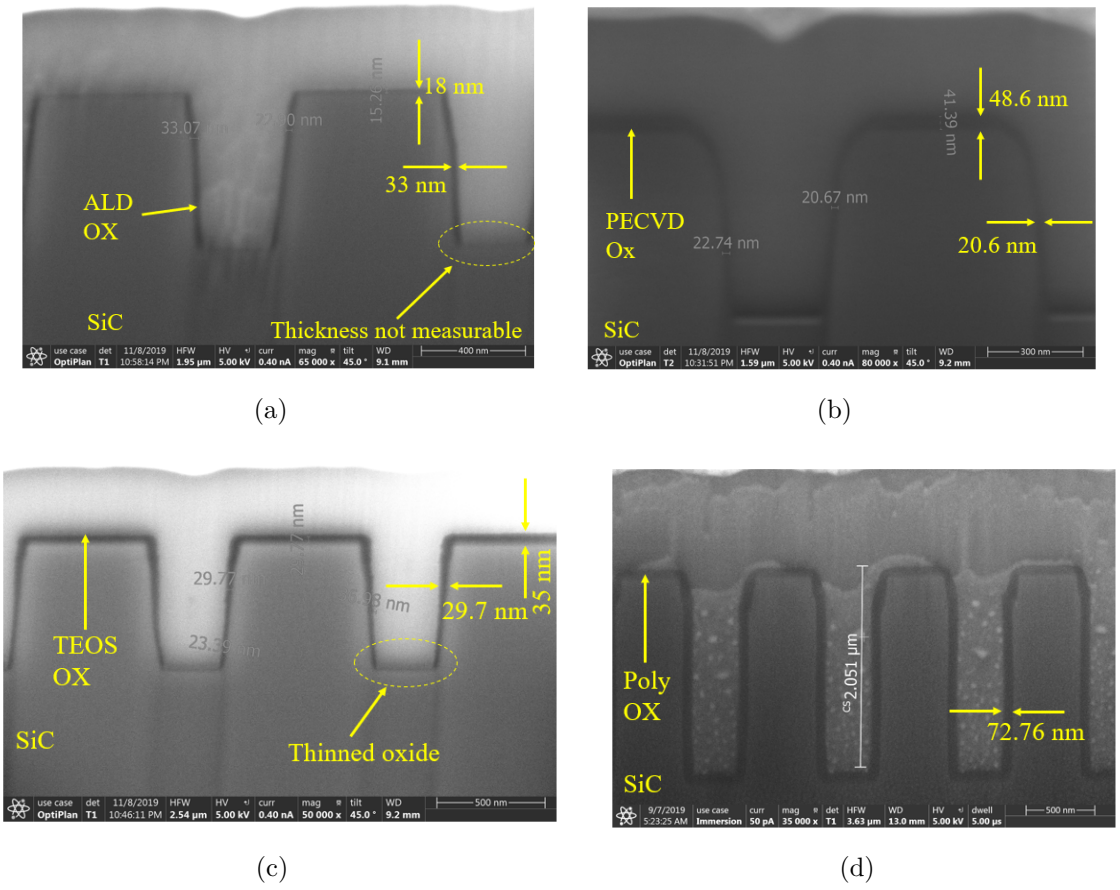
Figure 4.42. Tri-gate device with and without field oxide: (a) The tri-gate sample with field oxide feature, and (b) without field oxide.

The resist adhesion problem can be solved in a 2 step etch process combining an initial plasma etch and a short soft landing wet chemical etch. Consumption of SiC during the plasma etch can be prevented by swapping the trench etch and field oxide deposition processes. In this approach, after the implantation and anneal, a 1 µm thick field oxide deposition and patterning would be completed. After the definition of field oxide, the trench etch process as described in the previous section can be performed. However, if a H_2 etch

is required after the trench etch at 1600-1700°C, the prior deposited field oxide would be melted, which makes this alternative approach infeasible.

4.8 Gate Oxide

The gate oxide in SiC power DMOSFETs is usually formed by thermal oxidation at 1100–1200°C. The thermally grown oxide exhibits good stoichiometric quality, but has a high trap density at the SiO_2–SiC interface which limits the channel mobility. A high temperature anneal in NO usually follows thermal oxidation to improve the interface [45]. Despite performing the post-oxidation anneal, the electron mobility is still an order of magnitude lower than the bulk mobility, typically around 30 $cm^2/(V \cdot s)$. The issue is more challenging if the oxide has to be deposited instead of thermally grown. A deposited oxide process must be used in the tri-gate MOSFET, since thermal oxidation of SiC is highly anisotropic on the different faces. The oxide on the a-face normally grows 3–5× faster than on the Si-face, which will create a varying threshold voltage across the different surfaces of a tri-gate MOSFET. Therefore different oxide deposition techniques were investigated. A uniform oxide thickness was achieved by oxidizing a thin deposited polysilicon layer as shown in Fig. 4.43(d).



(a) (b)

(c) (d)

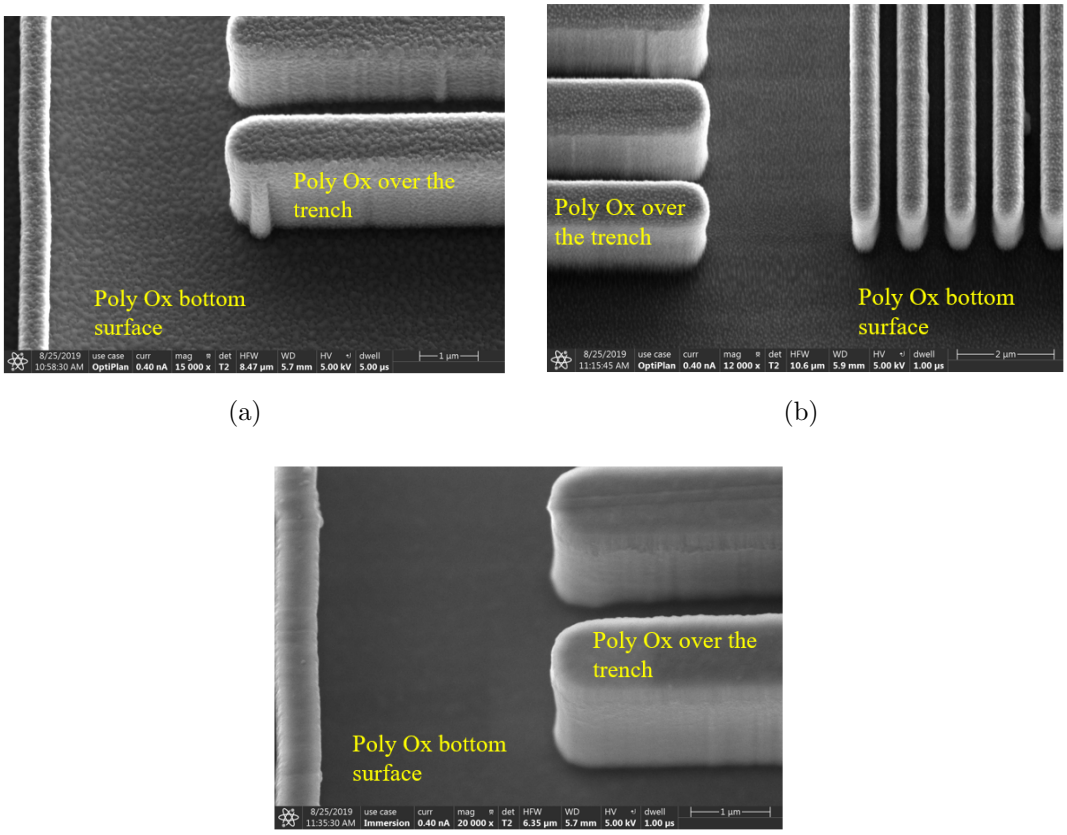
Figure 4.43. Different oxide deposition techniques: (a) Atomic layer deposition (ALD); (b) Plasma enhance chemical vapor deposition (PECVD); (c) TEOS-based LPCVD deposition; (d) Polysilicon LPCVD deposition and oxidation.

A different oxidation techniques were investigated as shown in Fig. 4.43. Atomic layer deposition (ALD), Plasma enhanced vapor deposition (PECVD), TEOS-based LPCVD deposition, and polysilicon LPCVD deposition and oxidation are compared. A uniform oxide thickness on different faces was only found in polysilicon oxidation process where other tenchinques suffer from non-uniformity. More detailed process optimization experiments are required for ALD, PECVD, and TEOS based oxide deposition techniques to improve uniformity and electrical characteristics. In this work, such development work was not pursued, and the polysilicon oxidation technique was selected.

An amorphous Si, rather than a polysilicon layer, was found to produce a smooth uniform oxide thickness after high temperature oxidation. On the other hand, large grain polysilicon

is inherently rough, and thus oxidized polysilicon creates a rough oxide layer which is not suitable for the purpose of a MOSFET gate oxide. The boundary between the formation of amorphous Si and polysilicon depends strongly on the deposition temperature. The first completed tri-gate device (Sample 4Q2) failed due to an electrical short between gate and source which was the result of an extremely rough gate oxide as shown in Fig. 4.38. To achieve a smoother oxide, a short loop experiment was performed to ensure amorphous Si deposition.

In this short loop experiment, the polysilicon deposition temperature was investigated on six 1×1 cm^2 size SiC test samples patterned and etched with a mask shown in Fig. 4.31. The samples were grouped into 3 categories, each of which contained 2 samples loaded together to deposit polysilicon or amorphous Si at a certain temperature. The deposition temperature and time for categories 1, 2, and 3 were 630°C for 2 min, 605°C for 6 min, and 580°C for 10 min respectively. One sample from each category was used to analyze surface roughness in in the SEM, with the results are shown in Fig. 4.44. The high polysilicon roughness deposited at 630°C is evident in Fig. 4.44(a). Polysilicon deposited at 605°C also showed roughness as shown in Fig. 4.44(b), but to a lesser extent. Finally, the material deposited 580°C is nearly amorphous in nature, with a very smooth surface in Fig. 4.44(c). It appears that 600-605 is the boundary between large grain polysilicon and amorphous Si. All depositions were performed at a pressure of 580 mTorr.

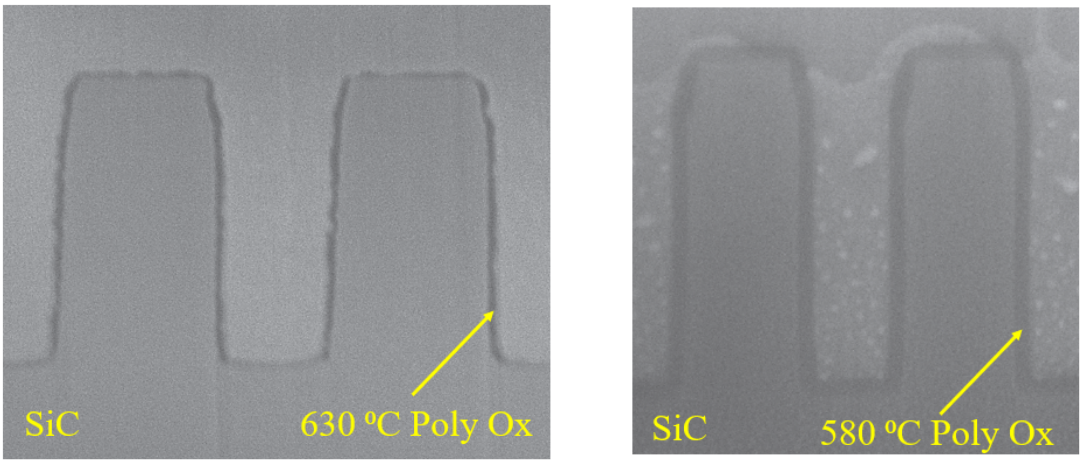


(a) (b)

(c)

Figure 4.44. SEM images of oxidized polysilicon, with the poly deposited at different temperatures, and wet oxidation was done at 1100°C for 5 min: (a) 630°C; (b) 605°C, and (c) 580°C.

Other samples from each category were wet oxidized at 1100°C and annealed for 2 hr in NO at 1175°C. A doped polysilicon gate was then deposited and patterned on these samples to perform electrical characterization on planar and trench MOSCAPs. The result of these electrical measurements will be discussed in the next chapter. The SEM analysis of these wafers reveals a very rough gate oxide in the sample where polysilicon was deposited at 630°C, and a smooth and uniform gate oxide in the sample where amorphous Si was deposited at 580°C. These results are shown in Fig. 4.45. As mentioned earlier, the pressure during LPCVD polysilicon deposition was maintained at between 580–600 mTorr, which is higher than the recommended value (150 mTorr), and is suspected to be related to poor vacuum pump condition.



(a) (b)

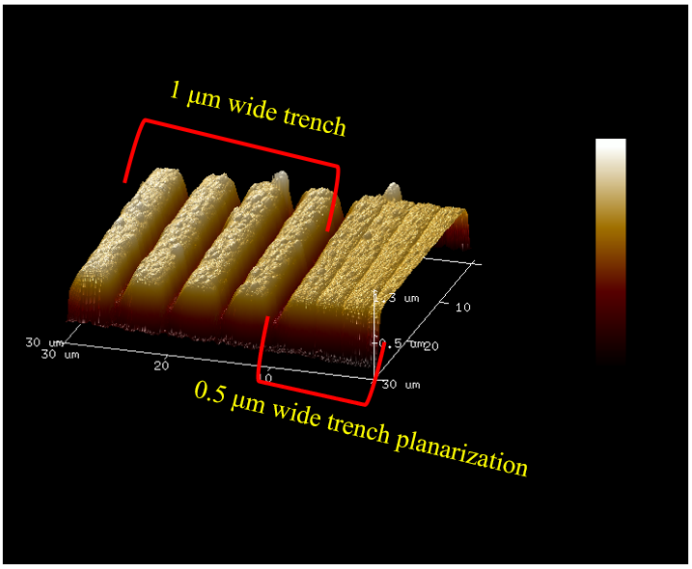
Figure 4.45. SEM cross-section of trench structures with 630°C and 580°C poly deposition and 1100°C wet oxidation: (a) Polysilicon deposited at 630°C, and (b) Polysilicon deposited at 580°C.

4.9 Polysilicon Gate

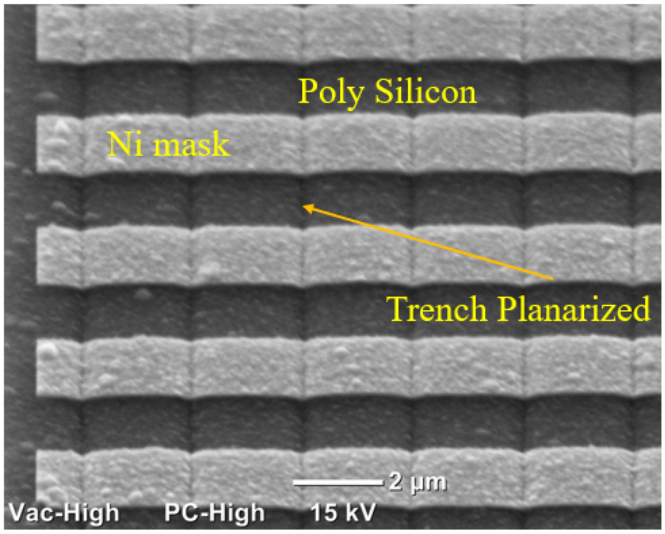
Heavily phosphorus doped n-type polysilicon is used as the gate in the tri-gate device. The gate polysilicon was deposited, with no wait time, after the post oxidation NO anneal. In this section, the polysilicon deposition, doping and patterning processes will be discussed in detail.

A 1 µm polysilicon layer was deposited in an LPCVD ProTemp furnace at a pressure of ∼580 mTorr and 630°C for 80–85 min for a deposition rate of 13 nm/min. The deposited polysilicon layer planarized the trench as shown in Fig. 4.46. Half of the 1 µm thick polysilicon was consumed during 1 µm formation of the thermally grown oxide which serves as an interlayer dielectric, which will be discussed in detail in the next section. The remaining 0.5 µm thick polysilicon was used for as the MOSFET gate. The deposited polysilicon was then doped using a phosphorus spin-on dopant (SOD) P509, purchased from Filmtronics. According to the specification, the SOD layer should result in a sheet resistance of ∼5 **Ω**/□, although it depends on various parameters like polysilicon thickness, anneal conditions, SOD chemical storage and usage conditions, etc. The SOD bottle is usually stored in a refrigerator at 4°C but even under these conditions, deterioration of the chemical was observed which

resulted in in increased polysilicon sheet resistivity of more than 1 k$\Omega/\square$. This problem was faced in sample 1Q3 in the first run of tri-gate devices. So certain precautions were taken in terms of usage and storage to prevent premature aging of chemical. First, the SOD bottle was subdivided into a number of smaller (4 mL) high density polyethylene (HDP) bottles to reduce handling and prevent contamination of the original bottle. Second, a plastic pipette was used while handling this chemical.



(a)



(b)

Figure 4.46. AFM and SEM images of polysilicon deposited over trench features in a test sample: (a) AFM image of planarization achieved by 0.47 µm polysilicon deposited over 2 µm deep 0.5 µm wide trench features, and (b) SEM image of polysilicon deposited over trenches, including metal gate etch mask.

In the process flow, after depositing 1 µm of polysilicon, the sample was first cleaned in piranha (1:1 of 98% H_2SO_4 : 30% H_2O_2) for 5 min, BOE for 3 min, piranha for 3 min, and finally rinsed in DI water for 2–5 min. The second piranha step is recommended by Filmtron-

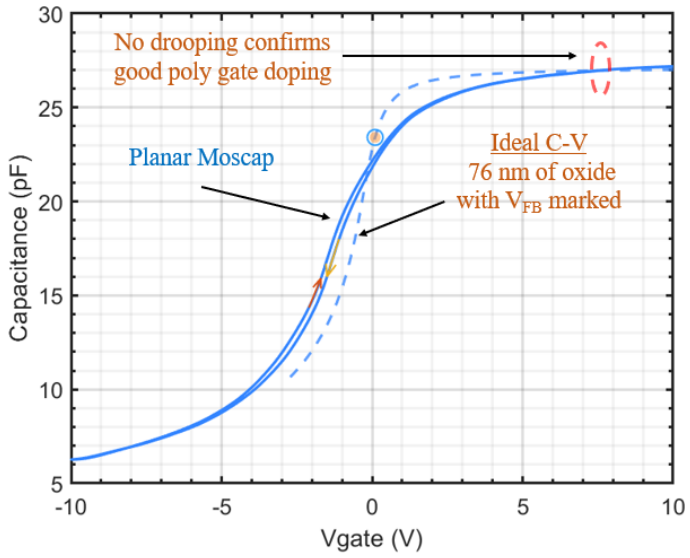
ics to make the sample hydrophilic for proper SOD wetting during spinning, although this may not apply to SiC, which is hydrophilic even after soaking in BOE. The sample was then dehydrated for 5 min at 200°C on a hot plate. The sample was cooled for ∼2 min in the ambient before spinning SOD from a 4 mL HDP bottle, which had been warmed up for 1.5–2 hr to reach the ambient temperature. During the SOD spinning, every surface of the spinner tool was covered by aluminum foil to prevent any corrosion caused by SOD. The chemical was drawn from the bottle using a plastic pipette and spun on the sample in 3 steps – (i) with a 2 sec ramp, spin at 500 rpm for 2 sec, (ii) with a 2 sec ramp, spin at 3000 rpm for 20 sec, and (iii) come to rest in 2 sec. The deposited SOD layer was then baked at 200°C for 20 min and loaded immediately in a high temperature furnace at 850°C. It takes ∼1 hr for the furnace tube to reach at this temperature, so the process was planned accordingly to minimize any wait time between hot plate baking and high temperature furnace loading. The temperature of the diffusion tube was then ramped up to 1000°C with a rate of 4 °C/min. The SOD diffusion process was performed at 1000°C for 2 hr in a 75% N_2 and 25% O_2 ambient. The tube was then cooled to 850°C at a rate of 2.5°C/min before unloading the sample from the hot stage. A thin layer of phosposilicate glass is formed on the surface during the process, which was stripped in BOE for 5 min.

The polysilicon doping was investigated both with 4 point probe sheet resistance and MOSCAP C-V measurements on a 3 µm thick polysilicon gated SiC test sample, which was also loaded in the furnace with the tri-gate sample during the dopant diffusion process. A Jandel 4 point probe measurement in was done on a blanket poly coated sample, which had a sheet resistance in a range of 7–13 $\Omega/\square$. The poly doping process was also verified by fabricating MOSCAPs on both planar and trench areas on the epitaxially grown SiC test sample. The polysilicon patterning was performed with an optically defined AZ9260 mask, and polysilicon dry etching in an STS-ASE with the conditions shown in Table 4.3. The backside oxide on the sample was stripped in BOE for 5 min while protecting the front side with an AZ9260 photoresist coating. To clean any backside polymer formations or strip any additional remaining oxide, the sample was etched in a Jupiter RIE tool according to the parameters listed in Table 4.11 for 1 min, followed by a 100 W Branson etch in a Ar/O_2 (120/6 sccm) plasma for 2 min, and finally another BOE etch for 2 min. The C-V measurement

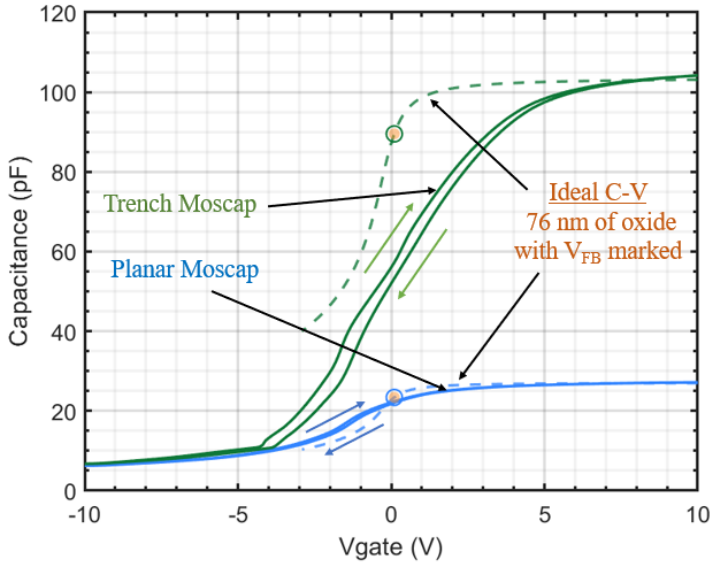
at 100 kHz of both the planar and trench MOSCAPs showed no drooping in accumulation, which confirms a highly doped polysilicon gate was formed as shown in Fig. 4.47. The C-V measurement of the SiC test sample was also used to investigate the gate oxide quality as described in the previous section.

Table 4.11. Jupiter RIE etch recipe

Parameter	Etch		
Gas (sccm)	SF_6/Ar (20/10)		
ICP power (W)	100		
Pressure (mtorr)	215		
	SiC	SiO_2	Si
Etch rate (nm/min)	28	40	2300



(a)



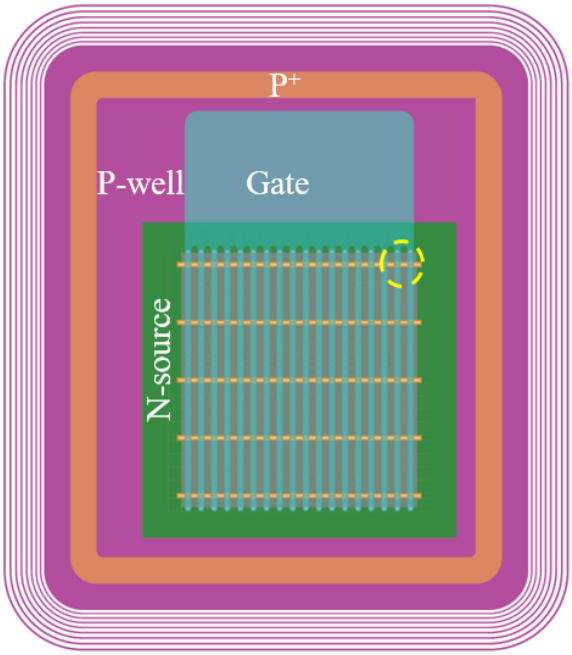
(b)

Figure 4.47. C-V measurement on a test sample from the PU431 wafer showing no drooping in the accumulation capacitance at high gate voltages, confirming good polysilicon gate doping: (a) Planar MOSCAP with a 76 nm oxide and an area of 6×10^{-4} cm^2, and (b) a comparison of the planar MOSCAP with a 2 µm deep trench MOSCAP having a total area of 23×10^{-4} cm^2.

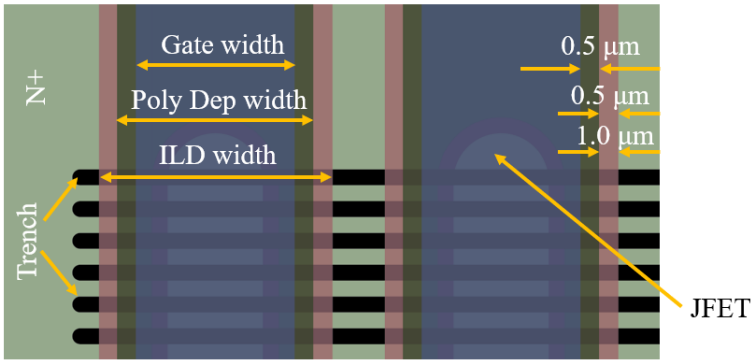
The next step in the tri-gate device fabrication process is the patterning and etching of the polysilicon gate. Based on the design layout, the drawn dimensions of gate source overlap and the ILD thickness are 0.5 µm and 1 µm respectively. Self-aligned gate-source isolation is

implemented by thermally oxidizing a portion of gate polysilicon at high temperature. This oxide is called the inter layer dielectric (ILD). To accommodate this layer, the gate patterning process includes an extra 0.5 µm of polysilicon on both sides of the gate fingers beyond the gate source overlap as shown in Fig. 4.48. Initially, a so-called bird's beak effect, or lateral diffusion of oxidizing species underneath the edges of the polysilicon layer and subsequent expansion of the gate oxide along the edges of the gate was not taken into account. This effect was later found experimentally, and explored by the author's colleague Dr. Ramamurthy, in a process simulation using the Sentaurus Process TCAD software as shown in Fig. 4.49. To first order, with perfect lithographic alignment, this effect increases the oxide thickness in the gate source overlap region. By itself, this does not have any significant detrimental effect. However, in the case of any lithographic misalignment the bird's beak effect can impact the oxide in the channel region, which can cause less gate electrostatic control over channel and a higher threshold voltage, leading to increased channel resistance. Therefore, the design rules and layout need a modification to take this effect into account. To accommodate such a modification, two approaches were followed: (i) the drawn dimensions of the gate source overlap were increased for higher process margins, and (ii) a slight thinner 0.8–0.9 µm ILD oxide was grown, which reduces the penetration of the bird's beak effect into the active channel region. However, both of these approaches introduce a secondary undesirable effect. In the first approach, increasing the drawn gate source overlap dimension decreases the source contact length for a given pitch, which potentially increases the source resistance. Since the gate patterning is done in a high resolution e-beam lithography tool, the gate source overlap only needs to increase by 0.1–0.2 µm, which will reduce the source contact width by about 20%. This reduction in source width may not contribute significantly to the total specific on-resistance of the device, since the contact resistivity is found to be very low, in the mid $1 \times 10^{-6}\ \Omega \cdot \mathrm{cm}^2$ range. In the second approach, the thinner dielectric imposes a risk in terms of device reliability and gate-source isolation. In particular, it may create a risk of gate-source shorts caused by metal diffusion through the defects in the thinner dielectric during the ohmic anneal process. However, a two step ohmic anneal process where the unreacted metal is etched away after first step can prevent this possibility. This ohmic anneal process will be discussed in Section 4.11. Therefore both of these changes were made

in the tri-gate fabrication process. In sample 1Q3 (later not completed due to a poly doping issue), the original 0.5 µm gate-source overlap is maintained but a 0.8 µm thick ILD layer was grown. On the other hand, in sample 4Q2, the gate-source overlap is extended to 0.75 µm with a full 1 µm thick ILD. In the second run, in sample 2Q4, both approaches were applied by extending the gate-source overlap to 0.6 µm and thinning the ILD dielectric to 0.9 µm.

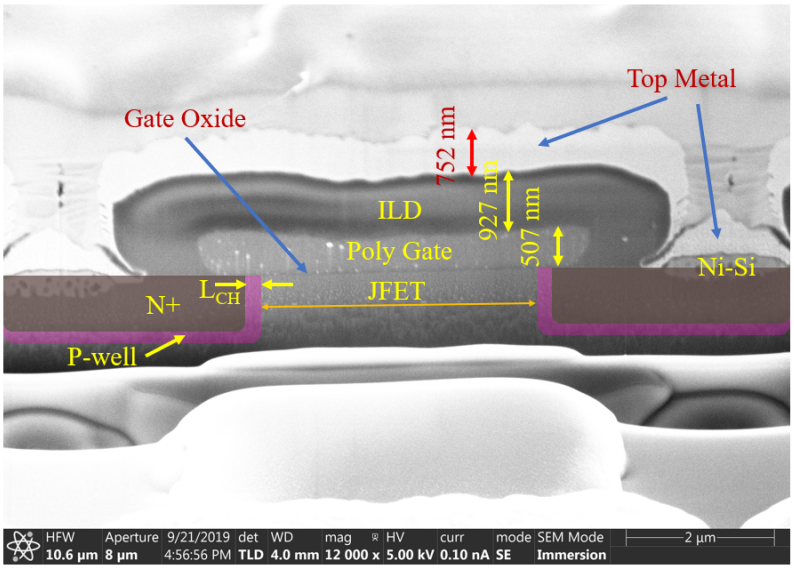


(a)

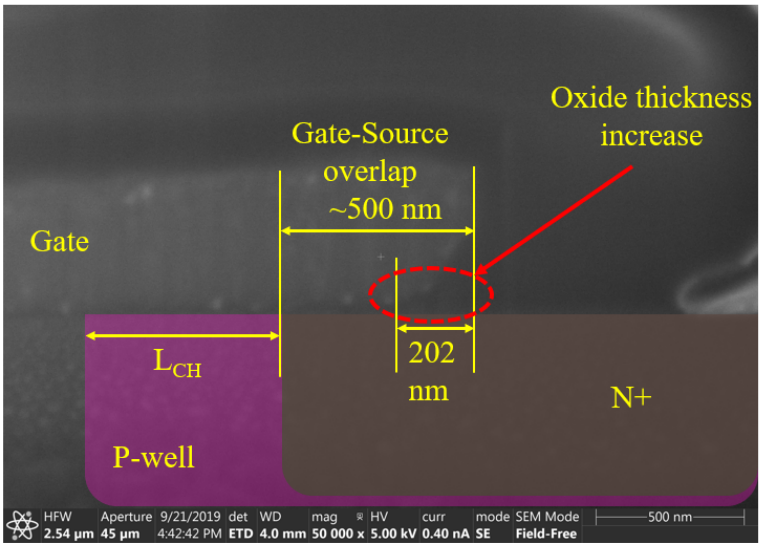


(b)

Figure 4.48. Mask layout showing the dimensions of the deposited polysilicon, ILD, and final gate: (a) Overall tri-gate device, and (b) Highlighted region in (a) showing the drawn dimensions.



(a)



(b)

Figure 4.49. SEM images on tri-gate 4Q2 sample showing the increased lateral oxidation during ILD formation (the dimensions not marked with ∼ were measured in the SEM): (a) SEM cross-section on a 4Q2 planar DMOSFET, and (b) Closer view of (a) showing the bird's beak effect.

In the first fabrication run of tri-gate MOSFETs (sample 4Q2), the polysilicon gate was patterned in a single e-beam lithography step using AllResist CSAR resist. The sample was first cleaned by soaking for 5 min each in toluene, acetone, methanol, and DI water. The

sample was then dehydrated at 150°C for 5 min. A 400 nm thick CSAR resist was spun at 4000 rpm for 60 sec and soft baked at 150°C for 3 min. The resist was then exposed at an accelerating voltage of 100 kV in a JEOL e-beam lithography tool with a dose of 280 µC/cm^2 and a beam current of 200 nA. The exposed resist was developed in Xylene for 70 sec, followed by a 1 min IPA rinse. To clean any resist residue, the sample was loaded in the Branson barrel etcher, and etched in an Ar/O_2 (120/6 sccm) plasma at 50 W for 20 sec. The patterned sample was then bonded on a 6″ Si carrier wafer using crystal bond, and loaded in the STS-ASE ICP-RIE tool. The CSAR masked polysilicon layer was etched ∼1.4 µm, recessing ∼400 nm into the trench, using to the plasma conditions reported in Table 4.3. However, with this approach, it was later found from tri-gate cross-sectional SEM analysis that the high exposure current used during the e-beam lithography step introduced a significant misalignment due to the coarse e-beam spot size. To obtain a better lithographic alignment tolerance, a small beam size exposure is required, which can be achieved by reducing the exposure current to 30 nA (beam diameter 60 nm). However, the reduction in exposure current requires longer a exposure time, thus affecting the lithographic throughput. Therefore a dual lithography process was introduced, using e-beam for the finer resolution features and tight alignment control, and optical lithography for coarser features. Taking the bird's beak effect into account, a 0.3 µm or better lithographic tolerance is needed in this step to maintain a 0.5 µm gate source overlap as shown in Fig. 4.49(b). In the fabrication of the 2Q4 tri-gate sample, an e-beam lithography step was first performed in the active regions in a same way as in sample 4Q2, with the exception of using a 30 nA exposure current and a 300 µC/cm^2 dose. The CSAR masked polysilicon was etched in the same manner as sample 4Q2 in the STS-ASE tool for 2 min, but the etch was only performed in the active region. To etch the polysilicon in the field area and PCM, a second etch step was done in the same tool with a photoresist mask. To implement this, the CSAR mask was first stripped in a hot bath of PG remover at 60°C for 6–8 hr. The sample was then solvent cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water. After a dehydration bake at 110°C for 2 min, a 6 µm thick AZ9260 was spun at 4000 rpm for 30 sec and soft baked at 110°C for 3 min. The resist was exposed in a Heidelberg MLA-150 laser writer with a dose of 500 mJ/cm^2. The resist was developed in AZ400K : DI Water

(80 : 300 mL) for ∼4 min. The resist residue was then cleaned in the Branson barrel etcher in an Ar/O_2 (120/6 sccm) plasma at 100 W for 2 min. The sample was then bonded with a 6″ Si carrier wafer using crystal bond and loaded in the STS ASE ICP-RIE tool for the polysilicon etch using the plasma conditions reported in Table 4.3 for 2 min. After the etch, the photoresist was stripped in a hot bath of PG Remover at 60°C for 6–8 hr. If the resist became hardened during the etch, a Branson barrel etching in Ar/O_2 (120/6 sccm) plasma can be performed at 300 W for 3–5 min. The complete process flow for both the single and dual step gate patterning is shown in Fig. 4.51 and Fig. 4.52, respectively. Figure. 4.50 shows the direction where the process flow in Fig. 4.51 and Fig. 4.52 are depicted. As shown in Fig. 4.52(f), in the overlapping area between the photo and e-beam defined regions, the oxide underneath the polysilicon was exposed during the second etch step, which reduced the oxide thickness from ∼46–50 nm to ∼26 nm.

The gate oxide quality and the poly doping process were verified with a MOSCAP measurement in the PCM region, and the subsequent process flow was followed. The final etched polysilicon pattern is shown in Fig. 4.53.

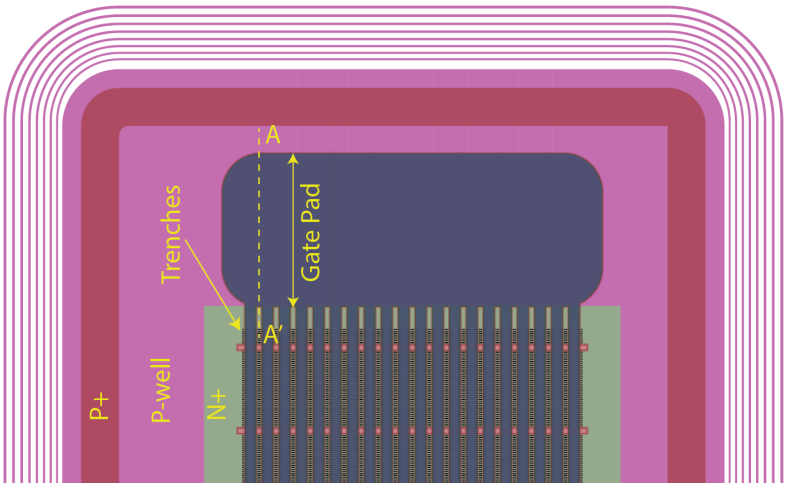
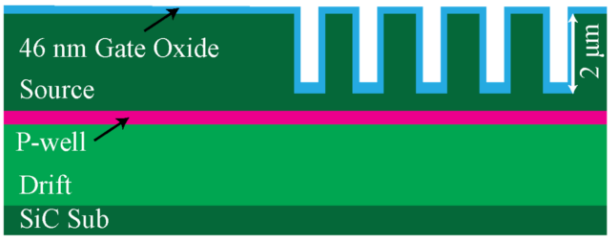
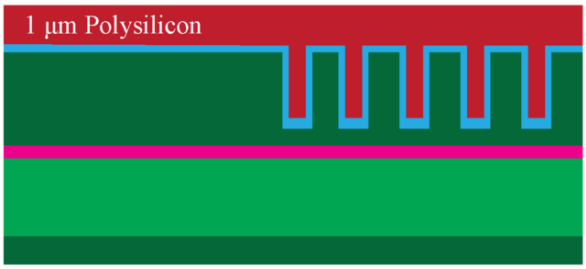


Figure 4.50. The process flows illustrated in Fig. 4.51 and 4.52 are shown along the A-A′ cross section



(a)



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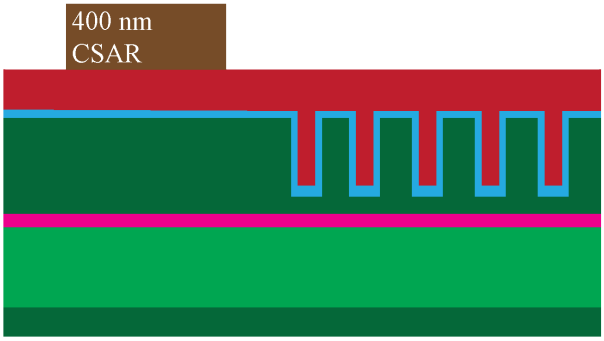

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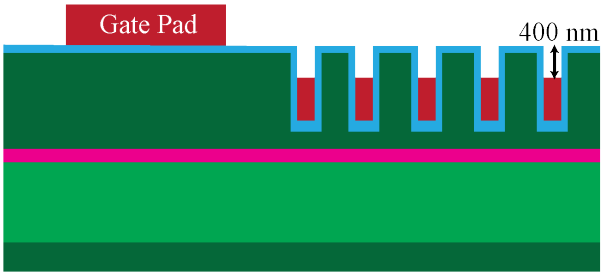


(d)

Figure 4.51. Single step polysilicon gate patterning process flow in the cross section shown in Fig. 4.50 : (a) Trench and gate oxide coated SiC sample; (b) 1 µm polysilicon deposition; (c) High throughput 200 nA e-beam lithography with CSAR resist, and (d) CSAR masked polysilicon etch.

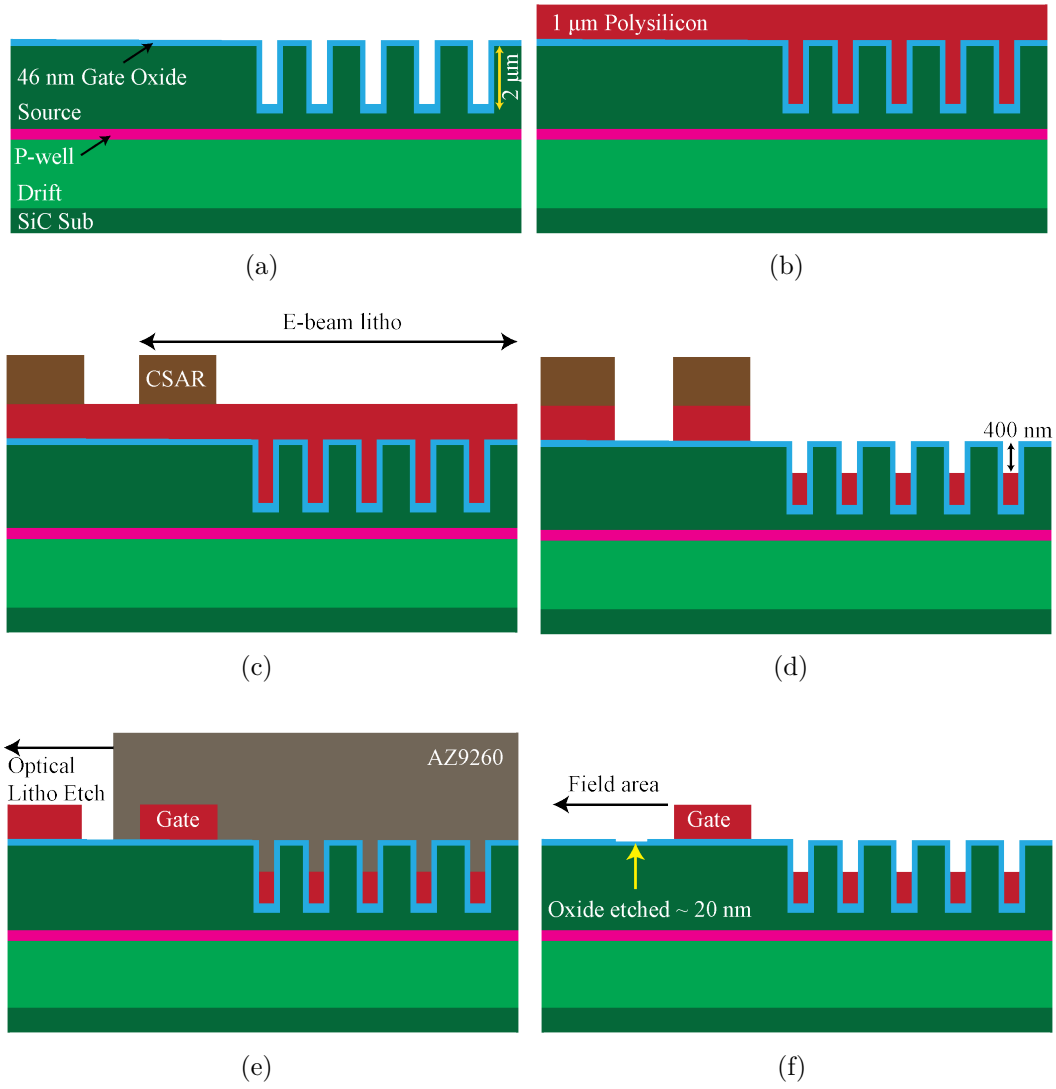


Figure 4.52. Dual step polysilicon gate pattern process flow in the cross section shown in Fig. 4.50: (a) Trench and gate oxide coated SiC sample; (b) 1 µm polysilicon deposition; (c) 30 nA high accuracy e-beam lithography with CSAR resist; (d) CSAR masked polysilicon etch; (e) Optical AZ9260 resist pattern for field area polysilicon etch, and (f) Final polysilicon etch.

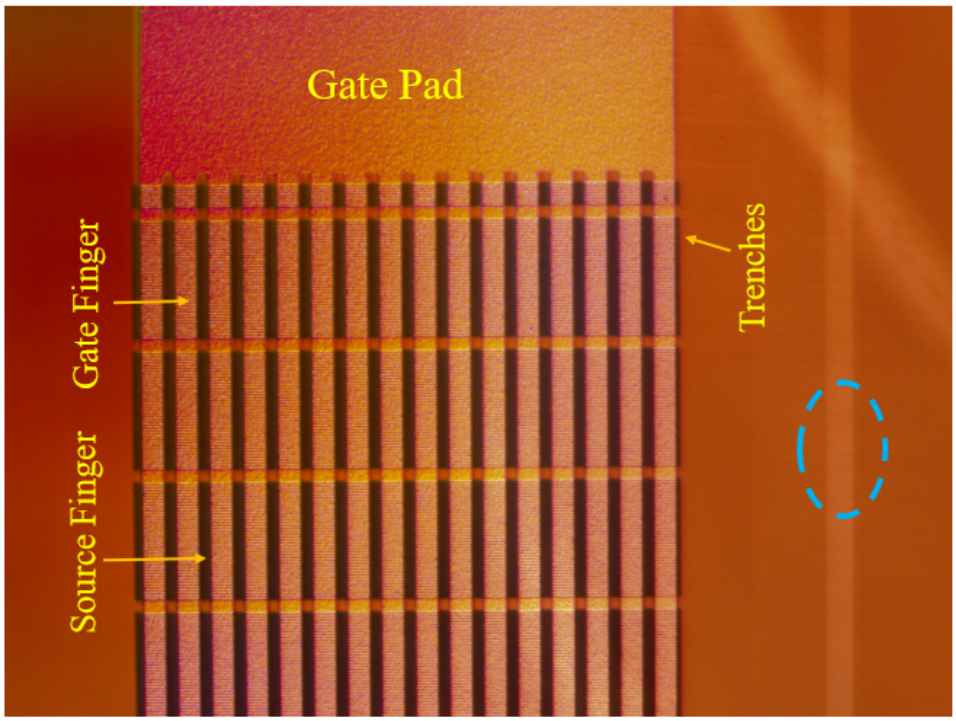
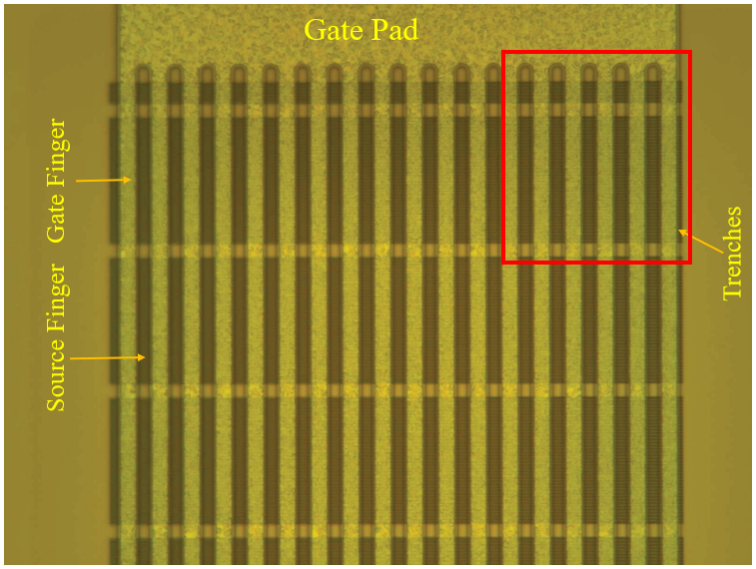


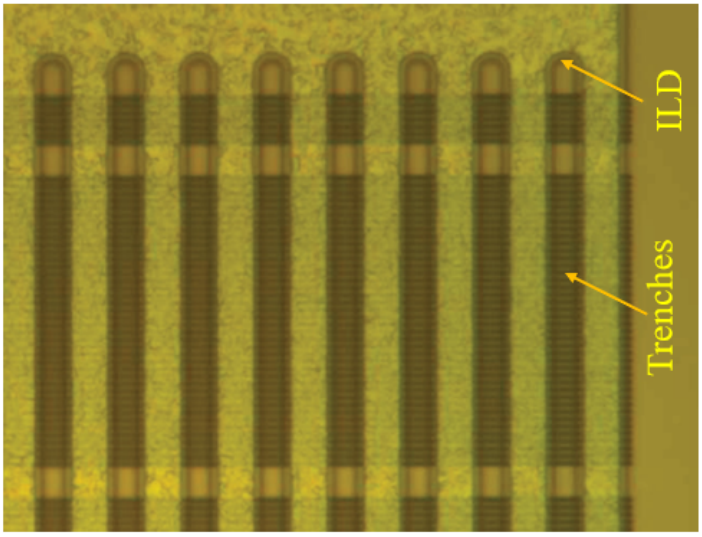
Figure 4.53. Optical image after polysilicon gate patterning. Dashed blue highlighted region is the thinned down oxide region due to overlap between lithography steps.

4.10 Interlayer Dielectric - the Growth

After the gate patterning and process verification, the gate poly was oxidized in a high temperature wet pyrogenic ambient to form a 1 µm thick interlayer dielectric (ILD) layer. The sample was first cleaned in piranha for 10 min, followed by a 5 min water rinse. An extended solvent cleaning — 20 min in toluene, 30 min in acetone, 30 min in methanol, and again 10 min in methanol — was also performed before loading the sample into the furnace. The oxidation rate was calibrated using a Si test sample at a set temperature of 1100°C. The calibrated oxidation conditions were next used to form the ILD layer in the tri-gate sample (2Q4). The oxidation was done in a 3 step process — 10 min dry, 205 min wet, and 10 min dry oxidation to achieve a 0.92 µm thick ILD. An optical microscope image of the tri-gate sample after ILD growth is shown in Fig. 4.54.



(a)



(b)

Figure 4.54. Optical image after 1 µm ILD growth: (a) Overview of a tri-gate device, and (b) Close-up view of the red highlighted region in (a).

4.11 Ohmic Contacts

A self-aligned ohmic Nickel (Ni) silicidation process was used to form the source, base, and the drain contacts. The common metal on the top surface was used for both the source and base contacts. The source and the p-well regions must be connected together to prevent

any parasitic BJT operation. The ohmic metal deposition and annealing process can be divided into five steps: 1) deposition of Ni on the top surface, 2) 750°C ohmic anneal, 3) etching of any unreacted Ni, 4) bask side Ni deposition, and finally 5) 1000°C anneal to from Ni silicide on both front and back surfaces. To start the process, the sample was first cleaned in 3 solvent baths — toluene, acetone, methanol, and DI water for ∼10 min each. After a dehydration bake at 110°C for 2 min, a bilayer resist of 0.4 µm thick LOR3B and 1.8 µm AZ1518 was deposited on the sample in a standard resist spinning system. The LOR3B resist was spun at 2000 rpm for 30 sec and baked at 190°C for 5 min, followed by AZ1518 resist spun at 4000 rpm for 40 sec and baked at 110°C for 2 min. The bi-layer resist was then exposed in the Heidelberg laser writer tool at a dose of 200 mJ/cm^2, and developed in AZ400K : DI water (80 : 300 mL) for ∼30 sec. The resist residue was cleaned in the Branson barrel etcher in a Ar/O_2 plasma at 100 W for 1 min. The ∼46–50 nm thick gate oxide in the patterned window was then etched chemically in BOE for 50 sec. A surface roughening etch was then done in a Jupiter RIE tool with the parameters listed in Table 4.11 for 1 min. The recipe also etches oxide at ∼40 nm/min, which ensures the removal of any oxide remaining after the BOE dip. Any possible C_xF_y polymer formed during the etch process was cleaned in the Branson barrel etcher with the same plasma conditions as the previously described residue cleaning step. In the final cleaning step, the sample was dipped in BOE for 20 sec. The sample was then loaded into an e-beam evaporation chamber where a 200 nm thick Ni was deposited at 1.5 A/sec under a pressure of 1×10^{-6} Torr. The metal was lifted off in a 60°C bath of PG remover for ∼6–8 hr. The sample was then cleaned in toluene, acetone, methanol, and DI water, each for 10 min. It should be noted here that the volume of SiC converted to NiSi during annealing process is proportional to the initial metal thickness in a ratio of more than 1:1. It was observed later during a failure analysis investigation that annealing a 200 nm thick Ni metal consumed about 260 nm of SiC, converting it to NiSi. This material loss is detrimental if the underlying implant regions are not deep enough. Therefore a thinner metal of about 50-100 nm would be more appropriate for ohmic contact process [37].

The two step annealing process was performed in a Jipelec RTA (rapid thermal annealing) tool in an argon inert ambient. The process was first verified with an epi-grown SiC test

sample having a shallow n-type source and p-type well implantation. Before loading the sample, the tool was treated by baking it at 1000°C for 5 min to dehydrate any moisture. Additionally, a multi step Ar pump and purge at 550°C for ∼40 min was done to remove any residual oxygen or moisture [37]. The SiC sample was then loaded upside down on a ∼20–30 nm oxide coated Si sample as shown in Fig. 4.55. The oxide coated Si sample was placed on a 6″ Si carrier wafer with fresh titanium (Ti) pellets each placed on ∼1×1 cm^2 Si pieces. The Ti pellets act as a getter which readily react with oxygen and help prevent any undesirable nickel oxide formation. It is important to place the Ti pellets on the small Si pieces. Without them, a reaction between the Ti pellets and the underlying Si at high temperature creates stress in the 6″ wafer which causes it to break. All of the samples and Ti pellets must be placed clear of the center for proper pyrometric temperature measurement. The pump and purge cycle was then repeated, but now with the sample loaded in the chamber. The sample was annealed at 750°C for 3 min at atmospheric pressure in an Ar inert ambient. Annealing at this temperature forms nickel silicide on the SiC surface, forming the source and base ohmic contacts.

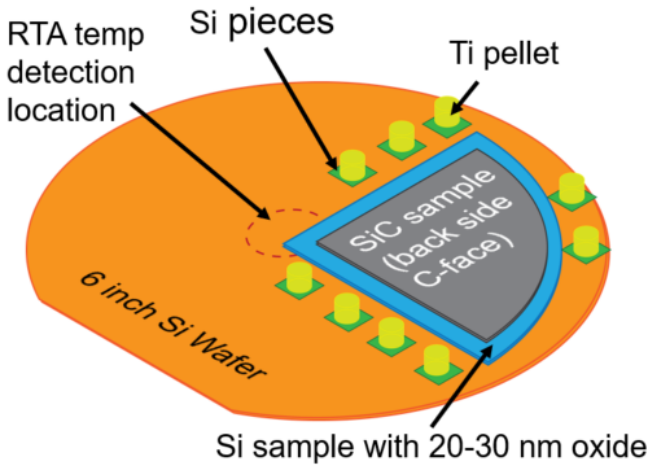


Figure 4.55. Wafer arrangement in the Jipelec RTA tool during ohmic contact anneal.

Any remaining unreacted Ni was etched in piranha (98% H_2SO_4 / 30% H_2O_2) for 5 min. This prevents any metal spiking through the ILD and short circuiting the source and the gate during the 1000°C anneal.

The backside metal was deposited before performing the final 1000°C anneal. To deposit metal on the backside, the front side was protected by 8–10 µm thick AZ9260 photoresist. After the protecting the front surface, the backside of the sample was cleaned in BOE for 5 min. A surface roughening step was performed on the backside in the same manner as on the top using the Jupiter RIE tool. The sample was then etched in a Branson barrel etcher for 2 min in an Ar/O_2 plasma at 100 W, followed by a 20 sec BOE dip before loading the sample into the e-beam metal evaporation chamber to deposit a 200 nm thick Ni layer. The front side photoresist was then stripped off in a hot PG remover bath for ∼2 hr. The sample was then cleaned in the usual series of 3 solvents. The nickel silicidation process consumes SiC ∼290 nm as shown in Fig. 4.49(a).

The backside metal deposition was followed by the high temperature annealing at 1000°C. The chamber treatment and sample loading procedure were same as the first anneal step. The backside Ni and previously formed nickel silicide was annealed at 1000°C for 3 min in an Ar ambient at atmospheric pressure. Finally, the process was concluded with a 5 min piranha etch and standard 3 solvent clean.

In the active region, a self-aligned ohmic process was accomplished using this silicidation process to define the source fingers, which are separated from the gate by an ILD layer. The first lithography step to lift-off and pattern Ni on front surface was not technically needed, provided there is a sufficiently thick field oxide. However, the field oxide was not grown on 2Q4 due to the lack of a proper deposition tool and method, as discussed in detail in Section 4.7. Thus a front surface ohmic metal pattern must be used, since otherwise, during the oxide cleaning step on the source fingers and RIE surface roughening, the thin ∼50 nm oxide in the field area would be removed and the SiC surface exposed, which is unacceptable.

The transmission line measurement (TLM) technique for determining contact resistance was used on the finished tri-gate samples to verify the ohmic anneal process. The measurements on sample 4Q2 are shown in Fig. 4.56, where a contact resistance of a 0.28 Ω and a transfer length of 0.315 µm were extracted, giving a contact resistivity of $1.23 \times 10^{-7}\ \Omega \cdot \mathrm{cm}^2$.

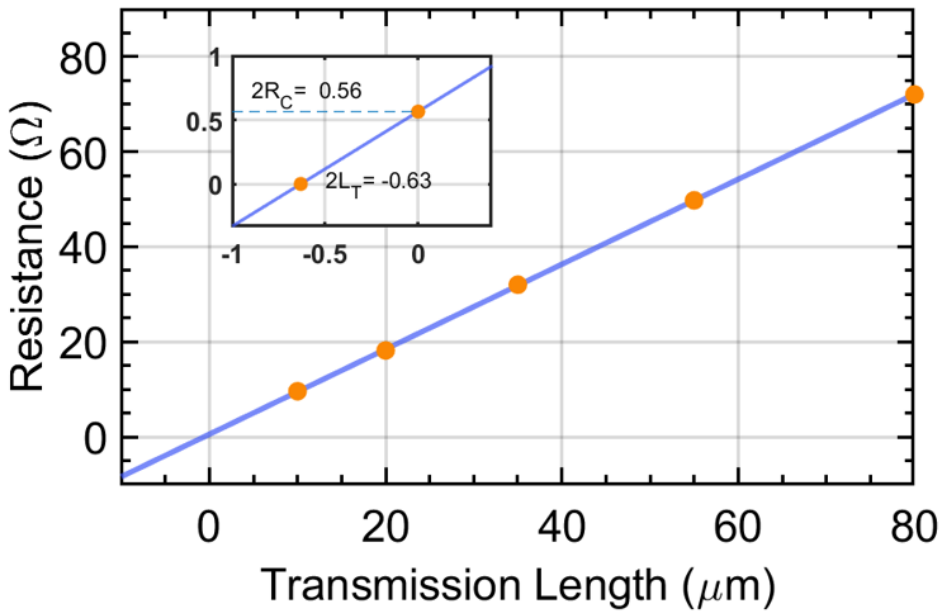


Figure 4.56. N^+ TLM measurement on the 4Q2 sample.

In the second fabrication run (sample 2Q4), a couple of problems occurred involving the ohmic deposition and annealing process due to system malfunctions. During the first run, the metal source in the e-beam evaporator depleted during the deposition, resulting in a poor liftoff. Therefore the deposited metal was stripped off and the deposition was repeated. In the second run, significant contamination and the presence of moisture in the RTA tool due to a bad seal resulted in the formation of NiO on the front surface. The oxidized nickel was stripped in an extended acid bath containing multiple steps of soaking in piranha, aqua regia (HNO_3/HCl 1 : 3), and the SC-2 solution from the RCA clean. In the third run, the ohmic deposition, lift-off, and anneal processes were successful after fixing both the e-beam evaporator and RTA tools. However, in both runs, based on our standard process flow, the sample underwent through total 3 RIE roughening steps, which thinned down the underlying SiC by ∼60–70 nm. This removed most of the highly doped n-type region from the surfac,e which resulted in higher contact resistivity of $1 \times 10^{-5}\ \Omega \cdot \mathrm{cm}^2$. Additionally, the shallow p^+ region also got mostly consumed due multiple RIE roughening steps combined with other material losses during various processes like sacrificial oxidation, etching, etc. This is the main cause of the source to drain shorts on this sample.

4.12 Interlayer dielectric - Patterning and Etching

To establish the gate connection, the ILD layer was patterned and etched in a window inside the large gate pad as shown in Fig. 4.42. Prior to ILD patterning, a surface roughening step in the Jupiter RIE tool was performed using the plasma conditions listed in Table 4.11 for 1 min. This surface roughening step was needed before top metal deposition, but could not be accomplished after ILD window was opened since the etch process consumes Si or polysilicon very aggressively, as shown in Table 4.11. Unlike sample 4Q2, there was no thick field oxide on sample 2Q4, so this surface roughening step was not performed, since the process also etches oxide at a rate of 40 nm/min which would result in a total loss of oxide in the field area.

To pattern the ILD window, an optical lithography using a 6 µm thick AZ9260 photoresist layer was performed with the Heidelberg MLA150 laser writer tool. The AZ9260 resist was spun at 4000 rpm for 30 sec and soft baked at 110°C for 3 min. The resist was then exposed with a dose of 500 mJ/cm^2 and developed in a AZ400K : DI water (80 : 300 mL) solution for ∼4 min. The resist residue was cleaned in the Branson barrel etcher in an Ar/O_2 (120/6 sccm) ambient at 100 W for 2 min. The sample was then bonded to a 6″ JEIDA flat Si wafer with crystal bond and loaded into the E620 Panasonic ICP-RIE tool. A dry plasma etch of the oxide was done according to the parameters listed in Table 4.10.

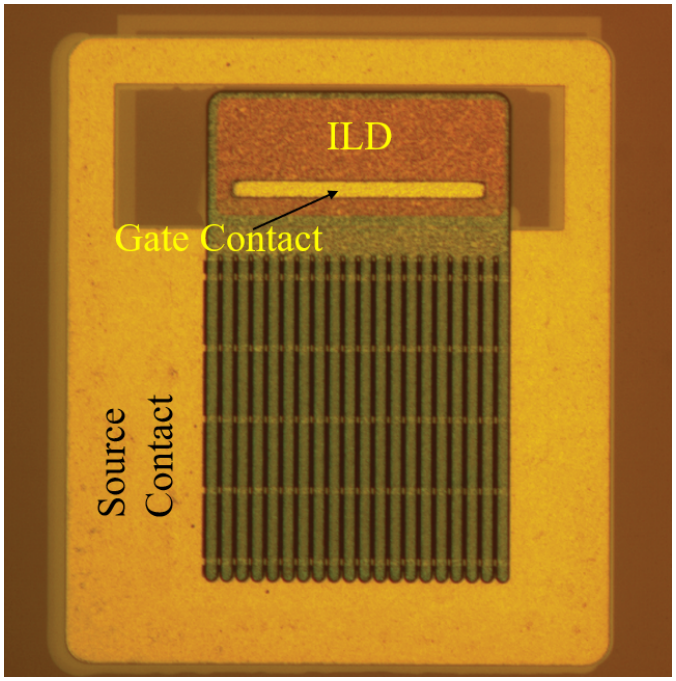


Figure 4.57. Optical microscopy image of the sample after ILD etch.

A wet chemical etch using BOE was not performed due to the resist adhesion and peel off issue that was described in Sec. 4.7. Based on our usual strategy, a dry plasma etch was done in multiple steps of 3 min each. This multiple short duration method is required to ensure complete etch of ILD layer and gate polysilicon exposure determined as by KLA-Tencor P7 profilometer measurements, due to the lack of end point detection in the tool. Since the photoresist etch rate listed in Table 4.10 is less than the oxide etch rate, the etch depth increased with time initially while etching oxide. When all the oxide was etched and polysilicon surface was exposed the etch depth tends to decrease since the etch rate of polysilicon is less than the photoresist. Therefore close monitoring of the etch depth can be used to detect completion of the ILD etch. Additionally, an electrical test should be done after stripping the photoresist to verify the complete removal of the ILD oxide and the exposure of the underlying polysilicon. An optical microscopy image of the sample after the ILD etch is shown in Fig. 4.57.

4.13 Top Metal

The ILD pattern and etch is followed by the final processing step of the fabrication process: the top metal deposition. A bi-layer metal of Ti/Au (25/1200 nm) was sputtered over the entire front surface. In the first run of tri-gate fabrication (sample 4Q2), a bi-layer metal stack of Ti/Au 25/800 nm was deposited in the PVD flexible substrate chamber at a pressure of 5 mTorr. A cross-section image of sample 4Q2 reveals that the thickness of top metal stack was not sufficient to produce a conformal coverage over the topology as shown in Fig. 4.49. Therefore in the second fabrication run, (sample 2Q4), a thicker metal stack of (Ti/Au) (25/1200 nm) was deposited at a pressure of 15 mTorr.

Table 4.12. Top metal deposition condition

Metal	Power (W)	Deposition rate (nm/min)
Ti	150	1.48
Au	75	7.25
	Pressure	5 – 15 mTorr

The top metal deposition conditions are listed in the Table 4.12. An in-situ cool off for 5–10 min is done between the two depositions.

The sputtered metal stack was patterned using a 6 µm thick AZ9260 etch mask. The resist was spun at 4000 rpm for 30 sec, followed by a soft bake of 110°C for 3 min. The resist was exposed in the Heidelberg maskless aligner at a dose of 500 mL/cm^2. It was then developed in DI water and AZ400K (300:80 mL) developer for ∼4 min. The developed pattern was then etched in a commercial Au etchant (GE-8148 from Transene). This chemical is very sensitive to aging, and a relatively new bottle is preferable to obtain a controllable etch rate. The etch rate of Au in this etchant was found to be 7 nm/min at room temperature. The etch process leaves a lot of Au particles on the surface as shown in Fig. 4.58. To prevent the accumulation of these particles, the sample was dipped vertically into the solution using a Teflon basket followed by an extended DI water soak and rinse, although a trace of these particles remained, and was removed after the subsequent Ti etch. The underlying Ti layer was etched in a commercial Ti etchant (TFTN from Transene). The etch was very

sensitive to temperature, and did not etch Ti at or below 70°C but etches very aggressively at higher temperatures. A controllable etch is achieved in a 75–85°C hot bath maintained by a Teflon coated thermocouple submerged in the etchant. This condition etches Ti at a rate of 5–7 nm/min. After the bilayer of metal is etched, the photoresist mask was stripped in a 60°C hot PG remover bath for ∼6–8 hr.

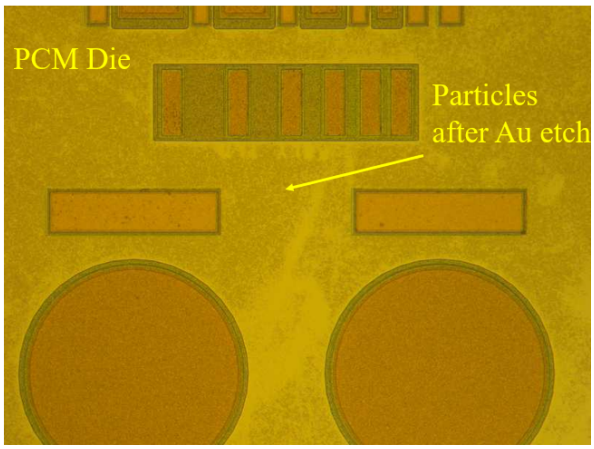


Figure 4.58. Gold particles covering the surface after the Au etch. These are removed during the subsequent Ti etch.

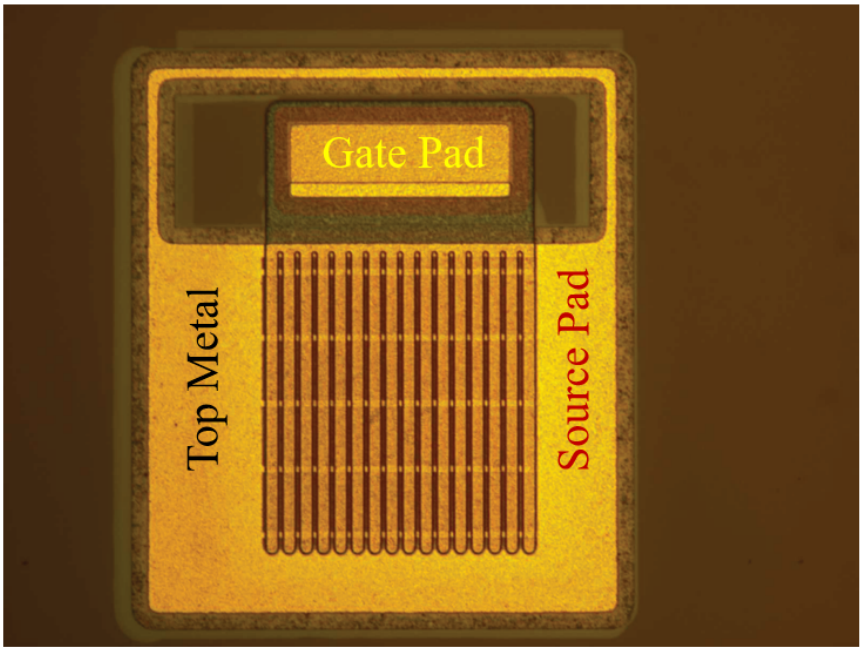


Figure 4.59. Optical microscopy image of the top metal after deposition and patterning.

A bilayer metal stack of Ti/Au (10/100 nm) was also deposited by e-beam evaporation on the backside of the sample. During this process, the front side was protected with a thick AZ9260 layer, and the usual pre-ohmic treatment was performed on the back surface: a 3 min BOE etch, surface roughening as described in Table 4.11 for 2 min, a 1 min 100 W Branson etch, and a final 20 sec BOE dip. The front side photoresist was then stripped in 60°C PG remover for ∼1–2 hr, and a final solvent cleaning was done in toluene, acetone, methanol, and DI water. An optical microscopy image of a completed device is shown in Fig. 4.59.

This concludes the detail process flow that was followed in fabricating Gen-1 tri-gate devices.

5. DEVICE MEASUREMENTS AND PROCESS MODIFICATIONS

This chapter describes the measurement and analysis of fully fabricated tri-gate samples. In the Gen-1 tri-gate, four samples, each quarters of 4″ wafers, were processed in parallel up to the trench etch step. The following steps, including the gate stack, interlayer dielectric, ohmic contacts, and top metal deposition, etc., were done sequentially to check and verify the process one sample at a time. The Gen-1 tri-gate sample information is repeated in Table 5.1 for the reader's convenience, and highlights two samples that were completed and measured electrically. The first sample to finish fabrication was 4Q2, but electrical measurements found that it suffered from high gate leakage, essentially leading to a gate–source short. The process was modified for the next sample (2Q4), but a similar problem was encountered but for a different reason. In this chapter, a detailed investigation of these two failed runs will be presented and necessary process modifications will be suggested.

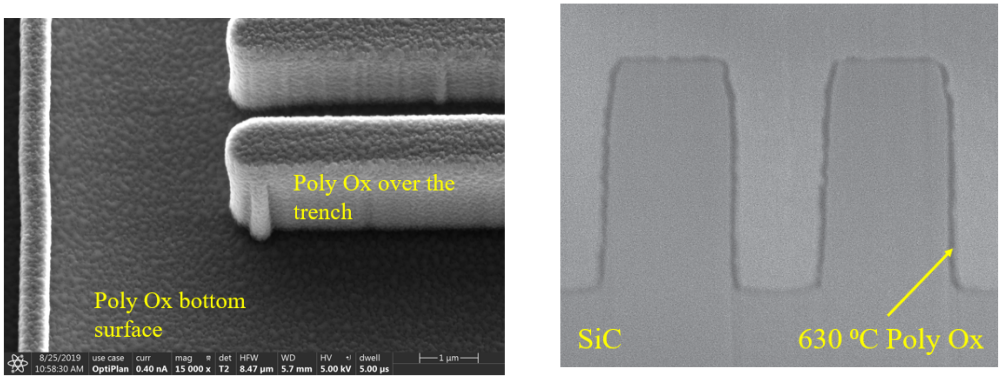
Table 5.1. Gen-1 Tri-gate Samples

Sample name	CSL layer thickness (µm)	Drift layer thickness (µm)
1Q3	3.1	8.3
2Q4†	3.2	5.2
3Q2	2.5	8.5
4Q2†	2.6	5.4

†Measured

5.1 First Completed Run of Tri-gate Devices (Sample 4Q2)

The first completed tri-gate sample was fabricated on a 5.4 µm thick epilayer with a 2.6 µm CSL layer. The 100 mm wafer was diced into 4 equal quarters, and one quarter, konwn as 4Q2, was processed. In this sample, both the tri-gate and planar MOSFETs showed gate-to-source and gate-to-drain shorts. The detailed sample fabrication process flow has already been discussed in the previous chapter. Here, the root cause of the device failures will be investigated, and an improved process will be implemented. The gate oxide of the 4Q2 sample was formed by oxidizing a 26 nm thick LPCVD grown polysilicon deposited



(a) (b)

Figure 5.1. Polysilicon layer deposited at 630°C and oxidized at 1100°C in a wet ambient: (a) Angled SEM image of poly-ox over trenches, and (b) FIB cross-section image of sample 4Q2.

at 630°C. As already discussed in the previous chapter, the polysilicon deposited at this temperature leads to a very rough film composed of large grains, which is amplified after oxidation. As a result, a very rough gate oxide was observed in sample 4Q2, which resulted in some areas lead to very thin oxide or possibly no oxide under the gate in some locations as shown in Fig. 5.1(b). This is one of the root causes of the gate-to-source and gate-to-drain shorts that were observed in sample 4Q2, as shown in Fig. 5.2.

Figures 5.2(a) and (b) show high gate leakage current which passes through to the source and drain terminals. The source terminal is separated from the gate by a self-aligned interlayer dielectric, so another reason for the failure could be the poor definition of the ILD contact window, as the pattern was broadened due to resist adhesion issues during the etch in BOE. To investigate the ILD layer in the Process Control Module (PCM), a test feature with two metal pads isolated by the ILD layer was tested. Normal isolation behavior was found in I-V measurements, as shown in Fig. 5.3. A cross-section SEM image analysis was also done to check the ILD isolation layer as shown in Fig. 5.4. Both analyses suggested that the ILD isolation layer was not the cause of this mode of device failure. Therefore it was concluded that the gate to source short was due to the very rough and leaky gate oxide as shown in Fig. 5.2(a). This process failure also impacted the n-type CSL MOSCAPs, which are top to bottom MOSCAPs separated by the gate oxide. Due to the leaky gate oxide

or possible electrical short, no C-V measurement could be done as shown in Fig. 5.5. An investigation was undertaken to find the root cause of the rough gate oxide and implement an improved process to obtain a smooth and robust gate oxide, and is discussed in the next section. Although it was determined that the poor quality and leaky gate oxide leads to device failure, this was not the only failure mechanism involved in sample 4Q2. Other devices exhibited a substantial amount of current between drain and source without any gate modulation as shown in Fig. 5.2(c). Fig. 5.2(b) also shows a similar phenomenon but on a smaller scale. This failure is appears to be due to a source and drain short in the p^+ stripes in the active area, which was unfortunately not understood until completion of the fabrication of the second tri-gate sample 2Q4. Analysis of this failure mode will be described in more detail in subsequent sections.

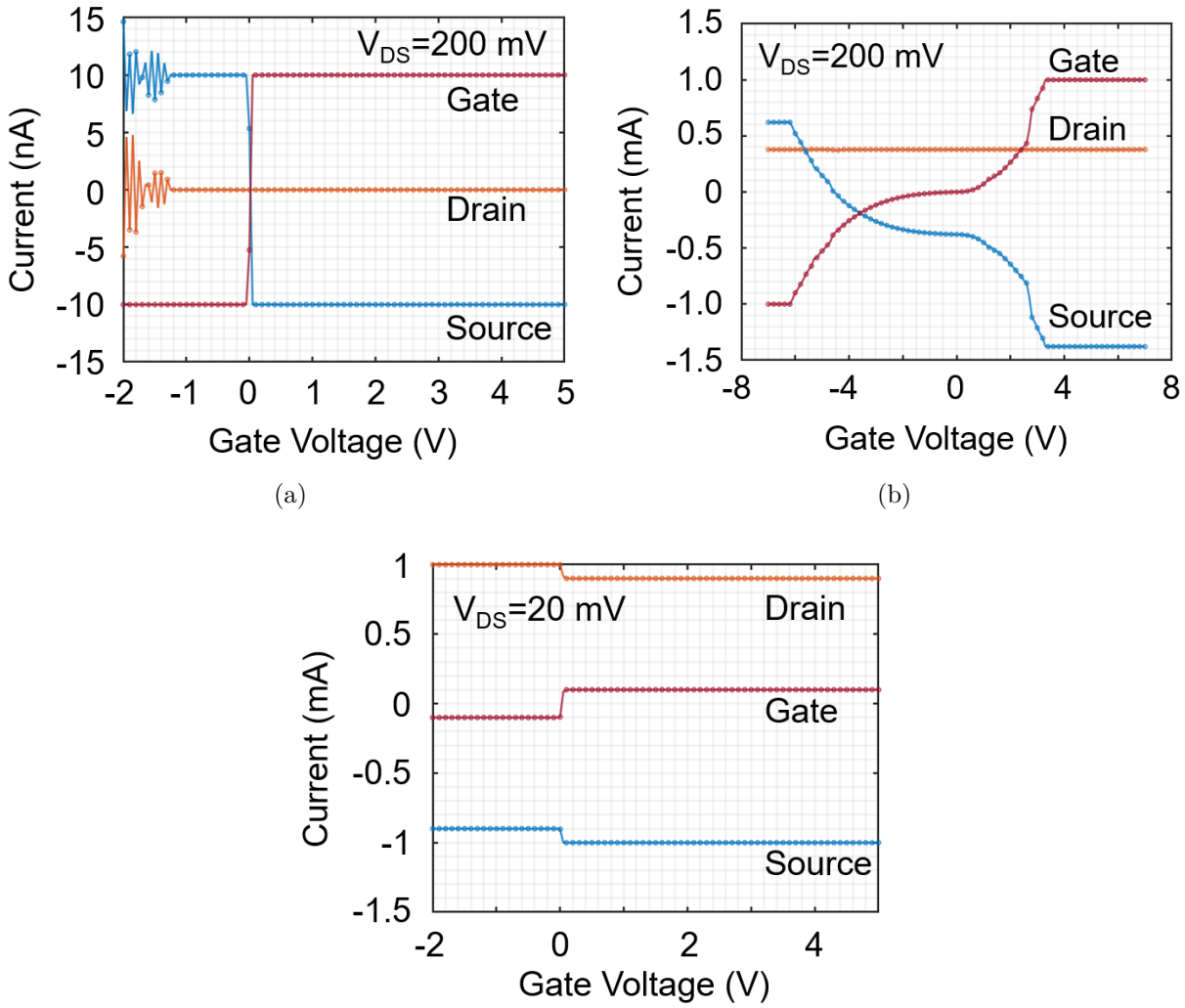


Figure 5.2. I-V characteristics of a tri-gate device on sample 4Q2: (a) a device which shows a gate-source short; (b) a device which shows a combination of gate-source and source-drain short, and (c) the device shows source-drain short.

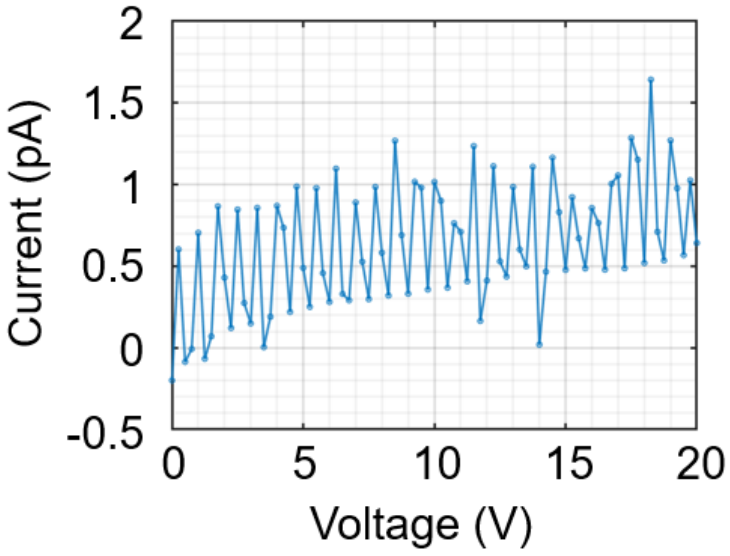


Figure 5.3. ILD breakdown test on sample 4Q2.

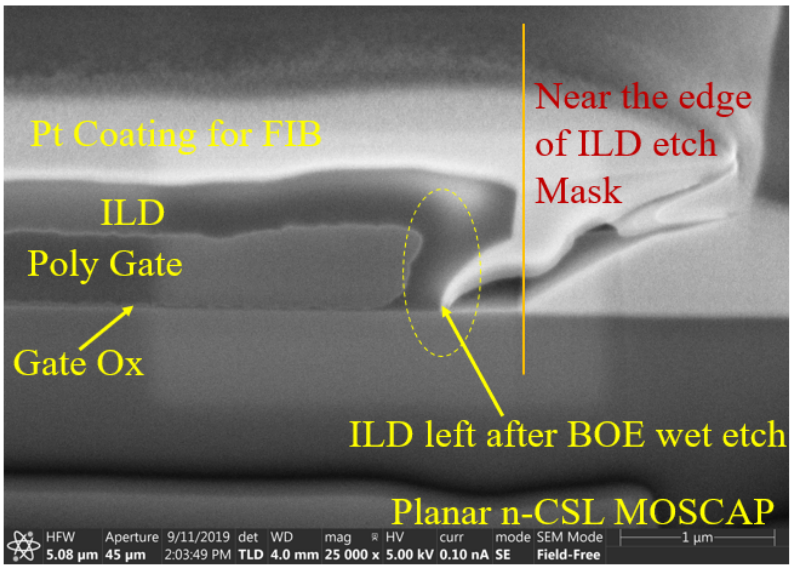


Figure 5.4. FIB image of a planar MOSCAP on sample 4Q2 near the ILD etch window mask. Image was taken to ensure the presence of ILD after bad wet chemical BOE etch

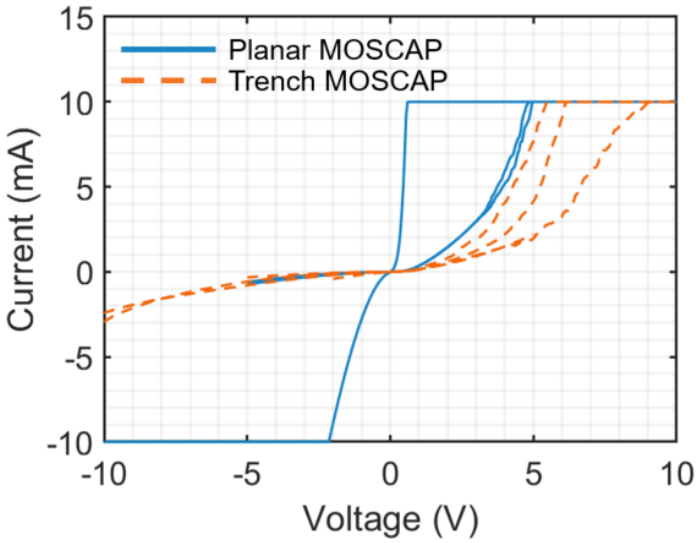


Figure 5.5. MOSCAP leakage on the 4Q2 tri-gate sample.

5.2 Polysilicon Gate Oxide Optimization

A short loop experiment was conducted on both trench and planar SiC MOSCAPs to optimize the polysilicon deposition and oxidation process. The test samples are taken from a quarter of a 4″ SiC wafer with a 5 µm thick 1.5×10^{16} cm^{-3} n-type doped epitaxial layer wafer. A quarter of this wafer was first patterned and etched to create trench fingers similar to those in the tri-gate device. Necessary alignment marks, ILD test devices, and polysilicon TLM features were also included in the mask layout. After the patterned SiC etch, the quarter wafer was diced into a number of 1×1 cm^2 SiC samples to perform a set of experiments on the polysilicon deposition and oxidation process. Polysilicon was first deposited on 3 samples at a different temperatures as shown in the Table 5.2. The deposited polysilicon was then oxidized in ProTemp furnace tube #7 at a setpoint temperature of 1100°C in a wet ambient for 5 min. Based on a standard protocol, the wet oxidation step was always sandwiched between two short dry oxidations at the same temperature for 4 min each. The formation of gate oxide was followed by a 100 nm thick Ni e-beam evaporation and liftoff to define the gate. Gate oxide leakage was then characterized as shown in Fig. 5.6. This device shows signs of early breakdown on samples with polysilicon deposited at 630°C,

consistent with our findings on sample 4Q2. On the other hand, oxide based on polysilicon deposited at a lower temperatures of 605 or 580°C exhibits a higher breakdown voltage. The SEM images in Fig. 4.44 shows that polysilicon films deposited at these temperatures were smooth and conformal, which is necessary for the tri-gate gate oxide process.

Table 5.2. Polysilicon gate oxide optimization sample lot 1

Sample	Poly dep temp (°C)	Poly dep time (min)	Poly growth rate (nm/min)	Oxide thickness (nm)
PU431D8	630	2	7.5	35 nm
PU431D6	605	6	5.8	70 nm
PU431D1	580	10	3.4	68 nm

All samples were oxidized at 1100°C in a wet ambient, using a "4+5+4 min dry+wet+dry" method. A nitric oxide anneal was not done on any of the samples, and nickel was deposited to form the gate

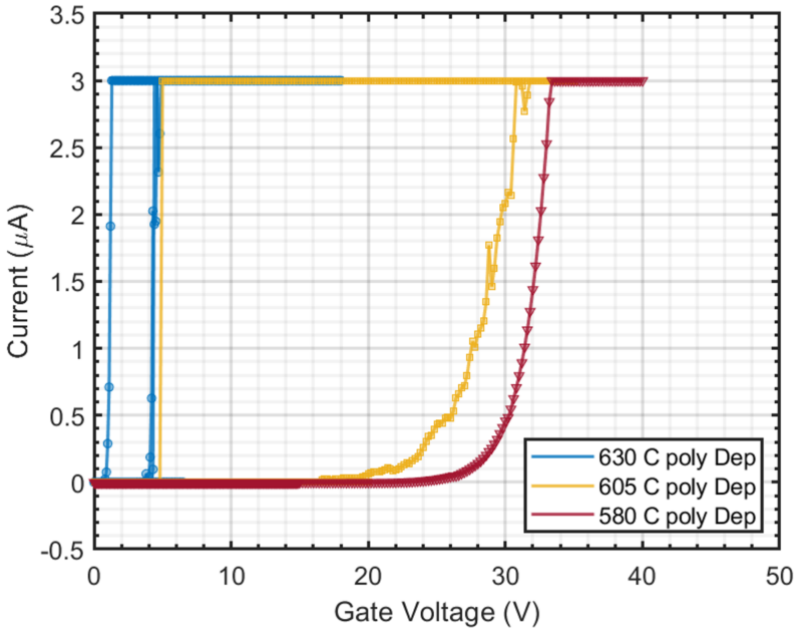


Figure 5.6. Polysilicon gate oxide breakdown measurement of the devices listed in

We therefore next focused on the lower polysilicon deposition temperatures for different oxidation tubes, and added the standard NO anneal with doped polysilicon gates. The DOE process variations and experimental conditions are listed in the Table 5.3.

All samples were prepared using standard solvent and RCA cleans before loading in the LPCVD tube. First, polysilicon was deposited on sample PU431D3 at 580°C for 10 min.

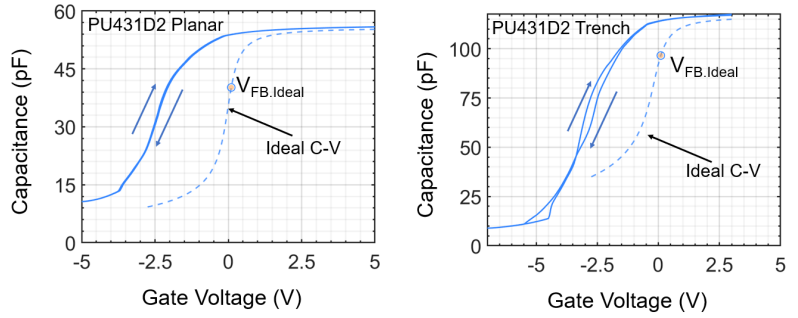
The sample was then oxidized in a wet ambient as in the first experiment to form 76.9 nm oxide. The interface was then treated using the standard NO anneal at 1175°C for 2 hours. Then a 1 µm thick polysilicon was deposited at 630°C and doped in the same manner as described in the previous chapter in Section 4.9. Since dry oxidation was known to produce a good interface with less fixed charge and interface state density in silicon, the technique was also tried here on sample PU431D2 and PU431D7 in two different tubes. Finally, a low temperature polysilicon was deposited at 550°C to explore the effect of temperature on the process. All the samples received a similar NO anneal treatment and a polysilicon gate.

Table 5.3. Polysilicon gate oxide optimization sample lot 2

Sample	Poly deposition	Tube	Oxidation	Oxide thickness (nm)
PU431D2	580°C for 5 min	Tube1	45 min dry	37 nm
PU431D3	580°C for 10 min	Tube7	4+5+4 min dry+wet+dry	76.9 nm
PU431D13	550°C for 10 min	Tube1	45 min dry	31 nm
PU431D7	580°C for 7 min	Tube4	45 min dry	46 nm

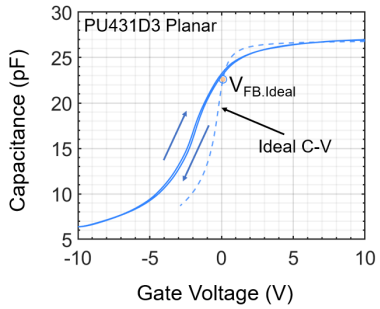
All samples were oxidized at a set point temperature of 1100°C, and NO annealed for 2 hr at 1175°C. n-type polysilicon was used as the gate.

C-V and gate oxide leakage measurements were done on both planar and trench MOSCAPs on all of the samples. The 100 kHz C-V measurements on planar and trench MOSCAPs on these samples are shown in Fig. 5.7. The gate oxide thickness was extracted from the accumulation capacitance and listed in Table 5.4.

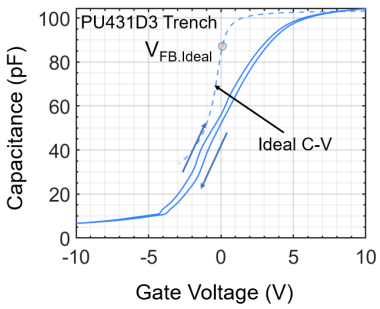


(a) PU431D2 Planar

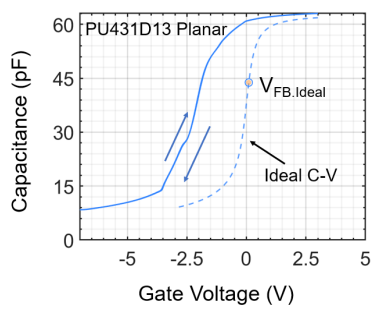
(b) PU431D2 Trench



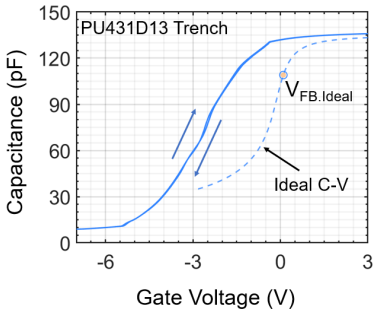
(c) PU431D3 Planar



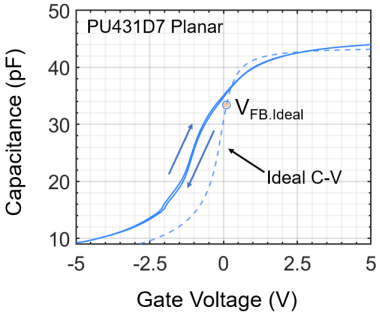
(d) PU431D3 Trench



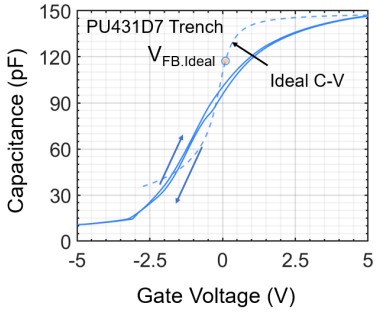
(e) PU431D13 Planar



(f) PU431D13 Trench



(g) PU431D7 Planar



(h) PU431D7 Trench

Figure 5.7. C-V measurements on both planar and trench MOSCAPs from the experiment listed in Table 5.3.

Table 5.4. Effective oxide thickness extracted from the MOSCAP measurments shown in Fig. 5.7

	Planar MOSCAP	Trench MOSCAP
PU431D2	37 nm	65 nm
PU431D3	76.9 nm	77.9 nm
PU431D13	31 nm	60 nm
PU431D7	45.4 nm	54.3 nm

The effective oxide thickness was always higher in trench MOSCAPs compared to its planar counterpart. This suggests that the sidewall oxide thickness was higher than the planar surface. The effect was negligible in case of 1100°C wet oxidation for 5 min in sample PU431D3, but dry oxidation in Tube 1 for 45 min in both samples PU431D2 and PU431D13 showed a significant oxide thickness difference between the sidewall and planar surfaces. To quantify the sidewall oxide thickness, an equivalent capacitance network with sidewall and planar surfaces in parallel can be assumed as shown in Fig. 5.8. The planar oxide thickness can be taken from the planar MOSCAP accumulation measurement. The sidewall oxide thickness can then be extracted from the equivalent capacitance value, provided there is no significant contribution from polysilicon depletion which can be justified from the lack of drooping in the accumulation capacitance.

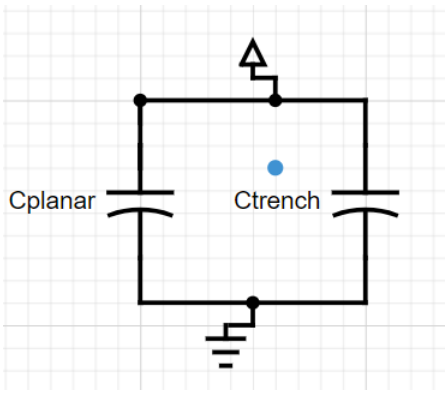


Figure 5.8. Equivalent capacitance network.

$$C_{eq} = C_{planar} + C_{trench} \tag{5.1}$$

$$C_{eq} = \frac{\epsilon_{ox}}{t_{ox.eff}} \times (A_{planar} + A_{trench}) \tag{5.2}$$

$$C_{planar} = \frac{\epsilon_{ox}}{t_{ox.planar}} \times A_{planar} \tag{5.3}$$

$$C_{trench} = \frac{\epsilon_{ox}}{t_{ox.trench}} \times A_{trench} \tag{5.4}$$

$$A_{planar} = 6 \times 10^{-4}\, cm^2 \tag{5.5}$$

$$A_{trench} = 17.4 \times 10^{-4}\, cm^2 \tag{5.6}$$

The extracted sidewall oxide thickness on samples PU431D2 and PU431D13 is about 2.8 times more than was found on the planar surface. This suggests that during the oxidation process a significant amount of SiC was also oxidized, which only can occur if the oxidation temperature was 100–150 higher than the setpoint temperature. At 1200–1250°C, dry oxidation normally produces 8–10 nm of oxide on a Si-face 4H-SiC surface, but results in 5–6 times more oxide on an a- or m-face sidewall, due to the anisotropic nature of the material [46]. This is consistent with the oxide thickness measured on a control (100) Si sample that was loaded with the SiC samples, which suggested a tube temperature of nearly 1200. A similar oxidized polysilicon technique was followed on sample PU431D7, but in different tube (4). A similar effect was observed, but with a less dramatic difference in oxide thickness on the different surfaces. However, the latter experiment confirmed that a 45 min dry oxidation at 1100°C does fully oxidize the polysilicon layer, since a much thicker oxide was observed on the Si control sample.

Oxide breakdown measurements were done on all of the samples, with the results shown in Fig. 5.9. A significant improvement was obtained compared with polysilicon deposited at 630°C, but the breakdown field and leakage are still not comparable to standard thermal oxide on SiC (∼8–9 MV/cm). Later, the author's colleague Dr. Ramamurthy developed a significantly improved polysilicon oxidation process [37], which was then used successfully on subsequent samples.

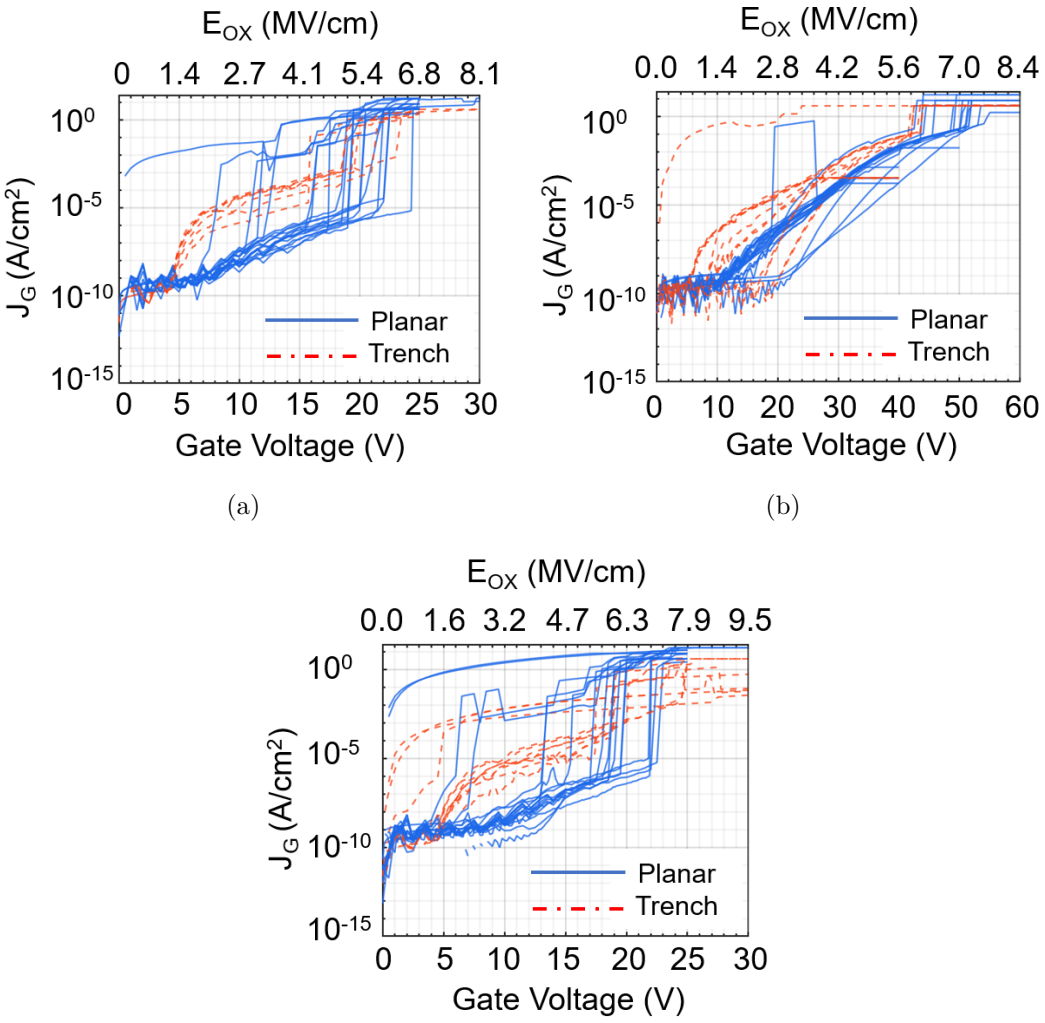


Figure 5.9. Gate oxide leakage measurements on fabricated MOSCAPs: (a) PU431D2 sample (Tube#1: 45 min dry ox); (b) PU431D3 (Tube#7: 5 min wet ox), and (c) PU431D13 (Tube#1: 45 min dry ox).

The data shows that the wet oxidation method exhibits higher leakage current, but with a tighter distribution. On the other hand, the dry oxidation method shows more variability, but generally lower leakage current. In both cases, the majority of the samples broke down at around 5.5 MV/cm. Since in the on-state the device operates at about near 4 MV/cm, the achieved oxide leakage characteristics are acceptable for an initial demonstration of the tri-gate device, but require significant improvement before becoming commercially viable.

A reasonably well-behaved C-V curve was found in samples PU431D3 and PU431D7. The planar MOSCAP C-V on these samples is similar to the calculated ideal C-V curve as shown in Fig. 5.7(c) and (g). The trench MOSCAP flat band voltages in Fig. 5.7(d) and (h) are slightly right-shifted on both cases, which imply different interface state densities on the sidewall and planar surfaces. On the other hand, on samples PU431D2 and PU431D13 as shown in Fig. 5.7(b) and (f), the C-V is distorted, which may be explained by the combination of different oxide and interface trap capacitances on different surfaces of the structure. Furthermore, the flat band voltages on different capacitance components could be different due to oxide fixed charge, interface trap density, etc. which introduces hump or kink when superimposed in C-V measurement The flat band voltage is ∼3 V left shifted from the ideal flat band voltage. This does not necessarily mean the interface quality is poor, as the shift would be expected with a net positive fixed oxide charge, but comparatively fewer acceptor-like interface states. On the other hand, a very high density of acceptor-like interface charges can cancel out the effects of positive fixed charge in the oxide to show a more well-behaved C-V curve as shown in PU431D3 and PU431D7. Nevertheless, the dry oxidation technique using Tube #4, as was used on sample PU431D7, was chosen for the next fabrication run of tri-gate devices.

5.3 Polysilicon Implant Mask Modification

The p-well implantation is defined by a 6 µm thick patterned polysilicon implant mask. To establish a good p-well contact, stripes of polysilicon posts were added to the p-well mask in the source fingers to permit a heavily doped p+ implantation to contact the base implant, as described in Section 4.5. The polysilicon posts and adjacent fingers merge during the oxidation step of the self-aligned source implant process, thus preventing n-type source implantation in these regions. However, the high aspect ratio polysilicon posts are mechanically fragile and prone to breaking off during the post implant cleaning and oxidation process as shown in Fig. 5.10. As a result, in the regions with missing posts, a heavily doped n-type source implant is performed, which cannot be compensated by the subsequent p+ implant. This creates a parallel direct path between the top source contact and the backside drain contact through the CSL and drift layers as shown by "Short Circuit Path (SCP)-1" in

Fig. 5.11 . This polysilicon post technique has been adopted in all of the tri-gate Gen-1 and Gen-2 samples, but in particular, 4Q2 suffered significatnly from extremely low yield due to polysilicon post damage. The mask layout clearly needs to be changed to implement a more reliable p-well implant and contact formation process. One alternative approach would be to opening the entire stripe for a p-well implant, and block the area with a separate electroplated Ni mask during source implantation as shown in Fig. 5.12. This would also increase the p-well contact area and provide improved transient reliability.

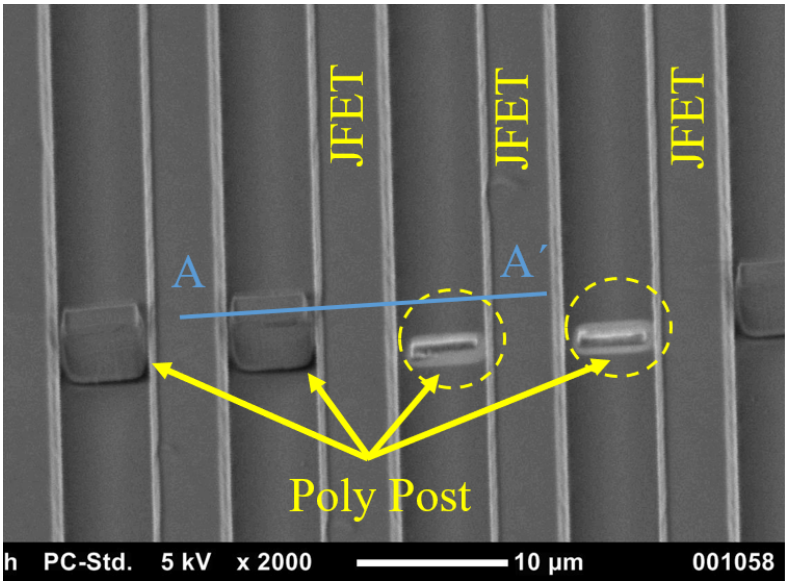


Figure 5.10. Polysilicon post breakage before n-source implantation on sample 4Q2.

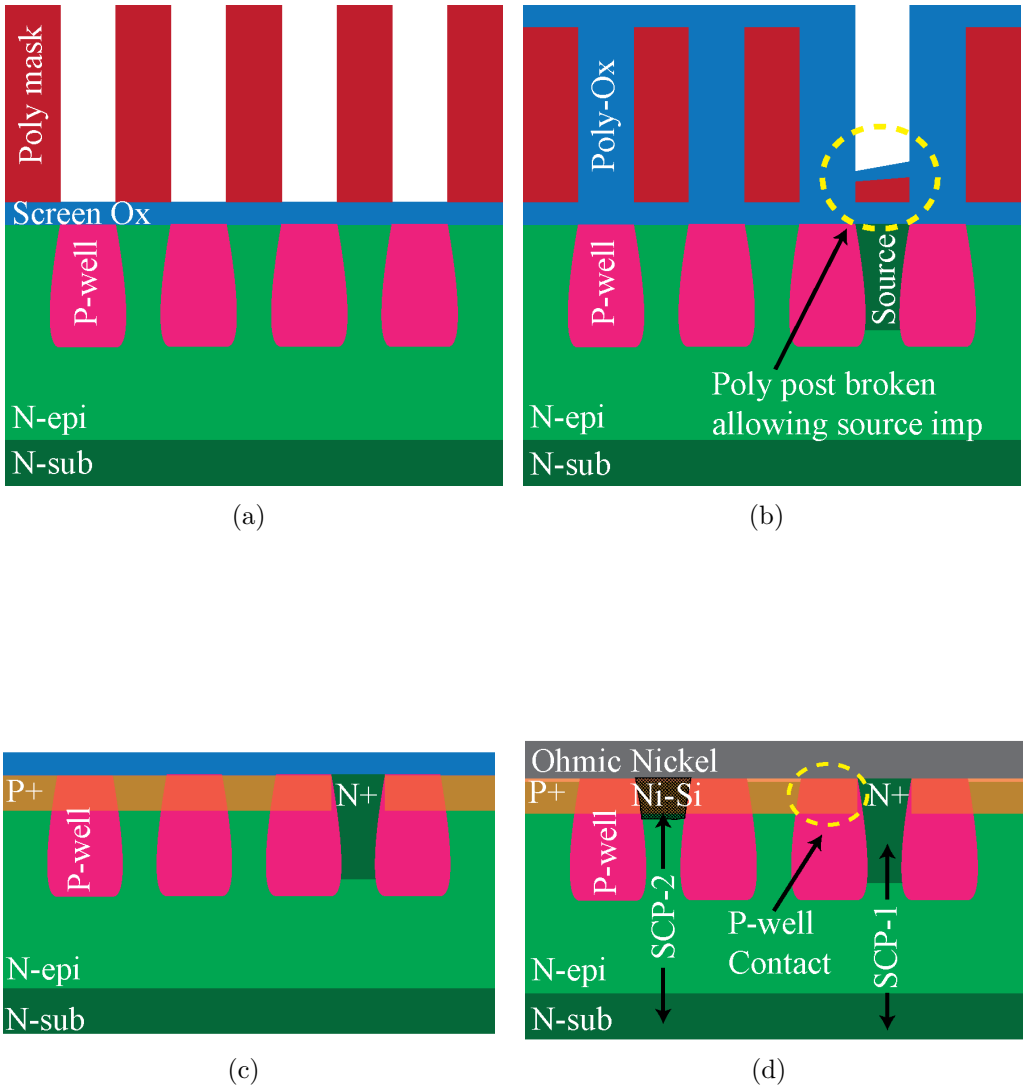
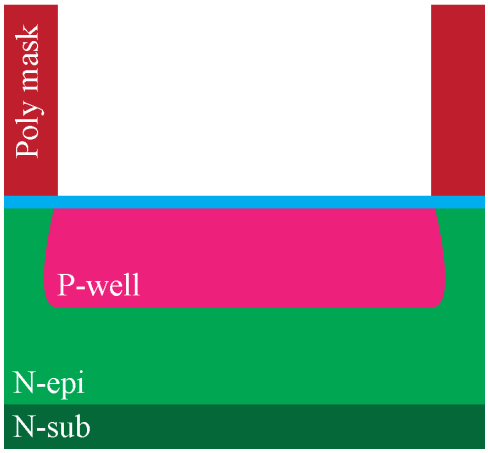
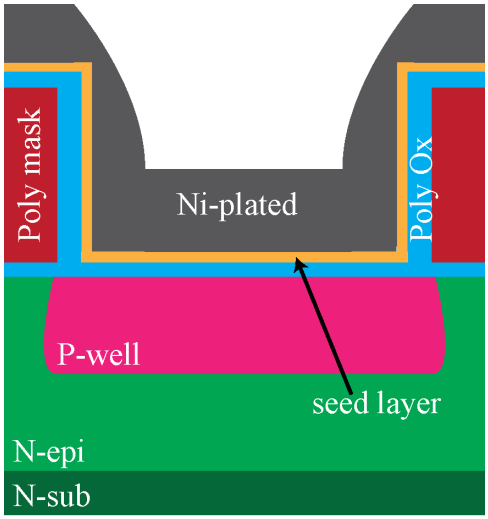


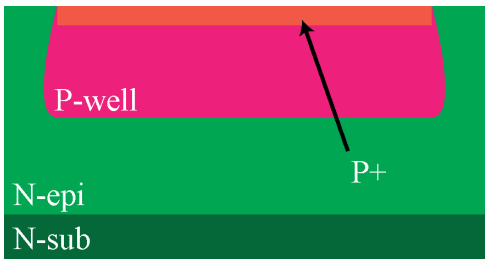
Figure 5.11. Process flow showing effect of damaged polysilicon posts using the same cross-section as shown in Fig. 5.10: (a) Polysilicon mask and p-well implantation; (b) Polysilicon post damage which allows unintentional n-source implantation; (c) P^+ implantation is unable to compensate N^+ source; (d) Two possible short circuit paths. SCP-1: missing post allowing unintentional N^+ source implant, and SCP-2: insufficient P^+ implant depth or excessive Ni thickness during ohmic contact anneal.



(a)



(b)



(c)

Figure 5.12. Suggested alternative implantation process flow to avoid drain-to-source shorts due to damaged p-well implant mask posts: (a) Polysilicon mask and p-well implantation; (b) Electroplated Ni N+ implant block mask in the p+ stripe region, and (c) p+ implantation.

5.4 Second Completed Run of Tri-gate Devices (Sample 2Q4)

After completing the failure analysis of Sample 4Q2, the necessary polysilicon deposition and oxidation process modifications were applied to Sample 2Q4. Unfortunately these new tri-gate devices also exhibited drain-source shorts as shown in Fig. 5.13. However, unlike the previous sample 4Q2, the gate oxide shorts were eliminated, and gate oxide leakage similar to sample PU431D7 was observed. Additionally the MOSCAP C-V curves obtained from 2Q4 also showed normal behavior. Again a step by step investigation was conducted to understand this new device failure mode.

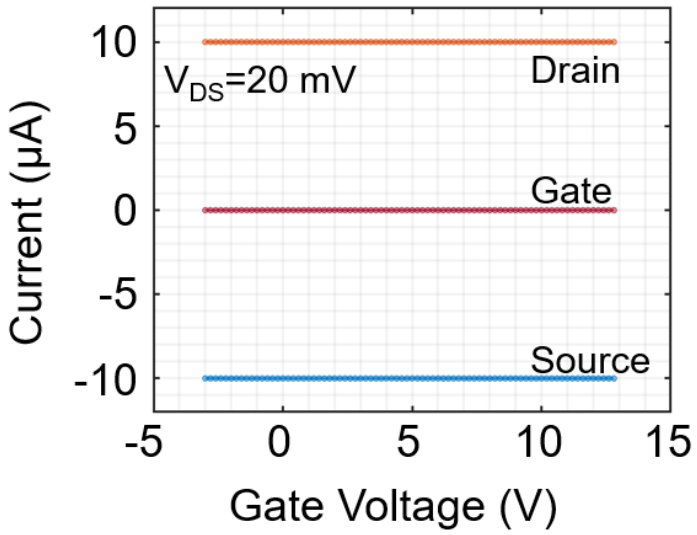


Figure 5.13. Typical IV characteristics from sample 2Q4.

The possible causes of the new drain-source shorts identified in the second fabrication run are as follows: (i) Surface inversion in the field area, possibly due to use of thin gate oxide instead of thick field oxide, (ii) Polysilicon post damage as described earlier, (iii) implantation tilt angle uncertainties, and (iv) Ohmic metal evaporation process repeated (3x) due to equipment failures as described in Section 4.11.

5.4.1 Surface Charge Inversion

The thin field oxide could be prone to field inversion by the random charge generated on the oxide due to moisture or contamination. This could invert the surface of the underlying p-well layer, and create a parallel path from the top surface to the bottom drain without any gate modulation. To investigate this possibility, I-V characteristics were obtained between two pads of adjacent lateral MOSFET devices, two pads of adjacent TLM structures, and one pad of a source TLM to backside drain. These areas are all n-type regions separated by a p-well implant, and thus should be isolated from each other by back-to-back p-n junctions. However, if there is any surface inversion present, then these I-V characteristics should show a linear resistive relationship. The I-V characteristics are shown in Fig. 5.14(c) and (d). In most of the cases the I-V characteristics show a back-to-back p-n diode type behavior as expected. Except for a few failed devices among the TLM structures, most of the measurements show diode like behavior. Therefore surface inversion is not causing the source-drain short failures affecting the tri-gate devices.

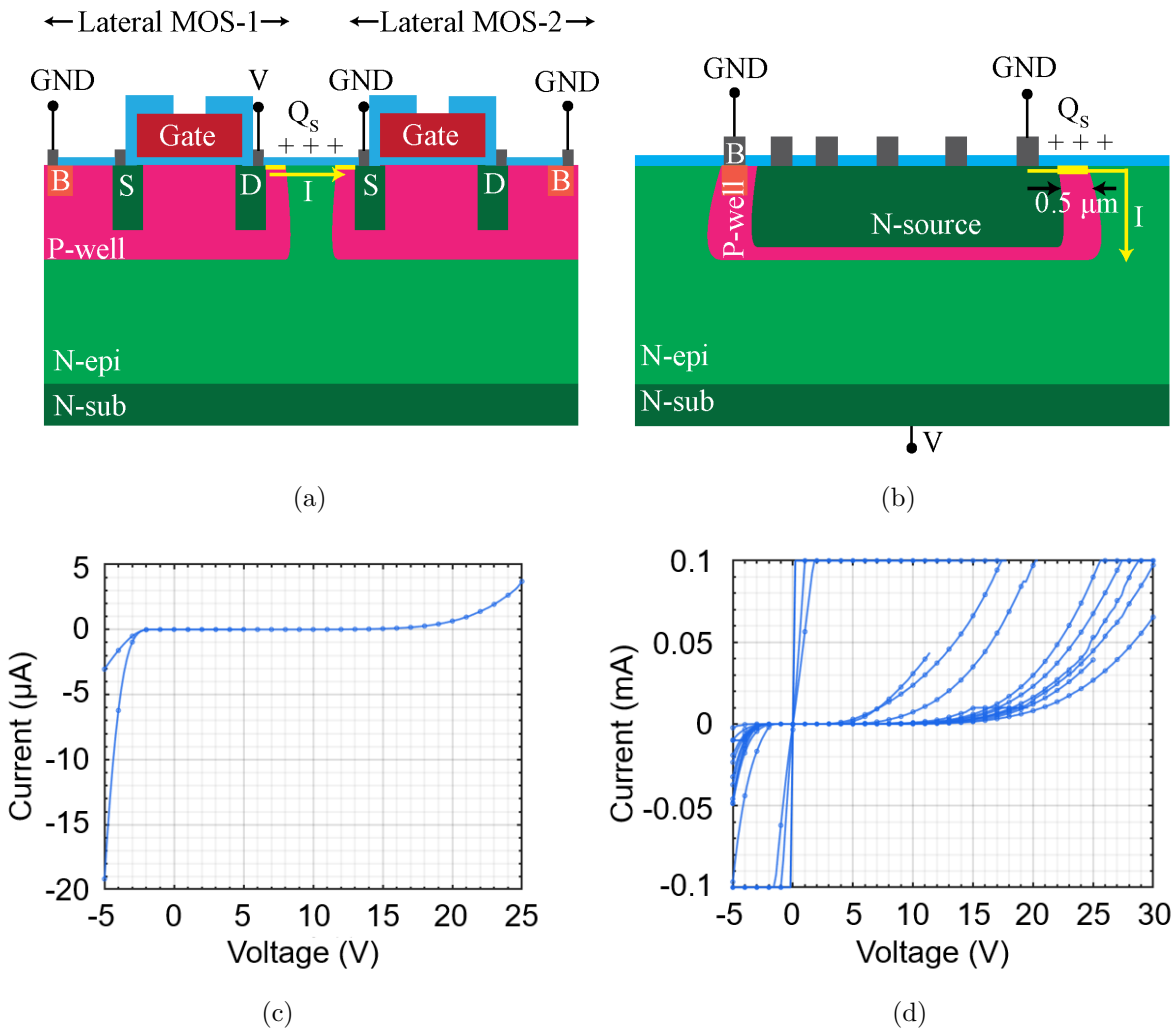


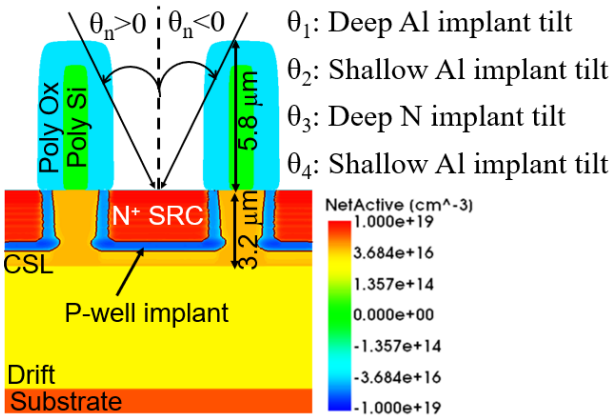
Figure 5.14. Electrical testing for possible field inversion: Test connections and I-V characteristics.: (a) Adjacent lateral MOSFET I-V test; (b) TLM pad to back side drain I-V test; (c) Typical I-V characteristics for (a), and (d) Typical I-V characteristics for (b).

5.4.2 Polysilicon Post Damage

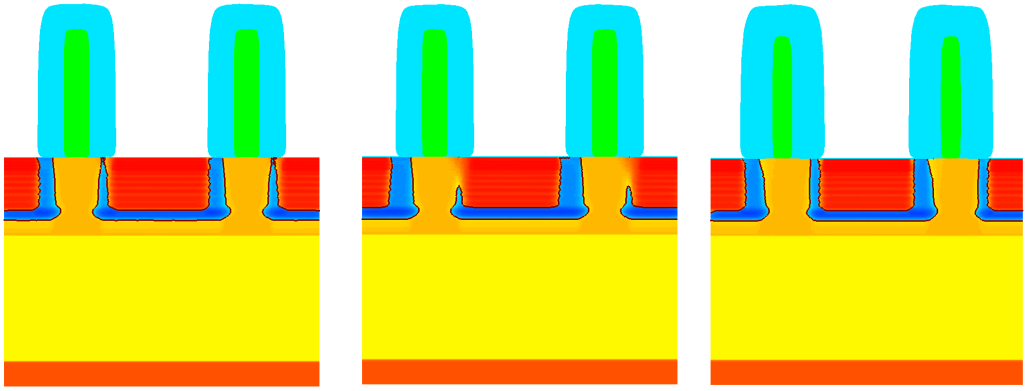
The missing poly posts, as described in Sec. 5.3 could be a potential reason for the device failures, but sample 2Q4 did not suffer from a low yield post damage. It is therefore unlikely that this is the sole cause of the failure of all the tri-gate devices measured.

5.4.3 Implant Tilt Angle Uncertainties

The uncertainties in the implant tilt angle and implant mask shadowing effects may give rise to a junction short between source to drain. As described in Section 4.1, a 5.8 µm thick polysilicon layer was used for a p-well implantation mask, and this polysilicon layer is oxidized by 1 um before implanting the n-type source. Both implants were done in 2 separate steps – (i) high energy, and (ii) low energy. The splits are also done by two different service providers. The implantations were done with 0° tilt angle specification but in practice ±1.5–2° off angle can be considered as the tolerance margin in some specific tool[47]. The samples were not mount in a specific order during different implantation process. Thus the accelerated ions incident on the sample during different runs of implantation were not well controlled especially if the beam raster is done based on magnetic deflection of ions. Therefore it is highly possible the tilt angles at different runs were different with respect to the sample orientation. Furthermore, wafer bowing can introduce addition angles of incident ions on different locations of the sample. It is therefore possible the implanted ions are shadowed by the high aspect ratio polysilicon mask, and that this shadowing is not consistent from one area to another, and from one implant to another. To explore this potential problem, a process simulation in Sentaurus TCAD was performed and cross-section SEM images were taken to visualize the channel region.



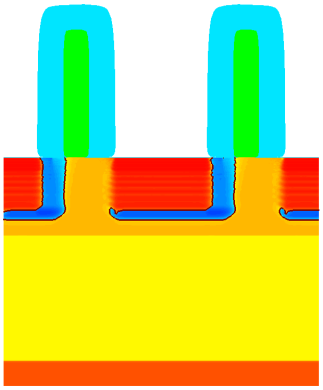
(a) θ_1=θ_2=θ_3=θ_4=0



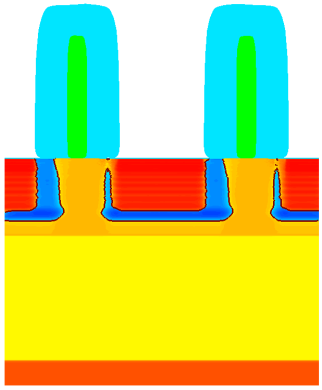
(b) θ_1=θ_2= 0; θ_3=θ_4= -2°

(c) θ_1=θ_2= 0°; θ_3=θ_4= -5°

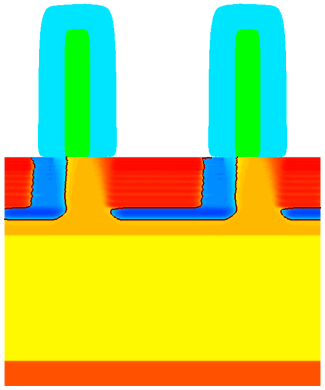
(d) θ_1=θ_2= 2°; θ_3=θ_4= 0



(e) θ_1=θ_2= 5°; θ_3=θ_4= 0°



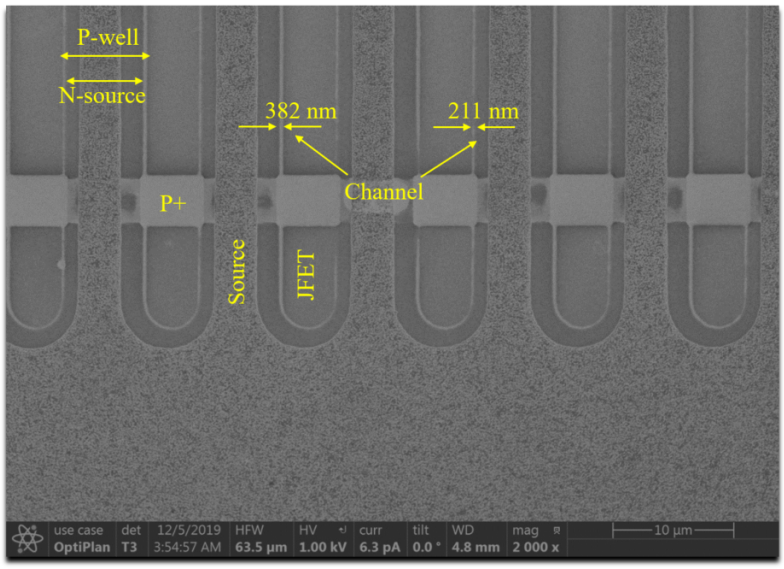
(f) θ_1=θ_2= 2°; θ_3=θ_4= -2°



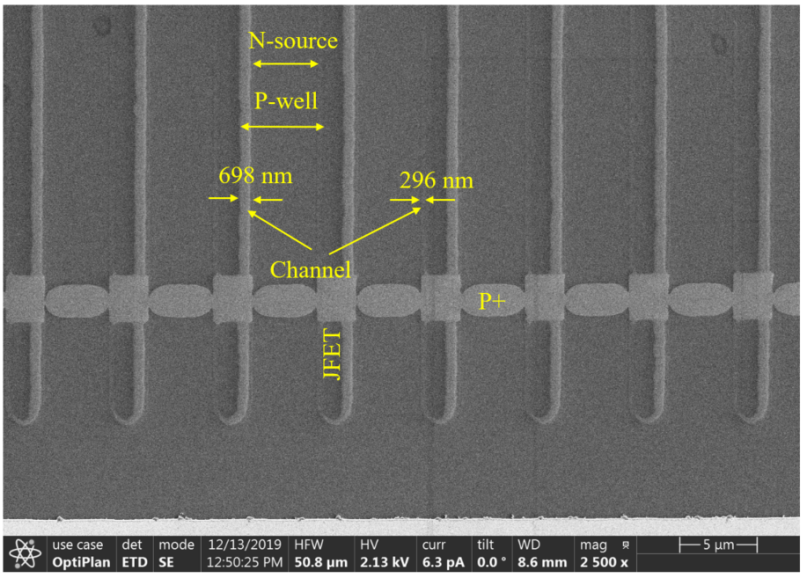
(g) θ_1=θ_2= 5°; θ_3=θ_4= -5°

Figure 5.15. Polysilicon masked implantation Monte-Carlo process simulation with various implant tilt angles where θ_1 and θ_2 are the deep and shallow Al implant tilt angles and θ_1 and θ_2 are the deep and shallow N implant tilt angles

Figure 5.15 shows the results of the process simulation with various combinations of tilt angles in both the aluminum and nitrogen implants. As is clearly evident from the simulations, the implantation tilt angle must not produce a deviation from perfect incidence more than $\pm 2^{\circ}$ for a 6 µm thick mask feature due to severe shadowing effect. If the difference in tilt angle between the Al and N implants exceeds 2°, the channel may not be formed on one side of the device, leading to a drain–source short.



(a)

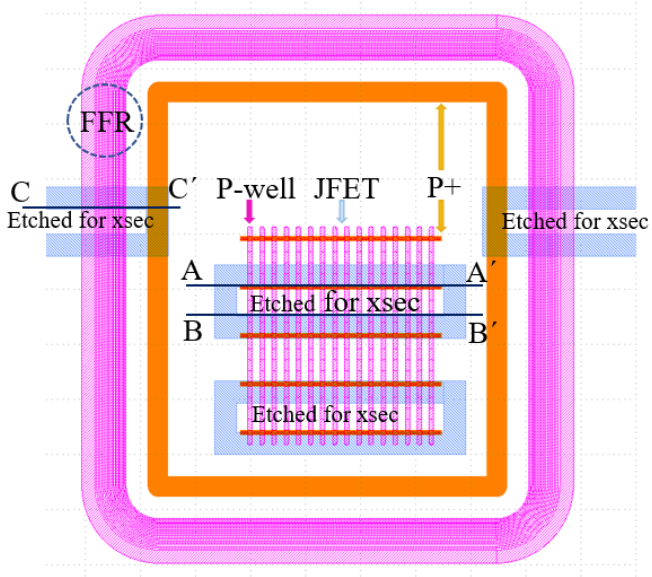


(b)

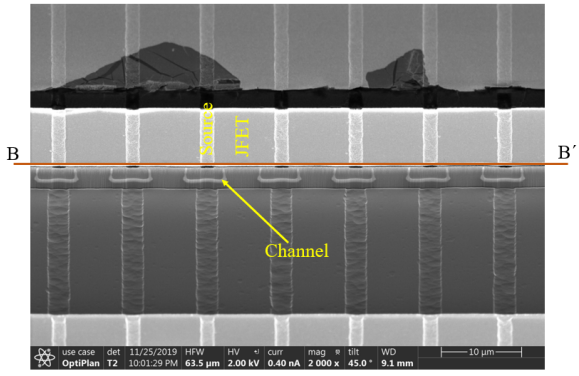
Figure 5.16. Top SEM image of channel after anneal and shallow surface etch using secondary electron potential contrast: (a) Gen-1 4Q2 tri-gate sample; (b) Gen-2 PU391Q1 tri-gate sample.

Figure 5.16 shows a top surface SEM image of two tri-gate devices after implant anneal using secondary electron potential contrast [48]. The technique utilizes the built-in potential of an unbiased p-n junction where electron radiates outward from the quasi p-neeutral regiona and electron move inwards in quasi n-neutral region. The electrons are scattered in a high

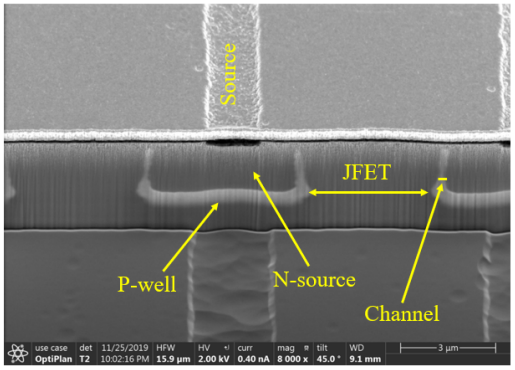
angle from the depleted region which is not detected. As a result, the p-region exhibits brighter image and both n-type area and depleted region shows darker image. Since it utilizes the built-in potential of material a very low energy secondary ion must be used for good imaging. Both figures show a continuous channel on the device, but one side is narrow compared to the other side, similar to the process simulation shown in Fig. 5.15(b) or (d). Figure. 5.17 shows a cross-section SEM image of the sample 4Q2 which shows the channel region on both sides. An attempt to measure the channel length was made with the aid of Matlab image processing tool as shown in Fig. 5.18, which shows the channel region is very thin near the top surface, and appears to be well below the nominal 0.5 micron channel length at all depths. The channel in fact appears to be missing at the top of the surface, but this could be an artifact due to etch residue build-up during the Ni masked SiC RIE etch. This is the first time within the group, we have successfully used the SEPC method in SEM imaging to identify semiconductor junction.



(a)

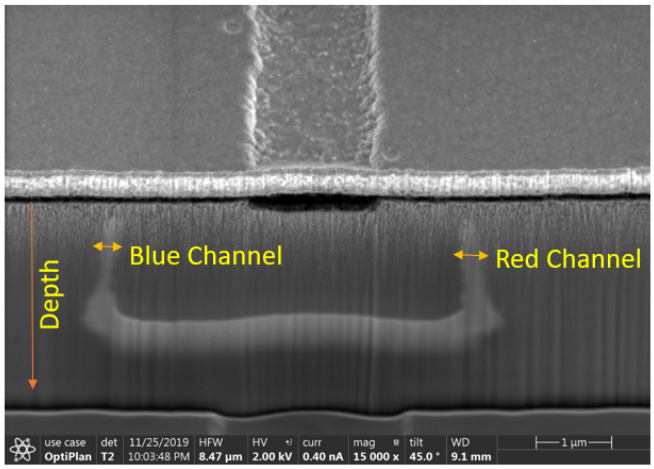


(b)

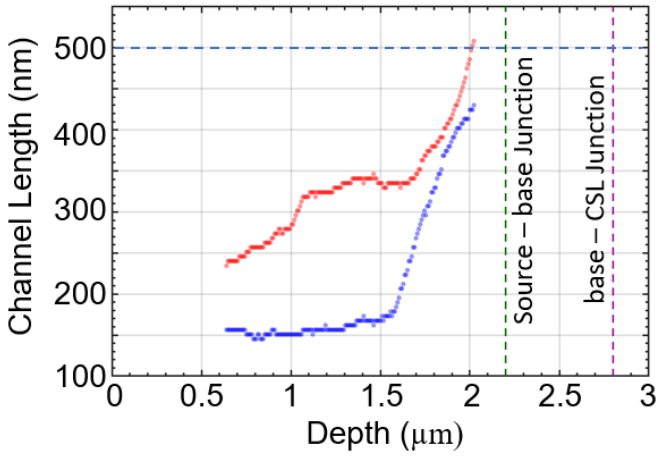


(c)

Figure 5.17. Cross-section SEM images of the channel region in sample 4Q2: (a) Map of fabricated cross-sections; (b) Cross-section along (B-B′) highlighting the channel, and (c) Close-up of one unit cell.



(a)

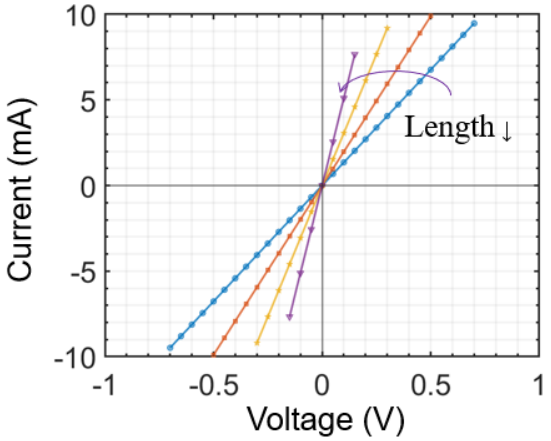


(b)

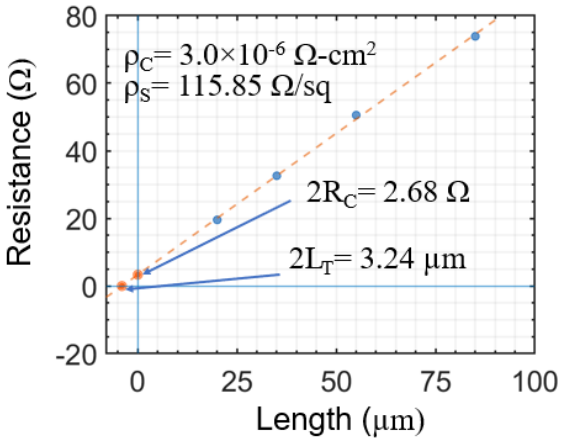
Figure 5.18. Cross-section SEM image of the channel region in sample 4Q2 along B–B′ in 5.17(a) : (a) SEM image, and (b) Channel measurements as a function of depth.

5.4.4 Ohmic Process and Anneal

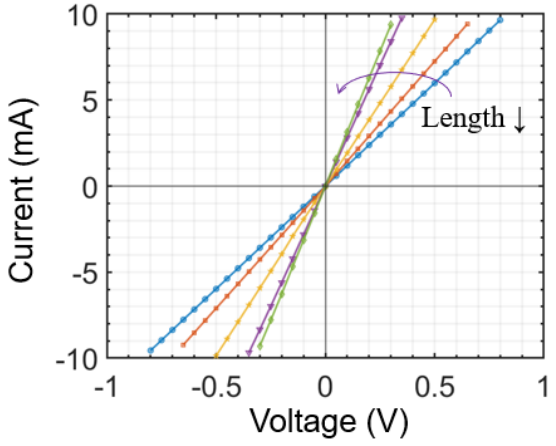
Finally, multiple repetitive ohmic metal depositions and anneals in sample 2Q4 may have also lead to the observed device failures. In the first attempt to deposit the ohimc metal, source exhaustion during Ni evaporation caused a poor quality lift-off. The metal was then stripped, and another metal evaporation was done, but this time the metal was oxidized during the contact anneal. When both tools were fixed, a final run of 200 nm thick Ni was deposited and annealed successfully to form NiSi on the top. However, according to our standard ohmic contact process, an RIE is done to roughen the surface before metal deposition. Repeating this process three times before each metal deposition consumed 25 nm of SiC in each step. During annealing, SiC is consumed in a ratio of 10:13 (Ni thickness : SiC consumed). Since 200 nm thick Ni was used in this run, around 260 nm of SiC was consumed. Additional to this, other previous steps like sacrificial oxidation of SiC during the post trench etch clean, potential SiC oxidation during the repeated effort to oxidize polysilicon to form a field oxide (which was later stripped and not replaced), etc., resulted in in a significant amount of material loss. This is quite evident if the source TLM measurements on samples 4Q2 and 2Q4 are compared as shown in Fig. 5.19. Sample 4Q2, which had gone through just a single ohmic contact process, shows one order magnitude lower contact resistance compared to the sample 2Q4. This is the effect of the exhaustion of top 0.5 µm thick highly doped source region due to material loss.



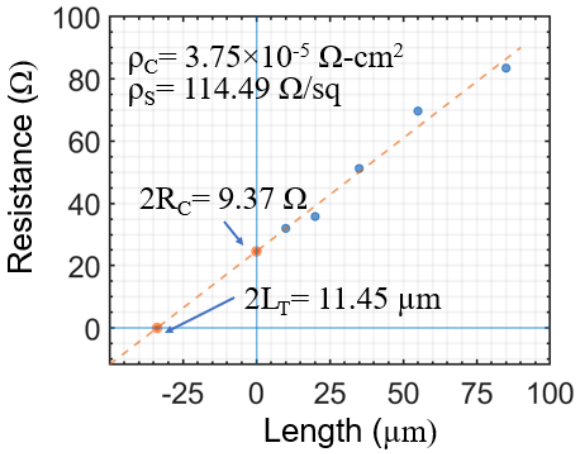
(a) Sample 4Q2 TLM I-V



(b) Sample 4Q2 TLM analysis



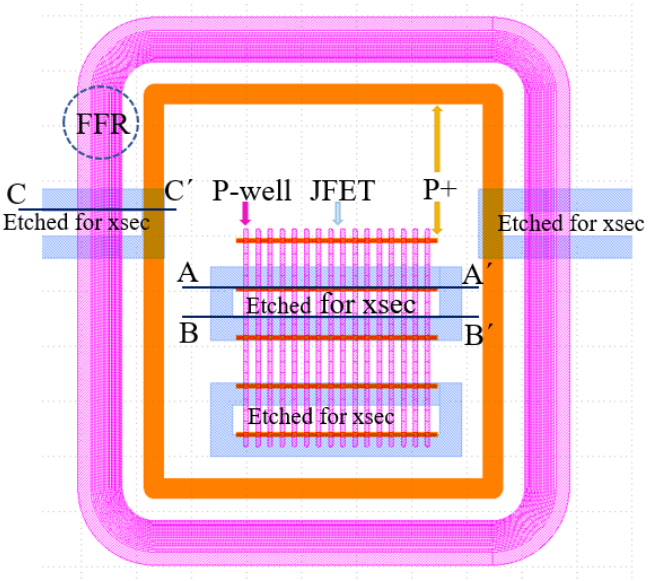
(c) Sample 2Q4 TLM I-V



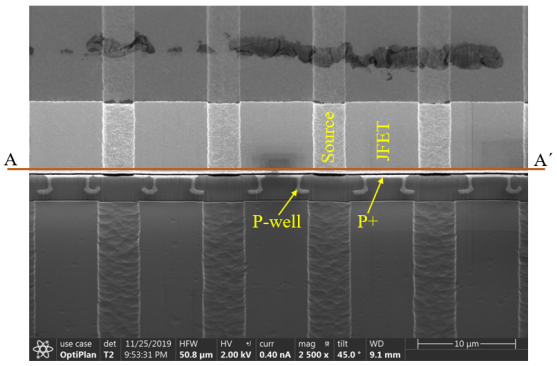
(d) Sample 2Q4 TLM analysis

Figure 5.19. TLM measurements on samples 4Q2 and 2Q4 showing the adverse effect of repetitive ohmic contact processing on contact resistance, likely due to source material loss: (a) TLM I-V measurements on Sample 4Q2 with a single ohmic contact process ; (b) 4Q2 contact resistance analysis; (c) TLM I-V measurements on Sample 2Q4 with 3x repeated ohmic contact process, and (d) 2Q4 contact resistance analysis.

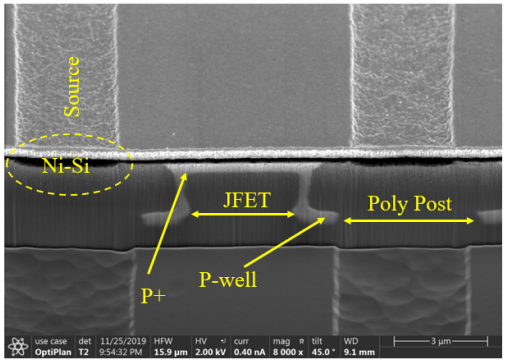
This is potentially the reason that highly doped 0.5 µm deep n-type region near the surface is being depleted due to the material consumption. This has a more dramatic and drastic effect on the highly doped p+ region. In the area under the polysilicon posts in the p+ base contact stripes, the top source contact is only isolated from the drain-connected CSL layer by the thin p+ implant as shown in Fig. 5.11. The p+ implant junction depth is also on the order of 0.5 µm, much of which also got etched during the ohmic process, leaving little to no barrier and a direct electrical short between the top source and bottom drain contacts as depicted as SCP–1 in Fig. 5.11(d). The consumption of material in sample 4Q2, which has gone only a single ohmic process is shown in Fig. 5.20. Figure. 5.17(c) shows an almost completely consumed p+ region underneath the source contact region due to nickel silicide formation. This effect is significantly more severe in sample 2Q4 since it has gone through three repeated ohmic processes including the RIE roughening etch. To verify this electrically, the I-V characteristics of the p+ to n-CSL diode in the PCM region was measured at different locations. The measurement is shown in Fig. 5.21 which clearly indicates the lack of a p–n junction, and instead a direct short between the source and drain contacts. This is likely the dominant failure mechanism in sample 2Q4, since this structure occurs in every active device.



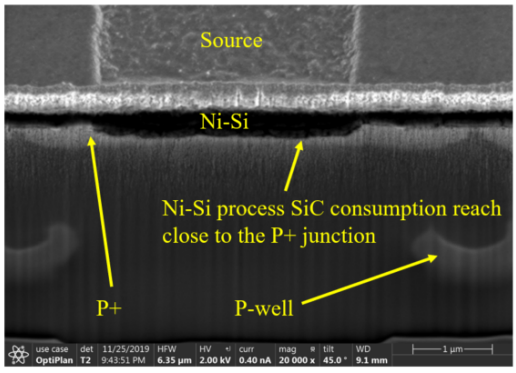
(a)



(b)



(c)



(d)

Figure 5.20. Cross-section SEM image of the P+ contact stripes on sample 4Q2: (a) Map of fabricated cross-sections; (b) Cross-section along the P+ stripe A–A′; (c) Closer view near the JFET region; (d) Closer view near P+ ohmic contact;

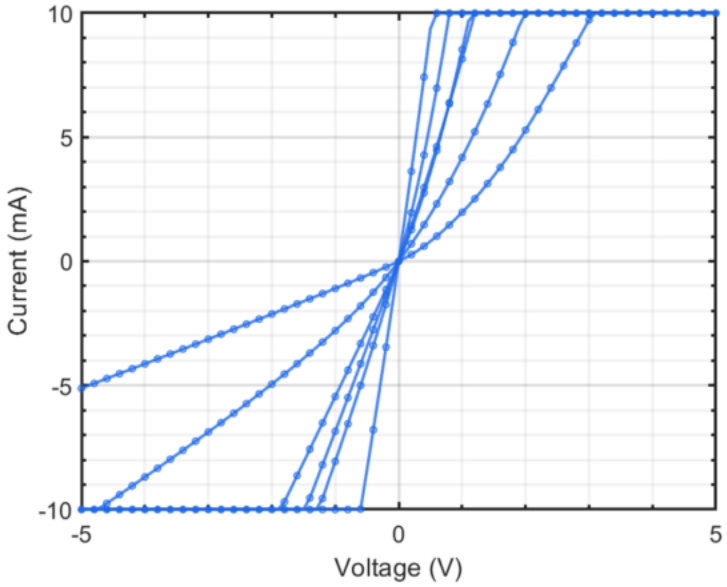


Figure 5.21. I-V characteristics of the P+ to n-CSL diode showing the source of the short circuit path.

To prevent this type of failure, two process modifications could be implemented either individually or in combination. First, a thinner layer of Ni (50-100 nm) could be used, which will consume less SiC during the silicidation process. Secondly, a less aggressive surface roughening step can be followed which would consume only 5 nm of SiC. And finally, if any re-work is required in a future fabrication run, the roughening etch should not be repeated as it was in this case. Any such process modifications would require verifying that the contact resistivity ohmic nature is not negatively impacted.

5.5 Lateral MOSFET Measurement and Mobility Issue

Lateral MOSFETs in the PCM region were characterized, and the output characteristics are shown in Fig. 5.22 for different channel lengths. Similarly, the transfer characteristics are shown in Fig. 5.23 for the same device with different channel lengths and a 20 mV drain bias. From the Id-Vg curve, the drain current much lower than expected, and the turn-on is very gradual.

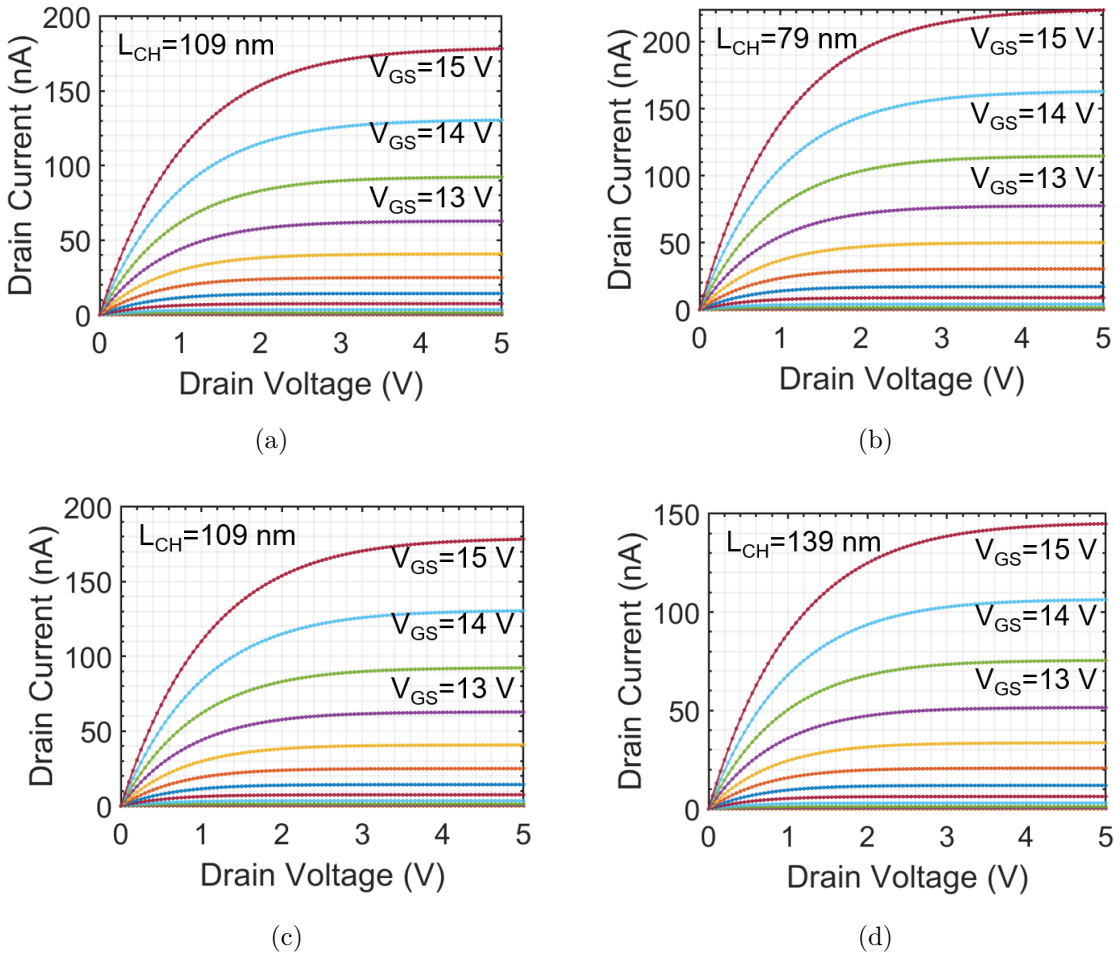


Figure 5.22. Output characteristics of lateral planar MOSFETs in the PCM region of sample 2Q4 for various channel lengths: (a) 49 nm; (b) 79 nm; (c) 109 nm, and (d) 179 nm.

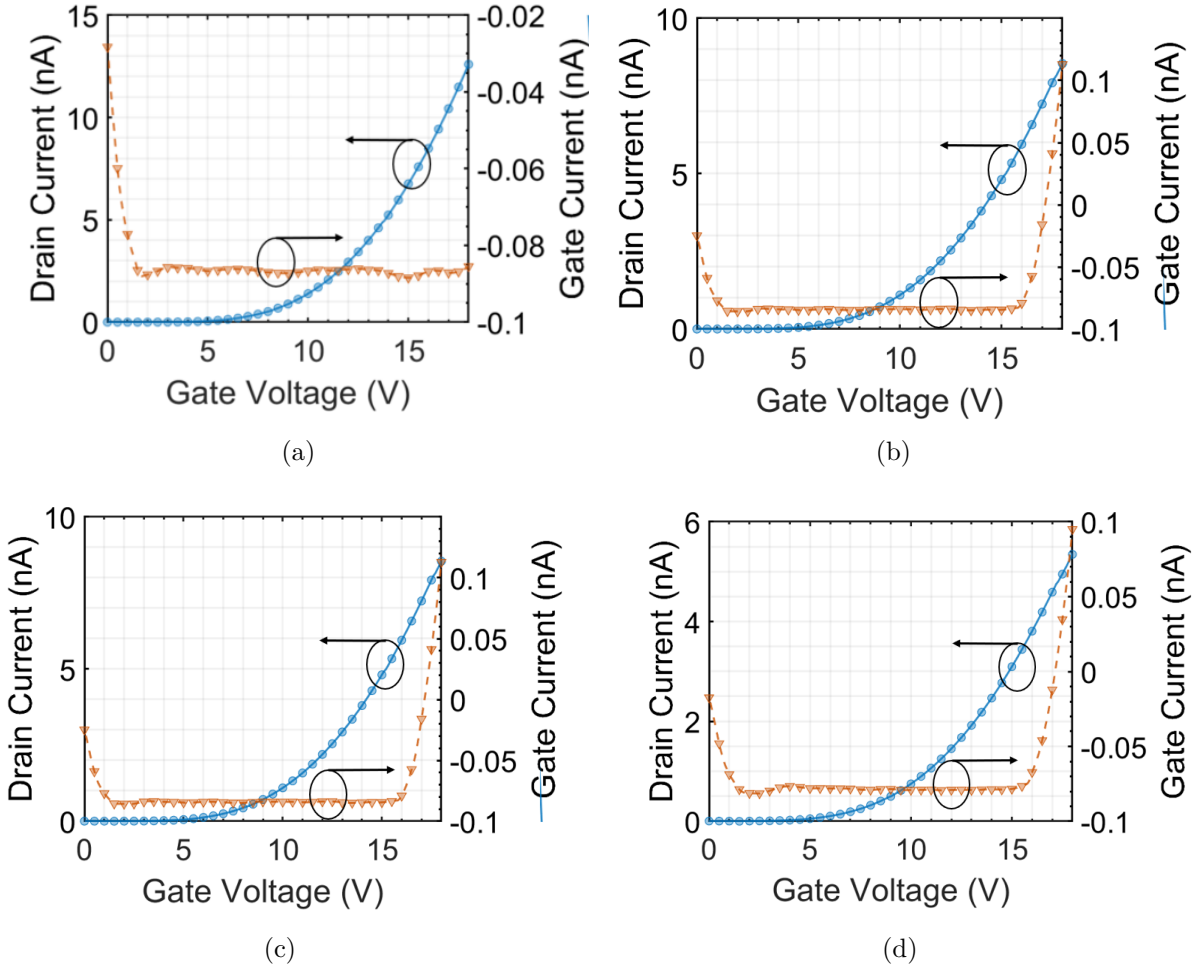


Figure 5.23. Transfer characteristics of lateral planar MOSFETs in the PCM region of sample 2Q4 for various channel length: (a) 49 nm; (b) 79 nm; (c) 109 nm, and (d) 179 nm.

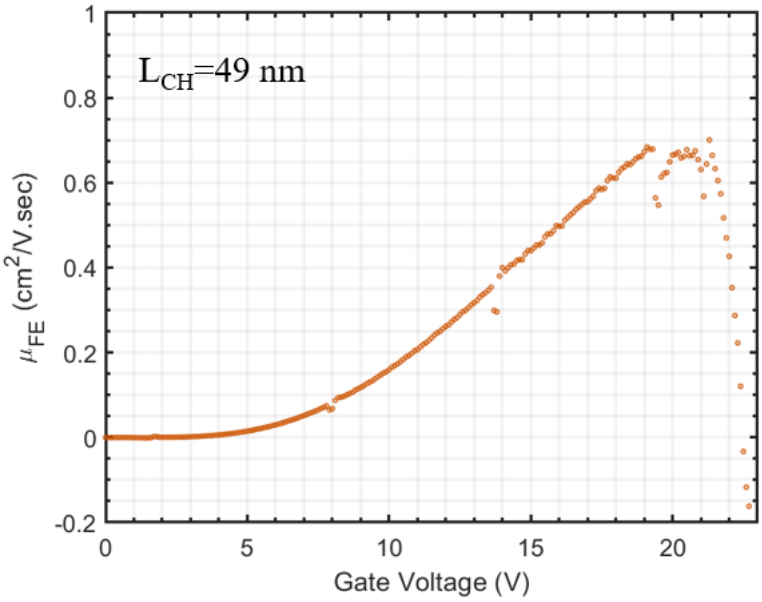


Figure 5.24. Field effect mobility of lateral planar MOSFETs in the PCM region of sample 2Q4.

The transconductance never reaches a peak, and gate oxide leakage becomes substantial compared to drain current at around 4.3 MV/cm. The threshold voltage is estimated from a linear extrapolation of the curve to be ∼7 V. The field-effect mobility extracted from a 49 nm channel length device is shown in Fig. 5.24, which shows a very low peak mobility, and drops steeply beyond 20 V because of gate leakage. A 100 kHz high-low C-V measurement was done on an n-CSL MOSCAP which shows around 1×10^{13} $1/(\text{cm}^2 \cdot \text{eV})$ of Dit which is an order of magnitude higher than the values reported in the literature [49]. The interface trap density analysis for both high-low and C-Ψ_S is shown in Fig. 5.25.

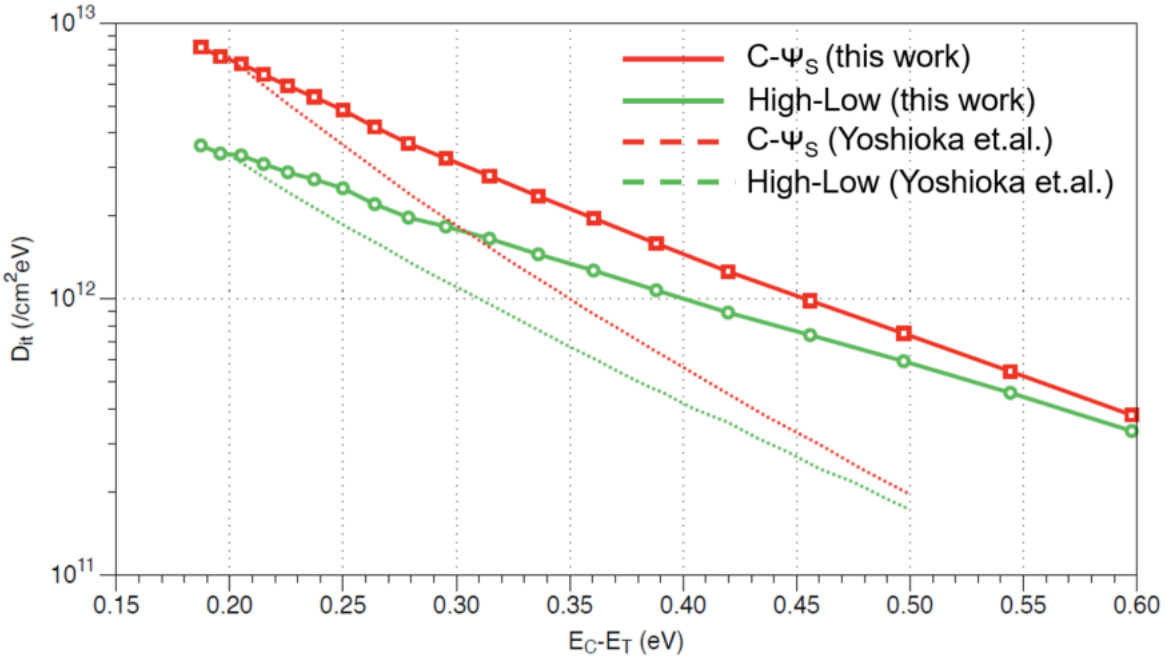


Figure 5.25. Interface trap density measurement on MOSCAP fabrication on the CSL layer in sample 2Q4 which is compared with the data reported in [49]

Finally, as mentioned before, during polysilicon oxidation during the gate oxide process, a thin layer of SiC was also oxidized. It is known that wet ambient oxidation produces less interface state density compared to the dry condition in the SiC thermal oxidation process [50]. Since a dry technique has been followed to oxidize the polysilicon, this may result in higher interface density at the SiC–SiO_2 interface. Furthermore, except for the nitric oxide anneal, no post oxidation treatment was done. It is reported that in situ Ar annealing after oxidation helps to reduce the interface state density [50]. Additionally, a short reoxidation at a lower temperature (900–950°C) can be performed to oxidize or diffuse any carbon compound dangling bonds near the interface [50]. At this low temperature, it is assumed that little to no further SiC will be oxidized. It is also reported that unloading the SiC sample from the oxidation tube at higher temperature can also produce a better interface [50]. The nitric oxide (NO) anneal can also be optimized by varying the temperature and duration [51]. The goal of NO anneal is to satisfy the interface dangling bonds in a nitrogen-rich ambient at high temperature.

5.6 Summary

In this chapter, the fabrication and characterization of first two runs of the Gen-1 tri-gate sample were discussed. Neither samples exhibited acceptable MOSFET behavior, but insightful information was extracted and process modifications identified that can be implement on future devices to solve these problems. A summary of suggested process modification is itemized below –-

- Polysilicon post implant mask in the p+ implant region can be redesigned to eliminate any post damage related problems. The proposed design change may also provide higher contact area to the p-well body, which could help improve device transient robustness.

- A thinner layer (50–100 nm) of Ni ohmic metal should be deposited, and a less aggressive surface roughening step should be developed

- Implant shadowing effect can be minimized by loading the samples in the same orientation in the different implanters. This will require clear communication with the third party implant service companies.

- The gate oxide formation process should be revisited, possibly by implementing wet ambient oxidation with an argon anneal post-oxidation anneal, low-temperature reoxidation, and an optimized NO anneal.

6. CONCLUSION AND FUTURE IMPROVEMENTS

The tri-gate 4H-SiC MOSFET is a novel approach that could push the SiC industry towards low into moderate voltage (400 V–900 V) applications, competing with Si and GaN devices. The inherent material properties and technological maturity of SiC device fabrication processes provide an opportunity for the potentially revolutionary unipolar tri-gate 4H-SiC MOSFET to replace bipolar Si MOSFET devices.

In this thesis, a detailed discussion of the development and implementation this complex structure is presented. The initial run of tri-gate devices failed due to a poor quality gate oxide, resulting in gate-to-drain shorts and poor mobility. Process modifications were suggested to solve these problems in the previous chapter. The project was continued with the rest of the partially fabricated Gen-1 and Gen-2 tri-gate samples by my colleague Dr. Ramamurthy. The process conditions were modified mainly by adding a gate trench hydrogen anneal, and in improved gate oxide and ohmic processes. The details of this process and the characterization of the resulting devices can be found in Dr. Ramamurthy's thesis [37]. In short, a H_2 anneal process was conducted at about 1500 after the trench etch to achieve a clean and smoothed sidewall surface. The process also rounds the sharp trench corners, which could help in reducing the field crowding and improve off-state performance. The gate oxide was formed using wet thermal oxidation at 1100, and an in-situ Ar anneal and a low temperature reoxidation at 900 was performed for oxide densification. These process changes improved the electrical characteristics drastically, as a peak mobility of 30 $cm^2/(V \cdot s)$ has been achieved after NO anneal oxidation. In the ohmic contacts, instead of 200 nm thick metal, as was used in the initial runs, a thinner 50 nm Ni was deposited, which consumes much less SiC in the ohmic anneal process. This prevents total consumption of thin P^+ layer which led to the gate-to-drain shorts in the previous Gen-1 2Q4 sample. A TLM study on the 50 nm deposited Ni showed good ohnmic contact performance, with a contact resistivity of 6–7 $\Omega \cdot cm^2$.

With these process modifications, devices from both Gen-1 (sample 3Q2) and Gen-2 (sample 400Q1) showed good device characteristics. Gen-2 tri-gate lot consists both a-face and m-face sidewall devices. Both variations were processed and measured. Here the perfor-

mance characteristics of devices from the Gen-2 400Q1 sample are shown where the sidewall was revealed on m-face. A 1 µm deep trenches were etched in this sample. A detail design layout and sample split of Gen-2 devices will be found in Appendix B and [37].

The output characteristics of a representative device are shown in Fig. 6.1 for gate voltages from -8 V to 18 V in 1 V steps.

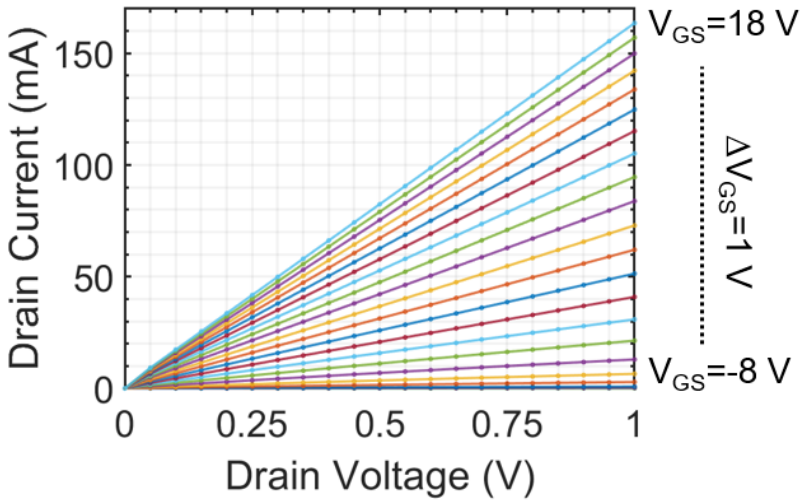


Figure 6.1. Output characteristics of a Gen-2 400Q1 tri-gate device.

The transfer characteristics of the 400Q1 sample are shown in Fig. 6.2. The figure also shows the conductance curve in orange and the extraction of a 1.5 V threshold voltage.

From the output characteristics, the specific on-resistance can be calculated, which is shown in Fig. 6.3 for a device with an area of 175 µm × 195 µm.

Figure 6.3 shows the specific on-resistance reduction with the gate voltage for both planar DMOSFET and Gen-2 400Q1 tri-gate device. At 4 MV/cm field operation ($V_{GS} = 18$ V), a 1.7× reduction of total on-resistance is obtained in tri-gate device. The novelty of tri-gate structure is to reduce the channel specific on-resistance which is reduced 3.7× compared to the DMOSFET as shown in Fig. 6.4. The extraction method of the channel specific on-resistance is described in [37]. An off-state measurement for a device from sample 400Q1

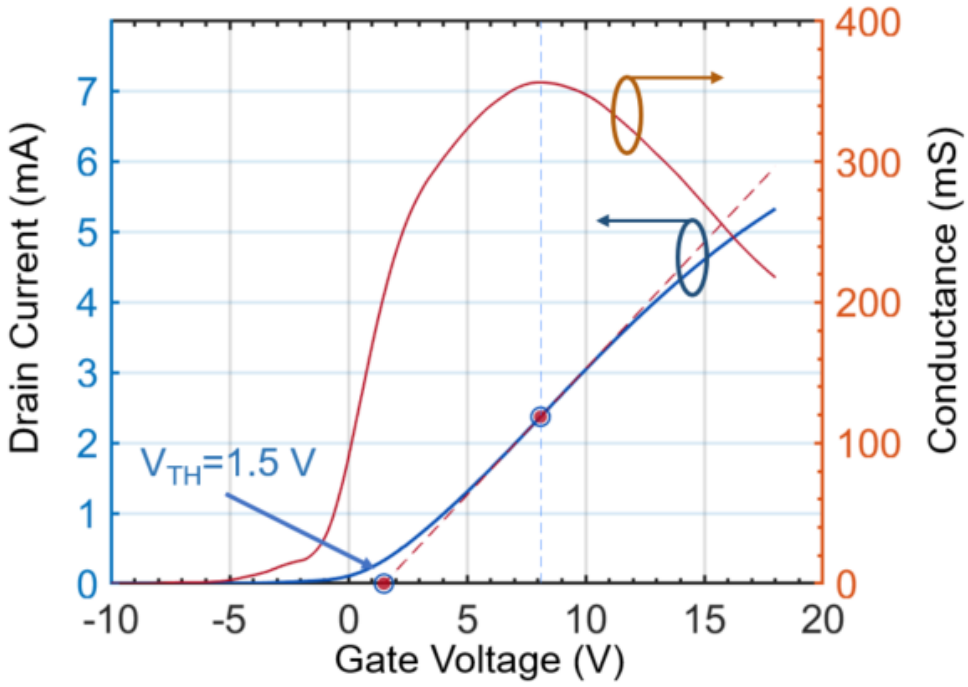


Figure 6.2. Transfer characteristics of a Gen-2 400Q1 tri-gate device.

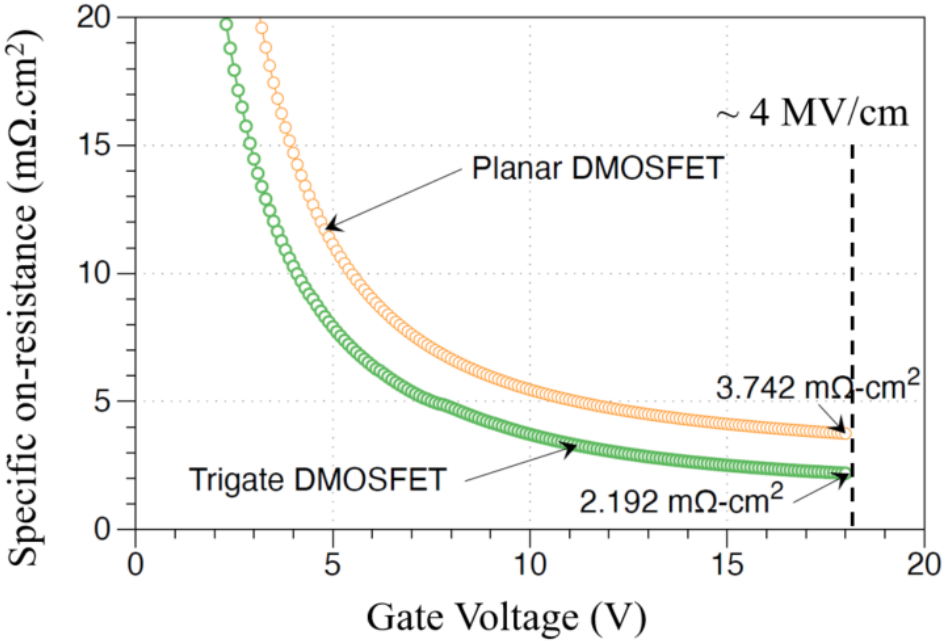


Figure 6.3. Specific on-resistance of Gen-2 400Q1 sample.

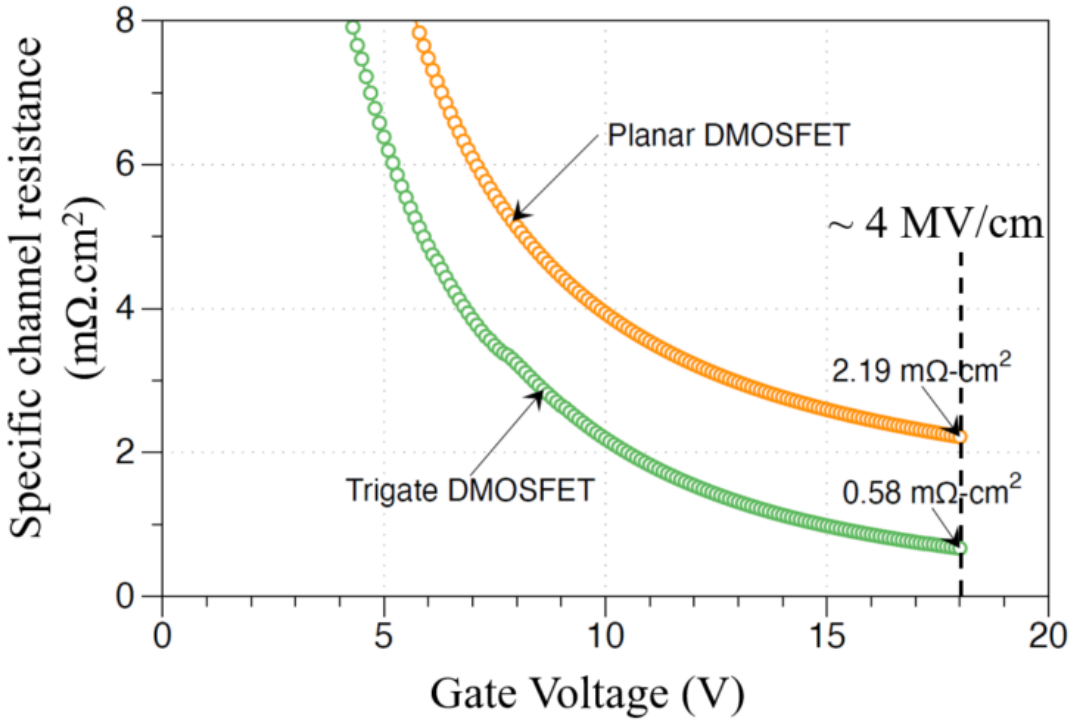


Figure 6.4. Specific on-resistance of Gen-2 400Q1 sample.

is also shown in Fig. 6.5. The device epi-layer and termination are designed for a 650 V application, and a breakdown voltage greater than 700 V is observed.

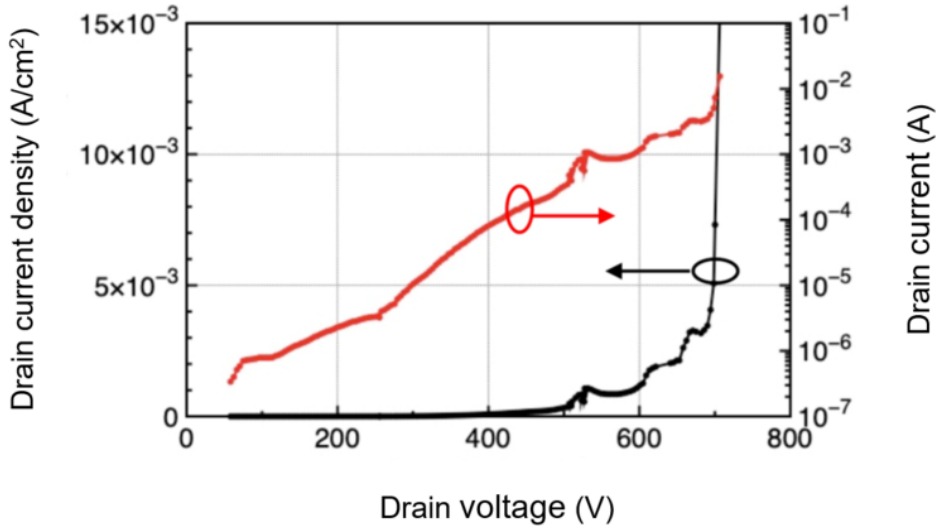


Figure 6.5. Off-state leakage and breakdown voltage of a Gen-2 device on sample 400Q1.

The initial development and characterization of a SiC tri-gate MOSFET described in this thesis shows significant promise in terms of reducing channel resistance, which is the major resistive component in mid-range voltage (400–900 V) SiC power MOSFETs. The utilization of additional sidewall channel width is now proven to reduce the total specific on-resistance by a factor of $\sim 2\times$ compared to a planar DMOSFET structure with similar dimensions and doping levels. Further improvement in resistance reduction could be achieved if steps were taken to minimize other resistance components, especially substrate resistance, as well as further improvements in the sidewall channel mobility. Moreover, the device reliability and switching characteristics need to be investigated. A few suggestions of possible future improvements are listed below:

1. Substrate resistance reduction: The full benefit of the tri-gate structure in reducing total resistance is muffled by other parasitic components; most notable is the resistance due to the substrate. In this thesis, no treatment is done to reduce substrate resistance. A common strategy to reduce the substrate resistance in the industry is to thin the wafer. Generally a 4″ SiC wafer substrate thickness is 350 µm. This normally thinned down to 100–200 µm which proportionally reduces the substrate parasitic resistance. Another novel way to reduce the resistance is to use a waffle etch and contact process

on the back side [52]. This approach etches most of the substrate material to within the 20 µm of the drift layer, but uses a waffle pattern to ensure sufficient mechanical strength.

2. Sidewall mobility: The sidewall mobility on the m-face in the Gen-2 PU400Q1 sample was measured to be around 10 $cm^2/(V \cdot s)$. A sidewall sacrificial oxidation and strip, H_2 anneal at high temperature and NO anneal at 1175°C were done to improve the sidewall oxide interface [37]. To achieve higher mobility on sidewall compared to Si-face [29], [38] tighter crystallographic orientation control, and further process related development are required.

3. Short circuit capability: The short circuit capability is measured as the time required to drive a device into a catastrophic thermal runaway failure after initiating a short circuit event. Normally half the rated blocking voltage is applied at the drain terminal, and a voltage pulse for a certain duration is imposed on the gate to initiate the short circuit condition. The drain current is measured and analyzed during the process to detect the failure point. Silicon carbide switching devices inherently suffer from low short circuit capability due to their capability to operate at significantly higher power density compared to Si devices. The key to improving the short circuit capability is to down scale the saturation current of the device, which can be achieved without affecting the channel resistance by using a constant gate charge scaling method [53]. An improvement on short circuit capability can also be achieved with an improved sidewall interface quality [54].

4. Drift layer resistance reduction: Normally a SiC power device is operated at elevated junction temperatures like 175°C. At this elevated temperature, the drift layer resistance increases due to mobility reduction by phonon scattering. As a result, the overall specific on-resistance may again be limited by the drift layer resistance. To approach this issue, a super-junction [55] type structure can be integrated with the tri-gate device, which will require a thinner and more heavily doped drift layer to achieve the rated blocking voltage. A superjunction drift layer will contribute less resistance compared a conventional structure.

5. Edge termination: The floated field ring structure was used for edge termination in this thesis. The termination parameters may need to be optimized, as the measured breakdown voltage (∼750 V) is significantly lower than the expected theoretical parallel plane breakdown voltage of (∼1000 V). The floating field ring termination approach is also known to be sensitive to the oxide interface charge. So other approaches like multiple floating guard ring edge termination claimed to be less sensitive to the interface charge could also be investigated [56]. The improved termination design may allow room to use slightly thinner and higher doped drift layer which may help reducing drift layer resistance. However, to date the channel resistance is the dominant resistance component in this class of application.

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A. FABRICATION STEPS FOR 4Q2 AND 2Q4 GEN-1 TRI-GATE SAMPLE

The detail fabrication and processing steps for both 4Q2 and 2Q4 Gen-1 tri-gate samples are given below. Both of the samples are processed in parallel until the implantation anneal step. After implant anneal, 4Q2 sample was taken first to finish the rest of the processing steps. This was then followed by the sample 2Q4. In some cases the fabrication steps were different between these samples which will be discussed.

A.1 Pwell Implant – (Optical Lithography)

1. RCA clean
2. Solvent clean - 5 min ultrasonication clean in toluene, acetone, methanol, and DI water bath
3. Thermal oxidation - 30 nm screen oxide was grown. The oxidation was done in a wet ambient at 1100°C
4. Polysilicon deposition - 6 µm Polysilicon deposited at 630°C and 580 mTorr pressure in LPCVD furnace
5. RCA clean
6. Polysilicon thermal oxidation - 200 nm of oxide was grown at 1100°C in a wet ambient. This oxide served as the field area mask during polysilicon etch to pattern implant block mask.
7. Solvent clean - 5 min ultrasonication clean in toluene, acetone, methanol, and DI water bath
8. Dehydration bake - 2 min at 110°C hot plate
9. Photo-lithography - 1.8 µm AZ1518 resist was deposited by spinning the resist at 4000 rpm for 40 sec. The resist was soft baked at 110°C for 2 min. The resist was

exposed in Mjb3 mask aligner at 10 mW/cm^2 intensity for 18 sec. The resist was developed in a two-bath MF26A solution for 20+8= 28 sec. Development was stopped in a 2 bath of water rinse for 10+60= 70 sec and a gentle squirting of water was followed for around 20 sec before nitrogen blow drying.

10. Resist Ash - The resist ashing was performed in the Branson barrel etcher in Ar/O2– 120/12(upper) 6(lower) sccm for 1 min at 100 W.

11. Oxide etch - oxide was etched in a BOE solution for 2 min. This opened the window in the active region where e-beam lithography was performed.

12. Resist Strip- AZ1518 resist was stripped by squirting and soaking in the acetone bath. The sample was cleaned in methanol bath

13. Registration mark for e-beam lithography - For the alignment of the next step e-beam lithography, a 1.2 µm polysilicon etch was performed with the patterned oxide mask in STS-ASE chamber for 30 sec. An oxide coated Si carrier wafer was used as the carrier wafer. The sample was bonded with carrier wafer using CrystalBond 555 adhesive from Ted Pella. The detailed etch recipe will be found in Table 4.3.

14. CrytalBond strip and sample clean- after the etch was done, the carrier wafer with the sample is placed on the hot plate at 60–65 celsius to melt the adhesive. The sample was carefully removed from the carrier wafer and the backside was cleaned by squirting water in a solvent bench. Later the sample was cleaned in the standard 5 min soak in acetone, methanol, and DI water bath respectively. The carrier wafer was cleaned in DI water bath with an ultrasonic agitation.

A.2 Pwell Implant – (E-beam Lithography)

1. Solvent clean- 5 min soak in toluene, acetone, methanol, and DI water bath.

2. Dehydration bake – 2 min at 125°C

3. HSQ FOX-16 deposition – the FOX-16 bottle was taken from the refrigerator and warmed for 30 min. A plastic pipette was used to draw the resist and dispense on the

sample. The resist was spun at 2000 rpm for 60 sec with a 4 sec ramp time. The resist was soft baked at 125°C for 3 min. This produces a 0.6 µm thick e-beam negative tone resist.

4. HSQ FOX-16 exposure- the resist was exposed in VB-6 Vistec e-beam lithography system at 100 kV, 95 nA current with 900 µC/cm^2 dose settings. The 30 nm of resolution was used for the exposure

5. Resist development – the exposed HSQ resist was developed in TMAH 25% base solution for 4.5 min followed by 5 min water rinse and nitrogen blow dry. Normally, 70 sec development is sufficient but after 70 sec development, HSQ residue was observed near the feature edges. So the development was carried in steps until a HSQ residue free feature was obtained.

6. Solvent clean- 5 min soak clean in toluene, acetone, methanol, and DI water bath

A.3 Pwell Implant – Polysilicon Etch

1. Mount to carrier wafer - The sample was mounted on 6″ oxide coated Si wafer using CrystalBond 555 adhesive from Ted Pella. Before mounting, the carrier wafer was cleaned in ultrasonication bath for 5 min each in toluene, acetone, methanol, and DI water bath. The carrier wafer was dried at hot plat at 60 °C. Then, the adhesive was rubbed carefully on the carrier wafer at the center. During rubbing, care was taken to prevent any exposure of the adhesive after the sample mount. The sample was placed on the adhesive coated location of carrier wafer and heated for 20 sec. Then the carrier was drawn out from the hot plate to cool down for 2 min. The adhesive condenses at this time and bonds the sample to the carrier wafer which cannot be pushed by the tweezer.

2. Polysilicon etch- the carrier wafer with the sample was loaded in the STS-ASE chamber and etched for 3.5 min to etch 5.6 µm of polysilicon with a recipe listed in Table 4.3. The etch was done in steps and each step it was monitored in the optical microscope to check complete polysilicon etch.

3. Demount- after the etch the carrier wafer was placed on the hot plate at 60°C. This melted the adhesive and the sample was carefully demounted from the carrier wafer. The backside of the sample was cleaned by squirting DI water. The carrier wafer was cleaned in the DI water ultrasonication bath.

4. Solvent clean- the sample was then cleaned by soaking in toluene, acetone, methanol, and DI water bath each for 5 min.

A.4 Pwell Implant – Third Party Process

1. Mount- the samples were mounted on 5″ Si carrier wafer using carbon tape. Care was taken to prevent any carbon tape exposure during implantation process.

2. High energy implantation – 680–4248 keV implant was performed in Ion Beam Services (IBS) at room temeprature. Due to long equipment downtime at IBS, the rest of the implants were done at CuttingEdge, Inc.

3. Low energy implantation - 20–480 keV implant was performed in CuttingEdge, Inc at room temperature.

A.5 Alignment Mark Etch

1. Solvent clean – the sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath

2. Dehydration bake – the sample was dehydrated at 110°C for 2 min.

3. Photolithography – AZ9260 resist was spun at 3000 rpm for 30 sec and baked for 3 min at 110°C. This resulted in a 8 µm thick resist. Before exposure ∼1 hr wait time was included for resist re-hydration. The resist was exposed in Mjb3 mask aligner tool at 10 mW/cm^2 power density for 42 sec. The resist was developed in a two bath of AZ400K: DI Water (320:80 mL) solution for a total 4 min 40 sec. The development was stopped by rinsing in water for 2 min followed by a gentle squirting of water for 20 sec.

4. Resist ash – the resist ashing was performed in Branson barrel etcher for 2 min in Ar/O_2– 120/12(upper) 6(lower) sccm setting at 100 W

5. SiC etch – SiC was etched in Panasonic ICP-RIE tool at 600 W ICP power, 200 W bias power, 3 Pa pressure in 20 sccm SF_6 ambient for 4min 40 sec in a step of 40 sec. This etched 0.9 µm of SiC in the registration mark window.

6. Resist strip – AZ9260 resist was stripped in acetone bath. The resist became hardened and a Branson barrel etch in 120/12(Upper) 6(lower) sccm Ar/O_2 was performed at 200 W for 15 min.

7. Solvent clean – the sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath.

A.6 N Source Implant Mask- in Active Area

The polysilicon fingers developed in the previous processing steps were oxidized to grow 1.0 µm of oxide with 0.5 µm lateral expansion which served as the mask for n-source implantation and thus defined the channel. The process flow will be found in Section 4.2 and a detail process parameters are listed in [37].

A.7 Source Implant Mask- in Field Area

1. Solvent clean- the sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath.

2. Dehydration bake – the sample was dehydrated at 110°C for 2 min.

3. Seed layer deposition – 15/500 nm of Ti/Au was sputtered on the sample for electrodeposition seed layer at 5 mTorr pressure. A higher pressure of 15 mTorr could also be used during deposition. For Gen-2 sample, 15 mTorr pressure was used.

4. Solvent clean- the sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath.

5. Photolithography – AZ9260 resist was spun at 3000 rpm for 30 sec with 4 sec ramp time. The resist was baked at 110°C for 3 min. This produced a 8 µm of resist film. Before exposure 1 hr of wait time was included for resist re-hydration. It was then exposed in Mjb3 mask aligner at 10 mW/cm^2 intensity for 60 sec. The resist was developed in a 2 baths of AZ400K: DI Water (320:80 mL) solution for a total 3 min 50 sec. The development was stopped in a DI water bath rinse for 2 min and a gentle 20 sec water squirting was followed.

6. Resist ash – the developed resist ashing was performed in Branson barrel etch tool in 120/12(upper) 6(lower) sccm Ar/O_2 for 2 min at 100 W.

7. Electrodeposition – nickel was electroplated at 15 mA current for 3 hr to give 2.8-–4 µm thick metal layer.

8. Resist strip – AZ9260 resist was stripped in PG remover bath at 70°C for 6 hours

9. Seed layer etch – Au was etched in Transene GE8148 solution for 3.5 min followed by multiple bath 15 min water rinse and soak. Ti was etched in Transene TFTN etchant for 2 min at room temperature. Technically, at room temperature, the etchant does not etch Ti. An elevated temperature is needed to etch Ti but there is also a risk to etch deposited Ni layer. So the thin Ti layer was unetched and served as a screening layer during implantation.

10. Solvent clean- the sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath.

A.8 N Source Implant – Third Party Process

1. Mount – the samples were mounted on 5″ Si carrier wafer using carbon tape as adhesive. During mounting care was taken to prevent any carbon tape exposure.

2. High energy implantation - 604–3009 keV nitrogen implant was performed at mi2-factory GmbH in Germany.

3. Demount – after the implantation the samples were demounted from the carrier wafer. The strong adhesion of carbon tape can be weakened by placing the carrier wafer in the a IPA bath. However, IPA solution cannot flow efficiently through the narrow space between the sample and carrier wafer mounted by the carbon tape. So the carbon tape is less exposed to IPA and demounting is not efficient. To expose the carbon tape, attempts of demounting needs to be taken time to time which will open the space for IPA to flow and react with carbon tape. This demounting process is more reliable and clean compared to demounting attempted on the wafer as received.

4. Solvent clean – the sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath.

5. Low energy implantation – 33–380 keV nitrogen implant was done at Cuttingedge, Inc at 500 celsius.

A.9 P+ Implant – (E-beam Lithography)

1. Polysilicon mask strip – the polysilicon mask was stripped in a multiple baths of HF:HNO_3 followed by BOE, piranha, and BOE clean

2. RCA clean - full RCA clean was performed.

3. Thermal oxidation – 30 nm screen oxide was grown for p+ implant process

4. Solvent clean- the sample was cleaned by ultrasonicating 5 min each in toluene, acetone, methanol, and DI water bath.

5. Dehydration bake – the sample was dehydrated at 180°C for 2 min

6. E-beam lithography: Dual resist layer of Copolymer EL11 and 950K PMMA A4 were used. Copolymer EL11 resist was spun at 1500 rpm for 45 sec with 4 sec ramp time. The resist was baked at 180°C for 3 min. Then the 950K PMMA A4 resist was spun at 4000 rpm for 45 sec with 4 sec ramp time. The resist was baked at 180°C for 3 min. This produced a total of 0.95 µm thick resist layer. The resist was exposed in Vistec VB6 e-beam lithography tool at 100 kV, 84 nA with 1300 µC/cm^2 dose. A 30 nm

resolution was used in the exposure. The exposed resist was developed in MIBK: IPA for 60 sec. The development was stopped in a IPA bath, rinsing the sample for 60 sec.

7. Resist ash: The developed resist ashing was performed in Branson barrel etch tool in 120/12(Upper) 6(lower) sccm flow of Ar/O_2 for 15 sec at 50 W

8. Metal deposition: Ti/Ni of 10/500 nm thick layer was deposited in the e-beam metal evaporation tool.

9. Liftoff- metal liftoff was performed in PG remover at 70°C batch for 13 hr, followed by acetone and IPA clean for 10 and 5 min respectively.

10. Solvent clean- the sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath.

A.10 P+ Implant – (Optical Lithography)

1. Solvent clean- the sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath.

2. dehydration bake – the sample was dehydrated at 180°C for 2 min

3. Photolithography- LOR 3B resist was spun at 2000 rpm for 30 sec and baked at 190°C for 5 min. The second layer of LOR 3B was spun at 2000 rpm for 30 sec and baked at 190°C for 5 min. AZ1518 resist was spun at 4000 rpm for 40 sec and baked at 110°C for 2 min. This produced a total resist thickness of 2.6 µm. The resist was exposed in Mjb3 mask aligner tool at 10 $\mu W/cm^2$ power density for 20 sec. The resist was developed in 2 baths of MF26A for total (20+8) 28 sec.

4. Resist ash: The developed resist ashing was performed in Branson barrel etch tool in 120/12(Upper) 6(lower) sccm flow of Ar/O_2 for 60 sec at 100 W

5. Metal evaporation- a 10/500 nm thick Ti/Ni metal layer was deposited in a e-beam metal evaporation tool.

6. Liftoff- the deposited metal was lifted off in PG remover bath at 70°C for 12 hours. The samples were cleaned in acetone and IPA bath for 10 and 5 min respectively.

7. Solvent clean- the sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath.

8. Third party implant - The samples were implanted in Cutting Edge Ion at 500°C

A.11 Implant Anneal

All samples were graphite capped during the implant anneal process to prevent any out diffusion of dopant from the surface. The graphite has been implemented by carbonization of photoresist layer at high temperature. The implantation anneal was performed in Epigress reactor tool at 1700°C for certain time. After anneal, the graphite cap was stripped in high temperature oxygen furnace. Details of the process steps will be found in [37].

A.12 Trench – (E-beam Lithography)

1. RCA clean - full RCA clean was performend on the samples.

2. Solvent clean- the sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath.

3. Dehydration bake – the sample was dehydrated at 180°C for 2 min

4. E-beam lithography – positive tone 950 K PMMA A6 resist was spun at 4000 rpm for 45 sec and baked at 180°C for 3 min. The resist was exposed in JEOL JBX 8100 FS tool at 100 kV in a dual current process. First, a 30 nA current 7 nm resolution exposure with a dose was done to define the trench mask in the active area. Then, a 100 nA, 20 nm resolution exposure was performed to define the outer edge of the mask in the active area. The exposed resist was developed in MIBK: IPA for 60 sec and the development was stopped in IPA, rinsing the sample for 30 sec.

5. Resist ash: This process was done on sample 2Q4 but it is not done for sample 4Q2. The resiude of developed resist was cleaned in Branson barrel etch tool in 120/12(Up-

per) 6(lower) sccm flow Ar/O_2 for 15 sec at 50 W. The resist on sample 4Q2 was not done because this process potentially causes increase of resist line edge roughness which impact the roughness of the deposited metal mask and thus the SiC etch shape. On the other hand, the resist ashing is recommended for achieving a good lift-off metal pattern.

6. Metal deposition: Ti/Ni (15/200) nm metal stack layer was deposited in an e-beam evaporation tool

7. Liftoff- The deposited metal was lifted off in a hot bath of PG Remover for 5 hr followed by Acetone and IPA soak for 10 and 5 minutes respectively

8. Solvent clean- The sample was soaked for 5 min each in a bath of toluene, acetone, methanol, and DI water.

A.13 Trench – (Optical Lithography)

1. Solvent clean- The sample was soaked for 5 min each in a bath of toluene, acetone, methanol, and DI water.

2. Photolithography – Positive tone AZ9260 was spun on the sample at 2000 rpm for 30 sec to achieve 10 µm of resist. The soft bake was done at 110°C for 3 min. A 1 hr of wait time was included before exposure for the resist rehydration. The resist was exposed in the mask aligner Mjb 3 tool at 8 mW/cm^2 intensity for 75 sec. The resist was developed in AZ400K: DI (80:320 mL) solution for 3 min 50 sec, followed by rinsing and squirting the sample in DI water for 2 min.

3. Resist Ash- This step was not performed on 4Q2 sample but followed in sample 2Q4. The developed resis residue was cleaned in Branson barrel etch tool in 120/12(Upper) 6(lower) sccm flow of Ar/O_2 for 90 sec at 100 W.

A.14 Trench Etch

A.14.1 Trench Etch - Sample 4Q2

1. Carrier wafer mount- 4Q2 sample was loaded in a 4″ Si carrier wafer using Santovac vacuum oil on a hot plate at 70°C. Care was taken such that no oil becomes exposed during the etch process

2. Etch – the sample was etched in Oxford Plasma Pro 100 tool in Notre Dame university nanofabrication facility. The etch was performed for 3 min 45 sec according to the parameter shown in Table 4.8. This resulted in a 1.5 um deep trench in the high resolution feature (0.5 µm wide fin and trench fingers).

3. Resist strip- The resist was stripped in acetone by squirting and soaking for 5 min followed by a methanol soak for 2 min

4. Mask strip- Any hardened resist and Ti/Ni mask was stripped in piranha for 15 min followed by a 5 min DI water rinse. The process was repeated one more time and the sample was cleaned in a diluted HF bath for 2 hr. Finally, a 5 min DI water rinse was done to complete the process.

5. Solvent clean- The sample was cleaned in solvents by soaking 5 min each in toluene, acetone, methanol, and DI water bath

A.14.2 Trench Etch- Sample 2Q4

1. Carrier wafer mount- 2Q4 sample was loaded in a 4″ Si carrier wafer using CrystalBond 555 on a hot plate at 60°C. Care was taken such that no adhesive material becomes exposed during the etch process.

2. Etch – the sample was etched in Oxford Plasma Pro 100 tool in Notre Dame university nano-fabrication facility. The sample was etched for 4 min according to the parameter shown in Table 4.8 except the chuck temperature was set to 20°C. The etch resulted in a 1.8 µm deep trench in the finer resolution feature (0.5 µm wide fin and trench fingers).

3. Resist strip- The resist was stripped in acetone by squirting and soaking for 5 min followed by a methanol soak for 2 min

4. Mask strip- Any hardened resist and Ti/Ni mask was stripped in piranha for 15 min followed by a 5 min DI water rinse. The process was repeated one more time and the sample was cleaned in a diluted HF bath for 2 hr. Finally, a 5 min DI water rinse was done to complete the process.

5. Solvent clean- The sample was cleaned in the solvent by soaking 5 min each in toluene, acetone, methanol, and DI water bath

A.15 Field Oxide Deposition

Field oxide deposition was performed on sample 4Q2 and 2Q4. But later, it was stripped from the sample 2Q4 due to the lack of proper deposition tool and process recipe development as discuss in Section 4.7.

1. RCA and Solvent clean- 4Q2 sample was cleaned in a standard RCA cleaning bath and it was followed by a solvent cleaning 5 min each in toluene, acetone, methanol, and DI water bath.

2. Polysilicon deposition – A 200 nm of polysilicon was deposited in ProTemp LPCVD tube 6 at 600 mTorr pressure.

3. Oxidation – The polysilicon was then fully oxidized in a wet ambient

4. NO anneal – The oxidized poly was then annealed in the NO tube at 1175°C for 2 hours

5. Process repeat- Polysilicon deposition, oxidation, and NO anneal process are repeated 2 more times to achieve 1 µm thick field oxide

Even, the process of polysiiocn deposition and oxidation was divided into 3 steps, a trace of unoxidizied polysilicon found in sample 4Q2.

A.16 Field Oxide Etch

1. Solven clean- The sample was cleaned in solvents by soaking 5 min each in toluene, acetone, methanol, and DI water bath

2. Dehydration bake – The sample was dehydrated at 110°C for 2 min

3. Photolithography – A positive tone AZ9260 resist was spun at 2000 rpm for 30 sec to achieve a 10 µm thick resist. The resist was soft baked at 110°C on a hot plate for 3 min. A wait time of 1 hr was included for resist re-hydration. It was then exposed in Mjb-3 mask aligner tool at 10 mW/cm^2 power density for 60 sec and developed in AZ400K: DI (1:4) water bath for 4 min 40 sec. The development was stopped and the sample was cleaned by rinsing it in a bath of DI water.

4. Resist ash- The developed resist ashing was done in Branson barrel etcher at 100 W for 90 sec with 120 sccm Ar and 12(upper) 6(lower) sccm O_2 flow

5. Oxide etch- The field oxide was etched in BOE bath for ∼30 min. A significant field oxide broadening was observed due to resist peeling issues.

6. Resist strip- The resist was stripped in a hot bath of PG remover followed by acetone and IPA cleaning

7. Solvent clean- The sample was cleaned by soaking 5 min each in toluene, acetone, methanol, and DI water bath

A.17 Gate Oxide

A.17.1 Gate Oxide- Sample 4Q2

1. Cleaning – The sample was cleaned in a piranha bath for 10 min.

2. Polysilicon deposition – The polysilicon was deposited in the LPCVD furnace at 630°C for 2 min. A 26 nm thick polysilicon layer was deposited.

3. Oxidation – The deposited polysilicon was thermally oxidized in a wet ambient at 1100°C. This resulted full thermal oxidation of the polysilicon layer to obtain around 50 nm of gate oxide.

4. NO anneal – The thermally grown oxide was then annealed in NO anneal tube at 1175°C for 2 hours

A.17.2 Gate Oxide - Sample 2Q4

1. RCA clean- The sample was cleaned in a RCA bath followed by the solvent cleaning

2. Polysilicon deposition – The polysilicon was deposited in the LPCVD furnace at 580°C for 7 min. A 23 nm thick polysilicon layer was deposited.

3. Oxidation- The deposited polysilicon was fully oxidized at 1100°C in a dry ambient for 45 min. A 46 nm thick thermally grown oxide was obtained.

4. NO anneal- The grown oxide was annealed in the NO tube at 1175°C for 2 hours.

A.18 Gate Polysilicon Deposition

1. Cleaning – The sample was then cleaned in Piranha and standard solvent bath

2. Polysilicon deposition – 1 µm thick polysilicon was deposited in the polysilicon LPCVD furnace at 630°C and 580 mTorr pressure for 80–85 min.

A.19 Gate Polysilicon Doping

A.19.1 Gate Polysilicon Doping - Sample 4Q2

1. Spin on Dopant (SOD) bottle warm-up – Spin on Dopant P509 bottle (250 mL) was warmed for 24 hr

2. Sample cleaning – The sample was cleaned in BOE and then dehydrated in a hot plate at 100℃ for 2–5 min

3. SOD deposition – SOD was then spread on the sample at 500 rpm for 2 sec in the spinner and deposited by spinning at 2500 rpm for 12 sec

4. SOD bake – SOD was then baked at 200°C for 20 min and allowed to cool down to 160°C

5. Drive in- The sample was then loaded in a furnace at 800°C and SOD was diffused at 1000°C for 2 hours in N_2 ambient.

6. BOE dip- The grown phospho silicate glass (PSG) was stripped in a BOE bath for 8–10 min .

A.19.2 Gate Polysilicon Doping - Sample 2Q4

1. Spin on Dopant (SOD) bottle warm-up – Spin on Dopant P509 bottle (4 mL bottle) was warmed or 2 hr

2. Sample cleaning – The sample was cleaned in BOE and then dehydrated in a hot plate at 100°C for 2–5 min

3. SOD deposition – SOD was then spread on the sample at 500 rpm for 2 sec in the spinner and deposited by spinning at 300 rpm for 20 sec

4. SOD bake – SOD was then baked at 200°C for 20 min

5. Drive in- The sample was then loaded in a furnace at 850°C and SOD was diffused at 1000°C for 2 hour in 75 % N_2 and 25 % O_2 ambient. The sample was also unloaded at 850°C

6. BOE dip- The grown PSG was stripped in a BOE bath for 8–10 min.

A.20 Gate Pattern

A.20.1 Gate Pattern - Sample 4Q2

1. Solvent clean- The sample was cleaned in 5 min each in toluene, acetone, methanol, and DI water bath

2. Dehydration bake- The sample was dehydrated at 150°C for 2 min

3. E-beam lithography – All resist CSAR 62 was deposited on the sample by spinning at 4000 rpm for 60 sec. The resist was baked at 150°C for 3 min. It results in around 400 nm thick resist which was then exposed in JEOL 8100 FS lithography tool at 200 nA beam current, 100 kV voltage, and 280 µC/cm^2 dose. Lithography was one step and no photolithography was followed after this. The resist was developed in xylene for 70 sec and development was stopped in IPA for 1 min. For sample 4Q2, 0.75 µm gate-source overlap design was used.

4. Resist ash- The developed resist was ashed in Branson tool for 20 sec at 50 W in 120 sccm Ar and 12(upper) 6(lower) sccm O_2 plasma

5. Carrier wafer mount – The sample was mounted on a 6″ Si carrier wafer with Crystal-Bond 555 at a hot plate of 60-70°C temperature

6. Polysilicon etch – The sample was loaded in the STS ASE tool and polysilicon was etched for 2 min 40 sec to etch around 1300-1400 nm of polysilicon.

7. Sample demount and clean- The sample was the demounted by applying temperature. The backside was cleaned in DI water and the CSAR resist was stripped in PRS2000 for 9 hr. The sample was then cleaned in acetone and IPA for 5 min each.

A.20.2 Gate Pattern - Sample 2Q4

1. Solvent clean- The sample was cleaned in 5 min each in toluene, acetone, methanol, and DI water bath

2. Dehydration bake- The sample was dehydrated at 150°C for 2 min

3. E-beam lithography – All resist CSAR 62 was deposited on the sample by spinning at 4000 rpm for 60 sec. The resist was baked at 150°C for 3 min. It resulted in around 400 nm thick resist which was then exposed in JEOL 8100 FS lithography tool at 30 nA beam current, 100 kV voltage, and 300 µC/cm^2 dose. The resist was developed

in xylene for 70 sec and development was stopped in IPA for 1 min. For sample 2Q4, 0.60 µm gate source overlap design was used.

4. Poly Etch – The sample was mounted on 6″ Si carrier and loaded into the STS ASE tool and polysilicon was etched for 2 min 10 sec according to the parameter listed in Table 4.3 to etch around 1300-1400 nm of polysilicon

5. CSAR mask strip- The CSAR mask was then stripped in hot bath of PG remover for 5 hr.

6. Solvent clean- The sample was cleaned in acetone and IPA for 10 min each. Then the sample was again cleaned in toluene, acetone, methanol, and DI water for 5 min each

7. Dehydration bake- The sample was dehydrated at 110°C for 2 min

8. Photolithography – AZ9260 resist was the spun at 4000 rpm for 30 sec. This resulted in a 6 µm thick resist. The resist was rehydrated at least for an hour. It was then exposed in MLA Heidelberg mask less aligner tool at 500 mJ/cm^2. The resist was developed in AZ400K:DI water (80:320 mL) for 2 min 30 sec.

9. Poly Etch – The polysilicon in field and PCM region was etched in the STS -ASE tool. The sample was mounted in a 6″ Si carrier wafer with Crystal bond 555 and etched in STS-ASE tool for 2 min according to the parameter listed in Table 4.3. After etch, the sample was demounted applying temperature and backside was cleaned in DI water.

10. Resist strip- The resist was stripped in hot bath of PG remover overnight and resist hardening was observed. PRS 2000 for 2 min was also attempted but the harden resist was not stripped. The sample was then loaded in the Branson tool and resist stripped at 300 W for 3 min in 120 sccm Ar and 12(upper) 6(lower) sccm O_2 plasma.

11. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

A.21 Inter Layer Dielectric (ILD) Growth

1. Clean- The sample was cleaned in a piranha bath

2. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

3. Poly Oxidation for ILD – The sample was then loaded in the oxidation furnace 4 to oxidize in a wet ambient for 205 min at 1100°C temperature to grow around 920 nm of oxide

A.22 Ohmic Metal Deposition

A.22.1 Ohmic Metal Deposition - Sample 4Q2

1. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

2. Photolithography- Bi-layer resist of LOR 3B and AZ1518 is used. The sample was dehydrated at 180°C for 2 min and LOR 3B resist is spun at 2000 rpm for 30 sec and baked at 190°C for 5 min. Then AZ1518 was spun on the sample at 4000 rpm for 40 sec and baked at 110°C for 2 min. The resist was exposed in Mjb-3 mask aligner for 18 sec at 14 mW/cm^2 dose and developed in MF26A bath for total 26 sec. The sample was then rinsed and squirted in DI water.

3. Oxide etch – The oxide in the ohmic layer was etched in a BOE bath for 21 sec

4. Surface roughening etch prior metal deposition – The sample was then etched in Jupiter CCP etcher at 100 W 10/20 sccm SF$-_6$/Ar plasma for 1 min. The etch consumed 26 nm of SiC. This was then loaded in the Branson etcher to oxidize any polymer formed during Jupiter etch. In Branson, the sample was etched for 1 min at 100 W in 120 sccm Ar / 12(upper) 6(lower) sccm O_2 plasma. The oxidized polymer was etched in BOE bath for 20 sec

5. Metal deposition – 200 nm thick Ni was evaporated in a metal e-beam evaporator

6. Liftoff – The deposited metal was lifted off in a hot bath of PG remover for 6–8 hours. The sample was cleaned in a IPA bath for 20 min.

7. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

A.22.2 Ohmic Metal Deposition - Sample 2Q4

1. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

2. Photolithography- Bi-layer resist of LOR 3B and AZ1518 was used. The sample was dehydrated at 180°C for 2 min and LOR 3B resist is spun at 2000 rpm for 30 sec and baked at 190°C for 5 min. Then AZ1518 was spun on the sample at 4000 rpm for 40 sec and baked at 110°C for 2 min. The resist was exposed in MLA 150 Heidelberg maskless aligner at 200 mJ/cm^2 dose and developed in MF26A bath for total 26 sec. The sample was then rinsed and squirted in DI water.

3. Oxide etch – The oxide in the ohmic layer was etched in a BOE bath for 20 sec

4. Surface roughening etch prior metal deposition – The sample was then etched in Jupiter CCP etcher at 100 W 10/20 sccm SF_6/Ar plasma for 1 min. The etch process consumed 26 nm of SiC. This was then loaded in the Branson etcher to oxidize any polymer formed during Jupiter etch. In Branson, the sample was etched for 1 min at 100 W in 120 sccm Ar / 12(upper) 6(lower) sccm O_2 plasma. The oxidized polymer was etched in BOE bath for 20 sec

5. Metal deposition – 200 nm thick Ni was evaporated in a metal e-beam evaporator

6. Liftoff – The deposited metal was lifted off in a hot bath of PG remover for 6–8 hours. The sample was cleaned in a IPA bath for 20 min.

7. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

8. Metal strip – The lift off metal suffered a yield loss due to the exhaustion of the source material during the deposition. So the metal was stripped in Piranha and the whole process from cleaning to the liftoff was repeated. But in the second time, the ohmic anneal at 750°C resulted formation of NiO compound due to gasket leak in the tool. So the metal had to be stripped one more time and third attempt of metal deposition was done. Second time, to strip the NiO compound, simple piranha etch did not work. A multi bath etch of Aqua regia, HCl/H_2O_2 (5:1), and NH_4OH were used to strip the NiO compound.

A.23 Ohmic Anneal

1. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

2. First step anneal- The sample was annealed in the Jipelec RTA tube. The tube was first baked at 1000°C for 5 min to dehydrate any moisture. The sample was then loaded upside down on a clean 20 nm oxide coated Si sample. The Si sample was placed on the 6″ inch carrier wafer required in the tube. 15–20 Ti pellets were also used around the sample, placing on 1 × 1 cm^2 Si samples. Ti pellets were used to absorb any oxygen present in the tube. After loading the sample, the tube was pumped and purged in a multi step process using Ar. Finally, the sample was annealed at 750°C for 3 min in atmospheric pressure to form nickel silicide.

3. Unreacted Ni strip – Unreacted Ni in the first anneal step was stripped in piranha for 10 min

4. Backside metal deposition- The front surface was protected with 12 µm AZ9260 resist. Backside was cleaned in the BOE bath for 4 min 30 sec and in the Jupiter plasma etcher at 100 W 10/20 sccm SF_6/Ar for 3 min. 200 nm Ni was deposited on the back using a e-beam metal evaporator. Front side resist was stripped in hot bath of PG remover for 1 hour 30 min.

5. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

6. Second step anneal – Similar loading procedure like in the first step anneal was followed in this step. The sample was annealed at 1000°C for 3 min.

7. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

A.24 RIE Etch - Sample 4Q2

1. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

2. Plasma etch – The annealed surface contaminant was etched in Jupiter CCP etcher at 100 W for 1 min in SF_6/Ar 10/20 sccm plasma. This etch is recommended before top metal deposition. Since the Jupiter etch recipe is very aggressive on polysilicon so this etch could not be performed after ILD opening while polysilicon gets exposed. This etch was not performed in sample 2Q4 since it had only 50 nm thick field oxide which would get etched during this process.

3. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

A.25 ILD Etch

A.25.1 ILD Etch - Sample 4Q2

1. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

2. Photolithography – The sample was dehydrated at 110°C for 2 min and AZ1518 is spun at 4000 rpm for 40 sec. It was then exposed in the Mjb-3 mask aligner at 10 mW/cm^2 dose for 18 sec. The resist was developed in MF26A for total 26 sec, followed by water rinsing and squirting.

3. Resist ash- The developed resist was then ashed in the Branson tool at 100 W for 1 min in 120 sccm of Ar / 12(upper) 6(lower) sccm of O_2 plasma

4. BOE etch – ILD was then etched in a BOE bath for 14 min. Significant resist peeling was observed.

A.25.2 ILD Etch - Sample 2Q4

1. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

2. Photolithography – The sample was dehydrated at 110°C for 2 min and AZ9260 is spun at 4000 rpm for 40 sec. It was then exposed in MLA 150 Heidelberg mask-less aligner at 500 mJ/cm^2. The resist was developed in AZ400K: DI water (80:320 mL) for total 2 min 30 sec, followed by water rinsing and squirting.

3. Resist ash- The developed resist was then ashed in the Branson tool at 100 W for 90 sec in 120 sccm of Ar / 12(upper) 6(lower) sccm of O_2 plasma

4. RIE etch – ILD was then etched in the Panasonic E620 tool in CF_4/CHF_3 chemistry for 13 min according to the parameter listed in Table 4.10.

5. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

A.26 Top and Back Metal Deposition

1. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

2. Metal sputter- The Ti/Au metal was sputtered on the samples. For 4Q2 sample 25/800 nm of Ti/Au was sputtered and for sample 2Q4 25/1200 nm of Ti/Au was sputtered.

3. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

4. Photolithography – The sample was dehydrated at 110°C for 2 min and AZ9260 is spun at 4000 rpm for 40 sec. It was then exposed in MLA 150 Heidelberg maskless aligner at 500 mJ/cm^2. The resist was developed in AZ400K: DI water (80:320 mL) for a total 2 min 30 sec, followed by water rinsing and squirting.

5. Au etch – The Au etch was performed in Transene GE8148 Au etcher for 3–4 min

6. Ti etch – The Ti etch was performed in Transene TFTN etcher at elevated temperature (75-80°C) for 1–1.5 min

7. Backside metal- The front surface was protected with 10 µm thick AZ9260 photoresist. The backside metal Ti/Au 10/100 nm was deposited in a metal e-beam evaporator.

8. Solvent clean- The sample was cleaned 5 min each in toluene, acetone, methanol, and DI water bath

This concludes the detail fabrication flow for tri-gate power device. In next chapter, various measurements from test sample and tri-gate device will be discussed.

B. GEN-2 TRI-GATE IMPLANTATION DESIGN AND DEVICE LAYOUT

Gen-2 tri-gate device is aimed for 1 µm SiC trench. The wafer list for fabrication is given in the Table 4.1 with the drift-epi layer and CSL layer information. In all samples, the CSL layers is thinned to 1.6 µm which is 0.1 µm less deep than the P-well junction depth. This ensures improved breakdown characteristics as described in Chapter 4. The detail processing and characterization of these samples will be found in my colleuage Dr. Ramamurthy's thesis [37]. Here the designed implantation profile and device map are briefly discussed.

Figure B.1 shows the designed Al and N implant for p-well and source region respectively. The full implantation energy and dose for both of the implants are listed in the Table B.1 and Table B.2 respectively. The first split of this lot involves the variation of sidewall face of tri-gate devices in different samples. The sample PU394Q4 and PU400Q4 were designed to reveal sidewall on a-face while sample PU394Q1 and PU400Q1 were designed to open sidewall face on m-face as shown in Fig. B.2.

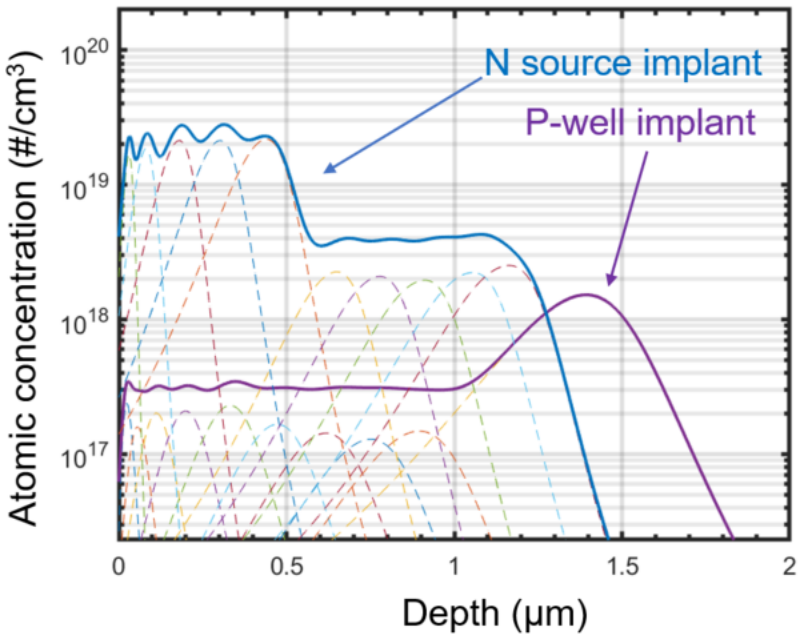

Figure B.1. Gen-2 tri-gate implant design.

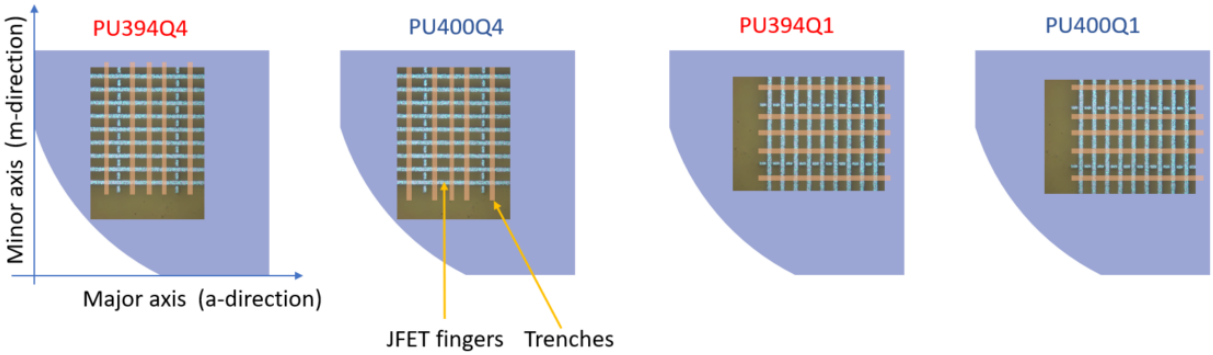

Figure B.2. Gen-2 tri-gate: Sidewall direction variation.

Table B.1. Gen-2 tri-gate – p-well aluminum implant profile

Energy (keV)	Dose (#/cm^2) $\times 10^{12}$
1830	60.0
1000	5.0
800	4.0
630	4.0
460	4.0
310	4.5
180	3.0
100	2.0
50	1.0
20	0.8

Like gen-1, gen-2 samples consist of 12 combination of devices with variation on JFET length and source contact length. The devices are named in an alphabetic order with a combination of JFET and full source contact length listed in Table. B.3. These letters were inscribed in the sample on bottom left corner of each device at alignment mark etch process for easy recognition during sample inspection and characterization. However, the dimensions of these letter in lithographic design was too tight to develop very clearly in the sample. Each die in the sample is comprised of 4 sub-dies as shown in Fig. B.3. In each sub-die consists of 20 devices as shown in Fig. 3.4 in Chapter 3. But here the main difference is edge termination design has been varied for a specified device in different sub-die level. We have designed 4 FFR termination design with the parameter listed in Table. B.4. In different sub-dies, all 4 FFR design were incorporated for a specific combination of device

Table B.2. Gen-2 tri-gate – n-source aluminum implant profile

Energy (keV)	Dose (#/cm^2) $\times 10^{14}$
1300	0.7
1130	0.6
920	0.5
740	0.5
580	0.5
350	4.0
220	3.2
120	2.4
50	1.2
18	0.5

type as shown in Table. B.5. For an example, for device A in sub-die no.1, the FFR-1 has been incorporated while in sub-die no.4 FFR-4 has been used.

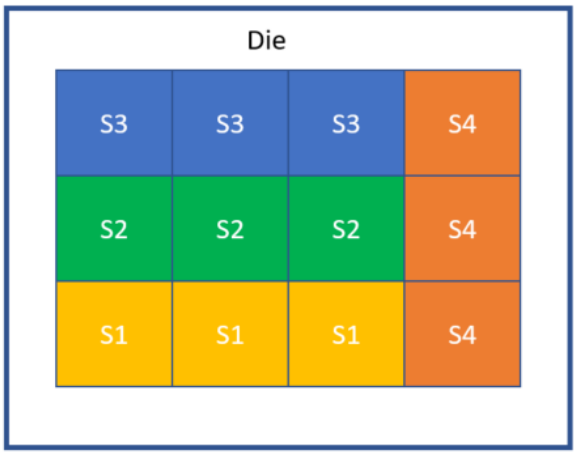

Figure B.3. Gen-2 tri-gate: Die map.

Table B.3. Gen-2 tri-gate device combination

Device name	JFET length (µm)	source contact length (µm)
A	2.0	1.0
B	2.0	3.0
C	2.5	1.0
D	2.5	3.0
E	3.0	1.0
F	3.0	3.0
G	3.5	1.0
H	3.5	3.0
I	4.0	1.0
J	4.0	3.0
K	4.5	1.0
L	4.5	3.0

Table B.4. Gen-2 FFR design with 5% expansion ratio on space and width

FFR name	Initial space (µm)	Initial width (µm)
FFR-1	1.15	1
FFR-2	1.25	1
FFR-3	1.35	1
FFR-4	1.45	1

Table B.5. Gen-2 tri-gate device FFR map

Device name	Sub-die 1	Sub-die 2	Sub-die 3	Sub-die 4
A	FFR-1	FFR-2	FFR-3	FFR-4
B	FFR-4	FFR-1	FFR-2	FFR-3
C	FFR-3	FFR-4	FFR-1	FFR-2
D	FFR-2	FFR-3	FFR-4	FFR-1
E	FFR-1	FFR-2	FFR-3	FFR-4
F	FFR-4	FFR-1	FFR-2	FFR-3
G	FFR-3	FFR-4	FFR-1	FFR-2
H	FFR-2	FFR-3	FFR-4	FFR-1
I	FFR-1	FFR-2	FFR-3	FFR-4
J	FFR-4	FFR-1	FFR-2	FFR-3
K	FFR-3	FFR-4	FFR-1	FFR-2
L	FFR-2	FFR-3	FFR-4	FFR-1

C. NICKEL ELECTROPLATING

For both gen-1 and gen-2 tri-gate fabrication, thick Ni was used as the n-source implant mask on PCM and bulk area. The Ni electroplating recipe was developed by my colleague Dr. Opondo. This deposition technique was based on custom made solution and here I am describing my notes taken while developing Ni electroplate mask for gen-2 tri-gate sample fabrication. The required seed layer for this process has been discussed in Chapter 4 and so it is not repeated here.

- Prior using the glass beakers for the Ni electroplating process, all of them were cleaned in standard piranha solution in the cleanroom, followed by at least acetone and methanol soak or full standard solvent clean which is toluene, acetone, methanol, and DI water soak
- A standard 99.9% pure Ni bar was used as the anode. The bar was soaked in methanol and DI water for cleaning purpose.
- 1000 mL of DI water was taken on a glass beaker and placed on a hot plate
- 450 gm of Ni Sulphamate was added
- 45 gm of Ni chloride was added
- 30 gm of Boric acid was added
- 35 gm of Ni carbonate was added
- All weights were measured in the precision weighting scale available in the lab
- Teflon coated thermocouple was used to measure the temperature and a Teflon coated magnet was used for striation.
- The solution is stirred at 200 rpm at 50 °C
- Boric acid was not seen to be mixed well
- The striation speed was increased to 400 rpm

- Mixed at this condition for 2 hr and then stopped the striation as well as heat source. The beaker was closed by wrapping with Al foil. It would be better to have glass made cover since the solution evaporates and potentially can react with Al foil and could cause potential contamination.
- The mixture is cooled for 14 hr
- The mixture is carefully poured into a fresh beaker carefully to separate the sediment
- The solution is then filtered using filter paper in a batch of smaller beakers
- The pH meter is first calibrated using standard solution of pH 4, 7, and 10 respectively.
- 5.6 pH is measured after the filtration.
- For good Ni electrodeposition a pH level of 4.0–4.6 is required
- To make it more acidic, Boric acid was added in steps (4+10+20+20+20 gm) with 50 mL of wafer in each step
- After final and the step before final the pH level of 4.8 was measured
- In the process the mixture is stirred at 400 rpm, 40 °C for 1 hr
- The mixture is cooled for 5-6 hr
- The solution is then filtered again using standard filter paper and multiple batch of clean smaller beakers
- After filtration the pH level of 4.6 was measured
- The solution was supposed to be sediment or residue free but some sediment could be seen. Despite that fact, the mixture was used for Ni electro deposition and a good deposition was achieved.
- All samples before putting in the mixture were barrel etched in Branson etching tool in Ar/O_2 plasma at 100 W with 120/12(6) sccm of flow for 90 sec.

- Before pouring the sample in the mixture, the sample was wetted by dipping in the DI-water for 10-20 sec. Care was taken so that the metal clip attached with the sample did not get wet.

- After the sample is hanged in the solution, the mixture is set to stir at 70 rpm and temperature was set to 40celsius. It normally took around 30 min to get to the set temperature. The metal clip attached with both sample and Ni bar was carefully managed to not to touch the solution. Also, a small Al foil was wrapped around the clips before attaching to the sample to increase the contact surface area.

- The deposition was done at 10 mA DC current (Gen-2 samples). For Gen-1 samples a 15 mA DC current was used which deposited Ni faster but it seemed for 10 mA took deposition smoother Ni surface was achieved. But this also could be run to run variation.

- During deposition, the solution was mostly covered with a Teflon cover with the openings only to get inserted wires and temperature thermocouple

- Ni was deposited for 1 hr 45 min which resulted in 1.1 µm film measured after the resist removal in the optical profilometer.

VITA

S M Naeemul Islam was born in 1986 in Dhaka, Bangladesh. He is the youngest among his 3 siblings and grew up in a serene place of Bangladesh University of Engineering and University campus in Dhaka. He attended Engineering University Higher Secondary School and Notre Dame College for high school studies. He then transferred to Bangladesh University of Engineering and Technology, where he completed his Bachelor of Science in Electrical and Electronic Engineering in 2009. After graduating, he joined as a lecturer for a short period of time at the American International University of Bangladesh. During this time, he also got enrolled in a part-time Master of Science program in Electrical and Electronic Engineering at Bangladesh University of Engineering and Technology where his research was focused on short channel effect modeling in CMOS logic device. He later, in 2010, joined as a lecturer at the Institute of Information and Communication Technology in Bangladesh University of Engineering and Technology. He finished his graduation in Master of Science in 2012 and the same year he got the opportunity to pursue his Ph.D. at Purdue University, West Lafayette in Indiana. He started his doctoral program in 2012 under the direction of Professor Michael Manfra, focusing on fundamental ν=5/2 fractional quantum hall study in high mobility GaAs/AlGaAs two dimensional electron gas system. In 2015, he began working under the direction of Professor Dallas T. Morisette, developing a novel 4H-SiC tri-gate MOSFET device aimed for low-mid voltage application. In January 2020 Naeem joined Wolfspeed, a Cree company as a research scientist, where he is working on future generation power semiconductor device design and modeling. He will receive his Ph.D. in December 2020.