PRACTICAL AND RELIABLE WIRELESS POWER SUPPLY DESIGN FOR LOW POWER IMPLANTABLE MEDICAL DEVICES

by

Christopher John Quinkert

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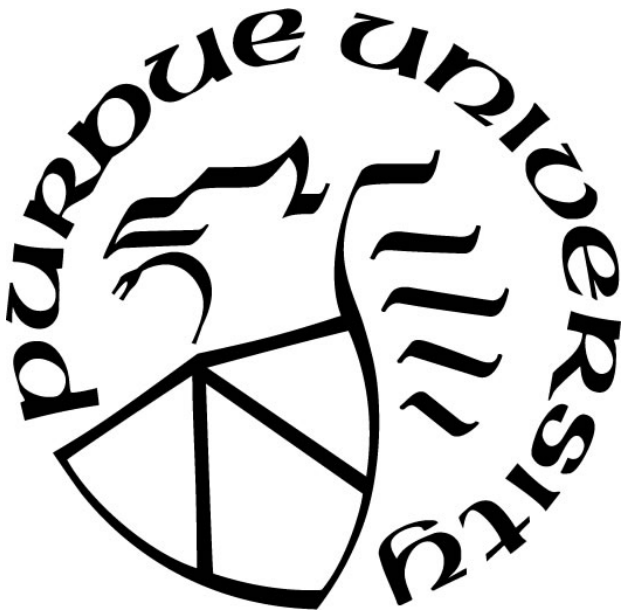

School of Electrical and Computer Engineering

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THE PURDUE UNIVERSITY GRADUATE SCHOOL
STATEMENT OF COMMITTEE APPROVAL

Dr. Pedro Irazoqui, Chair

Department of Electrical and Computer Engineering

Dr. Sunil Bhave

Department of Electrical and Computer Engineering

Dr. Byunghoo Jung

Department of Electrical and Computer Engineering

Dr. Scott Sudhoff

Department of Electrical and Computer Engineering

Approved by:

Dr. Dimitrios Peroulis

I dedicate this work to my family members, whose examples were the motivation for me to push myself to continue school beyond my undergraduate degree.

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LIST OF ACRONYMS

AC	Alternating Current
ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
BGR	Bandgap Reference
CMOS	Complimentary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
EGG	Electrogastrogram
ESR	Equivalent Series Resistance
f_0	Resonant Frequency
FCC	Federal Communications Commission
FPGA	Field-Programmable Gate-Array
HFSS	High Frequency Structure Simulator
High-Q	High Quality Factor
HVS	High Voltage Selector
IC	Integrated Circuit
IM	Impedance Matching
ISM	Industrial, Scientific, and Medical
LC	Inductor and Capacitor
LDO	Low-Dropout
Low-Q	Low Quality Factor
MIM	Metal-Insulator-Metal
MOSFET	Metal Oxide Silicon Field Effect Transistor
NIBB	Non-Inverting Buck-Boost
NIBBC	Non-Inverting Buck-Boost Converter
NMOS	N-Type Metal Oxide Semiconductor
NOC	Non-Overlapping Clock
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation

PLL	Phase Locked Loop
PMIC	Power Management Integrated Circuit
PMOS	P-Type Metal Oxide Semiconductor
POR	Power-On-Reset
PTE	Power Transfer Efficiency
PVT	Process-Voltage-Temperature
PWM	Pulse Width Modulation
RF	Radio Frequency
RLC	Resistor, Inductor, and Capacitor
SAR	Successive-Approximation-Register
SEPIC	Single-Ended Primary-Inductor Converter
VNA	Vector Network Analyzer
WPT	Wireless Power Transfer
ZCD	Zero Current Detector

ABSTRACT

Implantable wireless devices are used to treat a variety of diseases that are not able to be treated with pharmaceuticals or traditional surgery, These implantable devices have use in the treatment of neurological disorders like epilepsy, optical disorders such as glaucoma, or injury related issues such as targeted muscle reinnervation. These devices can rely upon harvesting power from an inductive wireless power source and batteries. Improvements to how well the devices utilize this power directly increase the efficacy of the device operation as well as the device's lifetime, reducing the need for future surgeries or implantations.

I have designed an improvement to cavity resonator based wireless power by designing a dynamic impedance matching implantable power supply, capable of tracking with device motion throughout a changing magnetic field and tracking with changing powering frequencies. This cavity resonator based system presents further challenges practically in the turn-on cycle of the improved device.

I further design a coil-to-coil based wireless power system, capable of dynamically impedance matching a high quality factor coil to optimize power transfer during steady state, while also reducing turn-on transient power required in dynamic systems by utilizing a second low quality factor coil. This second coil has a broadband response and is capable of turning on at lower powers than that of the high quality factor coil. The low quality factor coil powers the circuitry that dynamically matches the impedance of the high quality factor coil, allowing for low power turn on while maintaining high power transfer at all operating frequencies to the implantable device.

Finally, an integrated circuit is designed, fabricated, and tested that is capable of smoothly providing regulated DC power to the implantable device by stepping up from wireless power to a reasonable voltage level or stepping down from a battery to a reasonable voltage level for the device. The chip is fabricated in 0.18um CMOS process and is capable of providing power to the "Bionode" implantable device.

1. INTRODUCTION

Miniature implantable devices in animal models have long been a necessity for researchers looking to conduct long term physiological and behavioral studies in small freely moving animals. Many studies are done using devices that have a transcutaneous link like a headstage or skin cap, but these strategies require tethering the animal to some external wire or cable [1]. In an effort to allow these animals to freely move about their inhabited environment to conduct behavior studies, researchers have turned to wireless implantable devices to this end [1][2]. Within the realm of wireless implantable devices, powering the devices is a serious challenge [3]. Currently, devices tend to be powered by batteries [4-6], bioenergy harvesting [7, 8], or inductive coupling [9, 10]. Batteries by themselves provide stable power to implants, but they have the major issue of limited lifetime, which results in longer animal studies being impossible. Bioenergy harvesting tends to allow for devices with very small power budgets to operate, but devices performing complex functions, such as biopotential recording at high sampling rates and electrical stimulation at higher currents, require much higher continuous powering levels than can typically be provided by energy harvesting [11]. Inductive coupling provides a wireless power transfer (WPT) method that allows for longer lifetime implants with higher powering requirements[12, 13].

1.1 Inductive Wireless Power

Traditionally, implantable devices have been wirelessly powered using a coil-to-coil near field methodology where one coil external to the host animal is excited to create a magnetic field, which is then collected by a coil on the implanted device [12-14]. This approach, however, is very sensitive to the alignment and distance between the two coils, limiting the amount of area and orientation that an animal can be allowed to freely move about [13]. In recent years, large chambers called resonant cavities have been developed to both provide housing for small rodents as well as deliver wireless powering with midfield powering to devices implanted within the animal [14, 15]. These resonant cavities provide a good means of wireless powering for devices with higher power consumption than most implants currently used, while still not exceeding specific absorption rate (SAR) that the FCC standards deem as dangerous to tissue [1, 16, 17].

To optimize WPT within these resonant cavities, the cavity must be excited with an alternating current waveform at its resonant frequency (f_o). The resonant frequency of cavity structures is determined by the shape of the structure and the location and magnetic properties of its contents[13]. As a result, the f_o of a resonant cavity is determined by the size and location of a small animal being housed inside the structure. Due to this difficult complication, both the circuitry driving the cavity and the implanted device must be able to compensate for the changes in f_o if optimal WPT is to be found[18].

1.2 Resonant Cavity Wireless Powering Background

Due to the transient nature of the animal host moving about the wireless powering resonant cavity chamber, the device can be expected to be in an off-state at certain times during operation. This can occur due to low coupling between the cavity and the implant or simply because the animal needs to be removed from the resonant cavity for a period of time. As such, the device must robustly power on as well as operate at the steady state. This complication results in careful consideration being required when designing wireless power harvesting implants. The system's PTE is determined largely by both the impedance match between the resonant cavity and the implant, as well as the quality factor of the impedance matching network's components. Because of this, impedance matching networks must be designed with correctly matched impedance as well as high quality factor. In the static impedance case, this is easily achieved with off-chip ceramic capacitors. However, when trying to dynamically adjust the impedance on the fly to compensate for the changing wireless power environment, other impedance elements must be used.

1.3 Turn-On Transients In Dynamic Impedance Elements

When selecting and implementing these dynamic elements, often times the impedance can be quite different for the element when in the unpowered or off-state of the device compared to the steady state and properly powered impedance. In addition, many of these elements like capacitor banks or miller capacitors have low quality factor when not properly powered or biased. This low quality factor coupled with unknown off-state impedance can create a drastic cavity

input power requirement for turning on the device, which is much higher than the steady state cavity input power requirement to maintain device operation.

1.4 Battery Integration

In some implantable devices, the circuits are powered purely by wireless power, which results in smaller implants but also in more off-time and instability depending on the powering environment. For other implantable devices, they run off of a battery to supply a limited lifetime's worth of power to the device. In the case of the wireless-only devices, the input voltage produced by the wireless power can be quite small at times, requiring a converter to step the voltage up to a usable level for the implant's signal acquisition and stimulation therapy delivery circuits. In the battery case, the nominal voltage of the battery may need a converter to efficiently step the voltage down to a usable level for the implant. In the most rigorous of implants, the power supply should be able to handle having both wireless power as well as battery supplies on the same device. In this scenario, the power supply should be able to efficiently and effectively step up low wireless power voltages when battery power is not available, while also stepping down battery voltages when wireless powering is insufficient. The ability to seamlessly transition between these two modes is critical to effective power supply for implants needing both power sources.

2. WIRELESS POWER DEVLIERY AND IMPLANTABLE DEVICE DESIGN

In this work, I use a resonant cavity, implement algorithms, and build upon the work from [1, 18] to further improve wireless powering in resonant cavities. In an effort to increase PTE for high power budget small implants exceeding 40mW continuously, higher Q-factor cavity resonators are used with narrower frequency response, which results in a need for exciting the cavities as close to their f_o as possible, as well as having a device capable of keeping its impedance and f_o finely tuned to match the cavity at all times. I present a system capable of accounting for both issues. Firstly, the system monitors how the resonant cavity's f_o changes in real time and updates the frequency with which the cavity is being excited to match f_o. Secondly, the implanted device matches its own self resonant frequency to that of the cavity's in real time with a dynamic impedance matching (IM) network. With both of these improvements, higher amounts of power are transferred to the implanted device for more locations in the resonant cavity even as the animal gains weight over time. I present a fully implantable power supply made of discrete off the shelf integrated circuits (ICs) and test it with the dynamic IM system on the bench top powering a device called the Bionode [19], which is capable of recording biopotentials and electrically stimulating the nervous system. Finally, I develop a solution including a rechargeable battery test it *in vivo*.

2.1 Device to Be Powered: The Bionode

The Bionode is a multipurpose implantable device designed and fabricated by various members of the Center for Implantable Devices at Purdue University [19]. This device is comprised of two to three PCBs with off the shelf ICs on board. The Bionode runs off of wireless power and battery power and is capable of the following features: up to four channels of bio-signal acquisition, bio-sensor interfacing, one channel of balanced and biphasic electrical stimulation up to a few milliamperes of current, and two way data communication to provide stimulation and recording parameters to the device or provide data measurements out to the user in real time. After device fabrication, electrodes and sensors are attached to the Bionode, and the entire device is sealed in a mixture of glass, medial grade epoxy, and silicone to provide a

hermetic and non-toxic enclosure for the circuits. This device and packaging are shown in Fig 2.1 [19], and a block diagram of the board's functions are shown in Fig 2.2 [19].

Figure 2.1. A Bionode assembled at the coil and PCB level (left), and a Bionode fully packaged in a hermetically sealed glass case with electrodes, ready for implantation (right) [19].

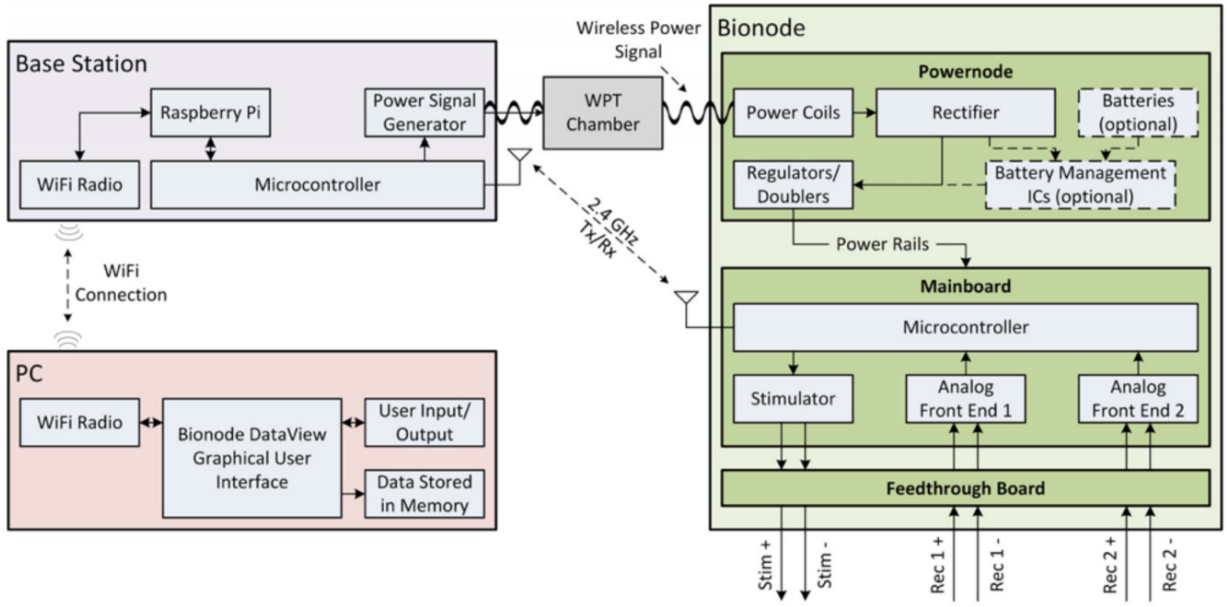


Figure 2.2. This figure depicts the Bionode system from the block level .The user interfaces with a GUI on their PC, which controls the Base Station. The Base Station communicates with two way data to and from the Bionode implant and is able to power the implant. Finally, the Bionode has a two way data link, wireless power link, and interfaces with the body externally.

In particular, I designed and worked with the Bionode's power circuitry and wireless power link, called the "Powernode." This PCB and collection of ICs harvests wireless power from two separate metal coils, pointing in two separate directions, as well as utilizes two batteries to deliver multiple regulated and unregulated supplies for the sensitive circuits that measure biopotentials and stimulate the host animal. The Powernode is designed to provide power up to around 60mW of peak power and an average of 16mW during standard Bionode operation. These power requirements of the Bionode vary with the operation of the device; when

radio transmission and stimulation are required, power needs are around 60mW, while when nothing but measurement is occurring, power consumption is closer to only a few milliwatts as shown in the plot of the power consumption in the average case in Fig 2.3. The main requirements of the Powernode is to provide stable, consistent regulated supplies to the digital circuits and analog measurement circuits, as well as high magnitude unregulated voltage supply rails to the stimulator for extra headroom when stimulating through higher impedances in the animal.

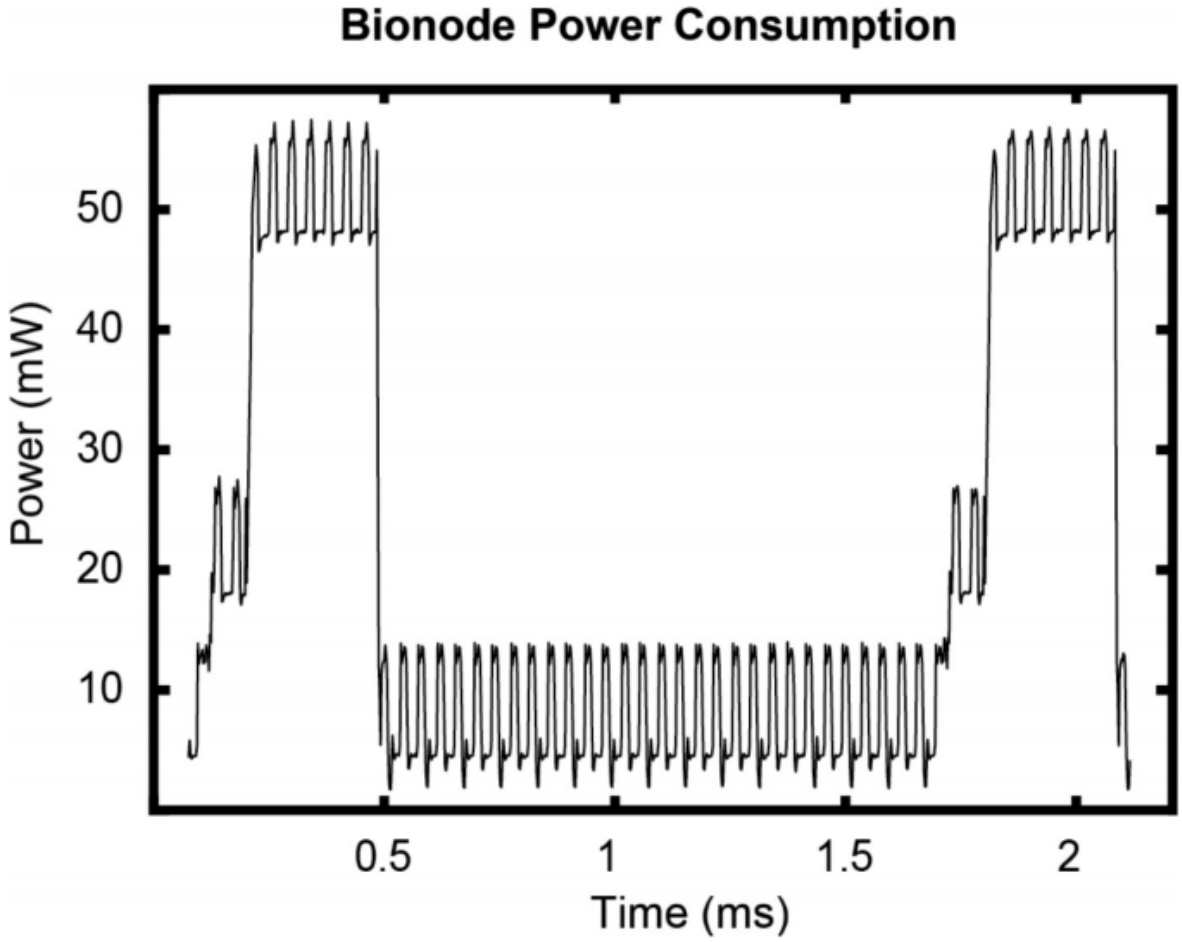


Figure 2.3. This is a standard power consumption curve over time for a Bionode circuit using the radio to send out measured data from the ADC and bio-signal acquisition circuits.

2.2 Powernode: Static Impedance Design

The Powernode's design is centered around using both the battery's power and the wireless power to provide supplies to the Bionode. The two coils each have their own

impedance matching circuit to provide maximal power transfer from the resonant cavity or transmitting powering coil to the receive coils on the Powernode. These two l-matching networks use two static capacitors that are initially predicted based on bandpass filter theory [15, 18, 20], and the capacitor values are manually tweaked for each device and animal to specifically tune the operating frequency and impedance of the implantable device to maximize power transfer efficiency. Each coil additionally has its own full wave rectifier doubler that converts the AC power received by the coils into a DC rectifier voltage to deliver power to the regulators and converters. The need for separate rectifiers is due to the two coils needing to be as electrically isolated and separate from each other as possible. If both coils shared the same rectifier, the resonant frequencies and impedances of the two coils are much harder to tune to a specific frequcny, and the two frequencies of each coil will be pushed further a part from each other and not able to be as close in frequency, resulting in a loss of efficiency at the desired operating frequency of the transmitting cavity or coil. These rectifiers produce a DC voltage drop across the full rectifier, and in this application, ground is chosen to be the midpoint of the rectifier, resulting in a positive and negative rectified voltage with respect to the rectifier's midpoint.

After rectification, the DC power available from the wireless power is able to be down-regulated to multiple +1.8V and +0.9V supplies for the microcontroller, analog recording circuits, and low voltage digital control circuits on the Bionode. In addition to the +1.8V LDOs, the negative rectified voltage rail is down-regulated to -0.9V by an LDO for the same circuits. Finally, the stimulator requires a high negative and positive supply in the range of -5V to 10V and +5V to 10V, respectively. This is achieved with switched capacitor doubler ICs. To prevent the rectified voltages from having too much AC noise from the wireless power, additional low pass filters are added into the circuit. Finally, the rectifier's negative and positive supplies are clamped to -4.2V and +4.2V to protect circuits downstream from overvoltage effects and damge. The batteries are attached in parallel with the negative and positive rectified voltage, and are litium ion batteries with a nominal voltage of 3.6V and maximum voltage of 4.2V. These two batteries may charge or discharge depending on the state of operation. Should the wireless power be doing poorly and not providing enough charge, the batteries will discharge and power the Bionode. Conversely, should the wireless power be providing excess power for the Bionode, the batteries will recharge from excess power provided by the coils. These charging and discharging

cycles are managed by two off the shelf PMICs. These functions and general circuit diagram are presented below in Fig 2.4.

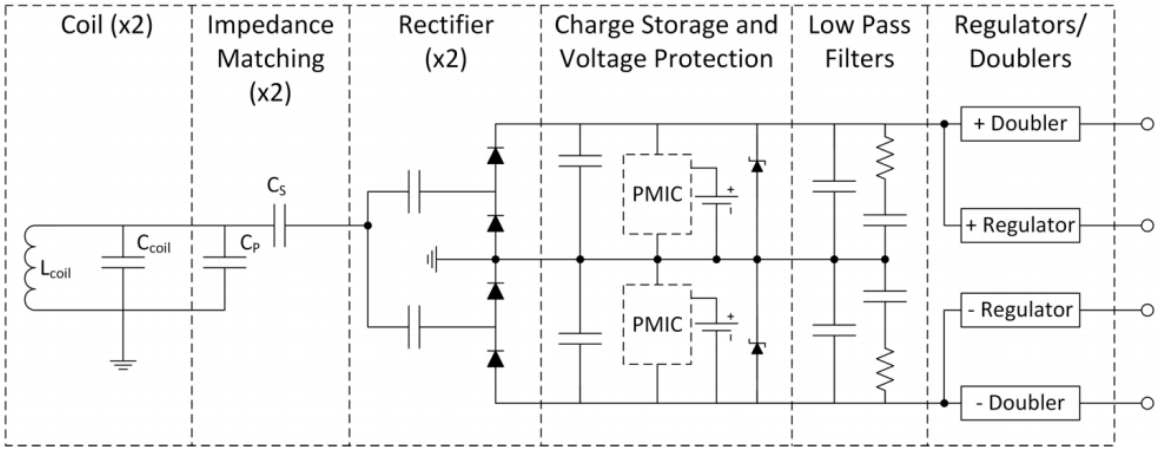
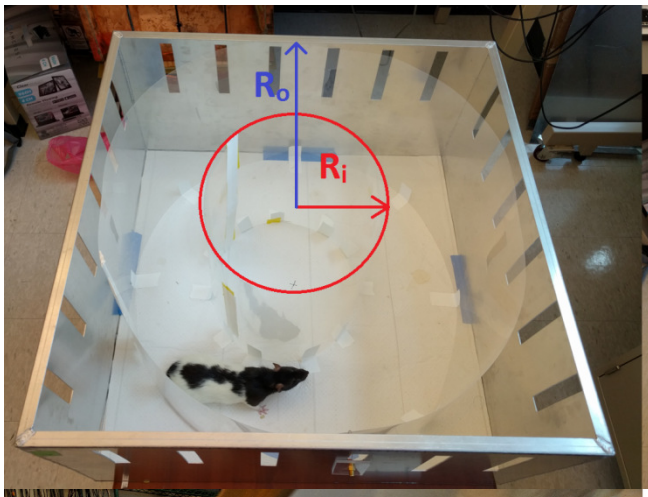


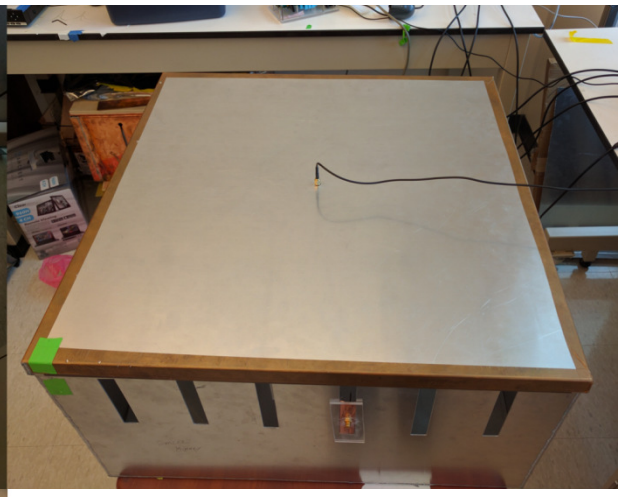
Figure 2.4. The schematic of the static Powernode power supplies used to power the Bionode implant.

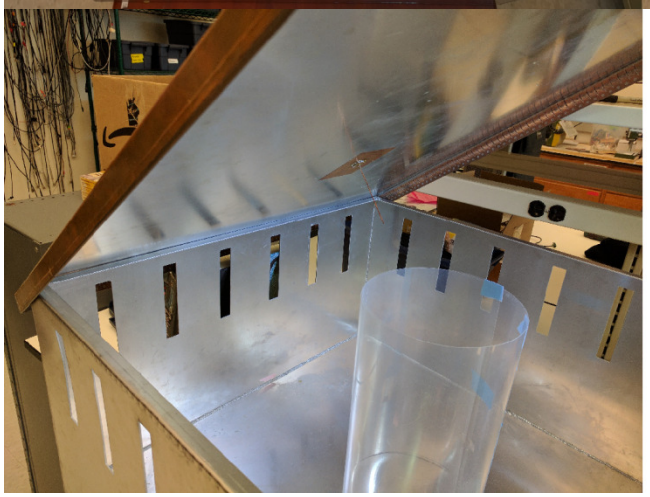
2.3 Resonant Cavity Dynamic Impedance Matching

Because of the evolution of the Bionode technology over recent years for various grants and applications, the power demands of the device have slowly increased to higher levels. To accommodate these increased power demands, the wireless powering of the device must be improved to provide higher PTE at the same input power levels to the transmitting device. In the following section, I present background on the operation of the resonant cavity, static impedance matching of the Powernode, and design an improved dynamic impedance matching system for the implantable Bionode powered by the resonant cavity only.

Fig. 2.5 shows an aluminum cavity resonator. This hollow structure simultaneously provides a housing structure for small rodents, such as rats or mice, to inhabit and provides wireless powering for implanted devices. The TM_{110} mode is excited with a probe in the center of the cavity with an AC signal to generate a circulating magnetic field [1]. From simulations, the fields mostly circulate around the center of the cavity with field strengths that in generally increase with increasing radius from the center -excluding the corners of the rectangle and the exact center of the cavity. In the corners and center of the cavity, the field strength is much weaker, and as a result, we add plastic barriers to prevent the animal from entering these low field strength regions [1].







RESONANT CAVITY DIMENSIONS

Dimension	Value
Width	70.00 cm
Length	70.00 cm
Height	30.50 cm
Outer Radius R_o	34.75 cm
Inner Radius R_i	6.75 cm

Figure 2.5. The resonant cavity used to power implantable devices. An animal is housed in the enclosure and prevented from traversing low field strength portions of the cavity (top left). The cavity is excited externally (top right) by a probe in the center of the cavity (bottom left), and has specific dimensions that determine its resonant frequency (bottom right).

As shown in previous works, the resonant frequency of the cavity is a function of the dimensions of the structure [15]. Due to the size of our cavity, f_o is approximately 347.8 MHz when nothing is inside of the cavity, and we select the probe length for minimal loading. Fig. 2.6 demonstrates the power reflection measurement for this structure. We move a rat phantom, capable of mimicking the electrical properties of a rat weighing 280-300g, to various radii in the cavity. The frequency at which minimum reflection occurs indicates the resonant frequency for that loading condition. This frequency is much lower than the frequencies in the GHz range where wireless powering is less efficient for implantable devices due to higher tissue absorption of RF energy at high frequencies [21]. In this work only the TM_{110} mode is harvested. In various

previous experiments, this mode was deemed to be the optimal excitation mode for implants of this size with the constraints placed on coil placement in the device. Other magnetic field modes can be generated with differing flux directions in resonant cavities, however, due to the requirements for animal housing, issues with interference between the two modes as well as harvesting of the two modes, and added required complexity of multiple well-spaced coils and associated electrical circuits, only the one mode is considered in this work.

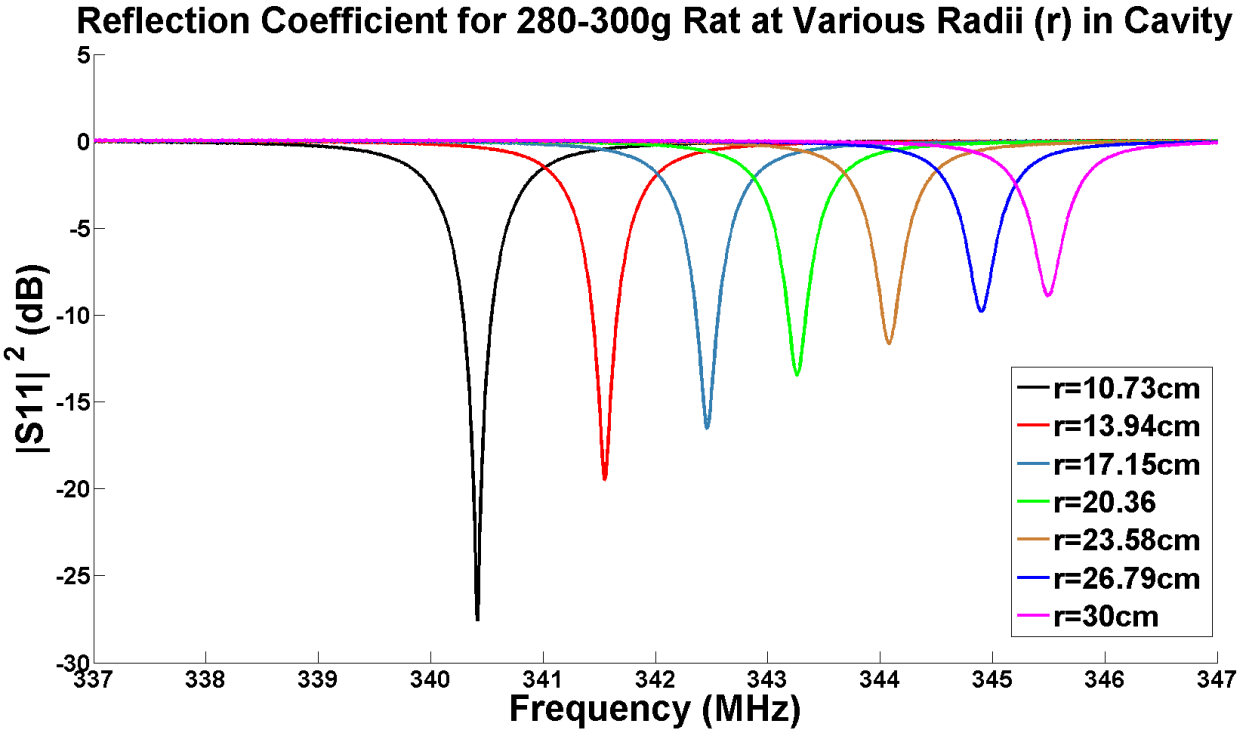


Figure 2.6. Plot of reflection $|S_{11}|^2$ versus frequency measured for the cavity with a vector network analyzer. A rat "phantom" mimicking the electrical properties of a rat sized at 280-300g is moved to various radii (r) in the cavity. The value f_o can be determined by the frequency at which minimum reflection occurs. It is shown that f_o decreases as an animal moves inward.

In Fig. 2.7, we model the cavity resonator as a parallel RLC with a 50 ohm AC signal source. The probe is modeled as a lumped capacitor, and the capacitive coupling between the probe and the resonator is a pi network. The pi network capacitances vary with the length of the copper probe used [16]. When an adding an animal to the outermost radius of the cavity resonator, the tissue acts as a lossy dielectric [15], and the resonant frequency of the cavity will decrease. As the animal moves further into the cavity to smaller radii, the resonant frequency further decreases due to the presence of stronger electric fields towards the center of the cavity.

This is a function of the animal's weight; thus, as an animal gains weight, this effect becomes more dramatic. We model the implantable as a parallel RLC circuit as well. Shown in Fig. 2.8, we include an IM circuit in the form of a J-inverter to maximize power transfer efficiency [13].

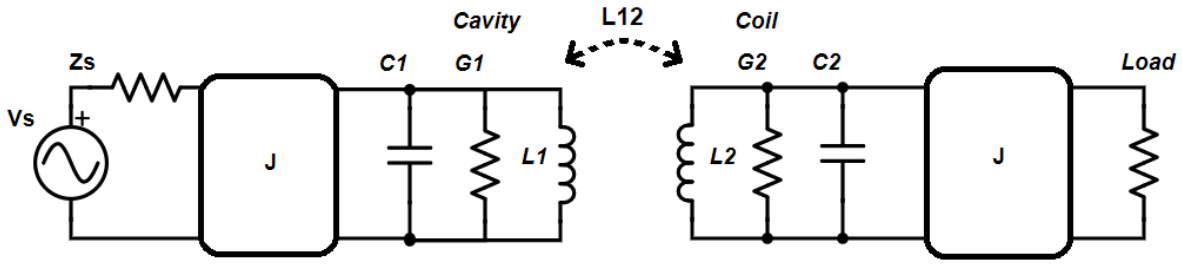


Figure 2.7. Circuit model of wireless power transfer as inductive coupling between two RLC circuits. The transmitting circuitry on the left includes an AC source and probe capacitance with impedance matching network in the form of a J-inverter. The receive circuitry on the right includes the RLC coil with impedance matching J-inverter and the connected load, which includes power management circuitry and the implantable device itself.

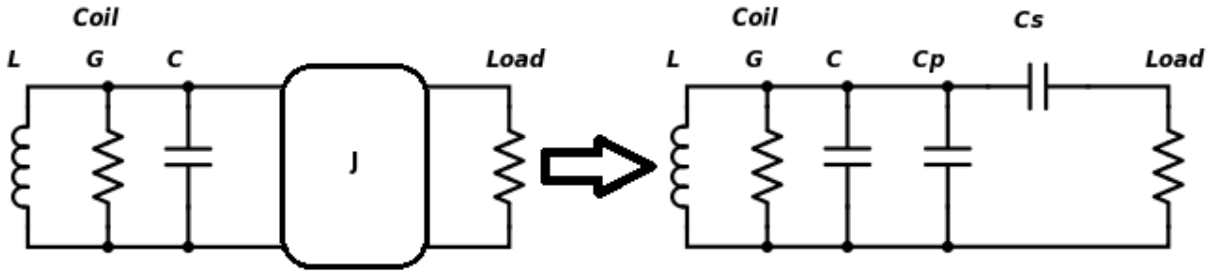


Figure 2.8. Realization of J-inverter matching circuitry as a half pi capacitor network to match the coil to the load impedance.

For a given frequency, we determine values for the IM network's two capacitors C_s and C_p based on the algorithm presented in [18]. In previous work [13], the frequency selected is either the resonant frequency of the cavity when the animal is either at the outermost region or when the animal is halfway between the outermost and innermost allowable radii.

However, the optimal PTE case exists when the animal is in this location and an AC signal at this specific frequency excites the cavity. As the animal moves and the resonant frequency of the cavity changes, the PTE decreases as both the cavity and receive device are not operated at the optimal frequency. To solve this issue of f_o changing and resulting in sub-optimal conditions, we need two solutions. We require a "frequency tracking" driving circuitry to update

the frequency exciting the cavity to match f_o and a "dynamically impedance matching" receive device on the implant to update the receive device's resonant frequency to keep up with f_o. When implementing both of these improvements, optimal PTE exists in the system.

2.4 Resonant Cavity Frequency Tracking

To effectively keep up with the animal's motion in the cavity and have the driving frequency quickly track and update to the changing resonant frequency of the cavity, we use a driving system called the "basestation", fabricated on a four-layer PCB with discrete components capable of this task. The basestation and frequency tracking work described herein is the work of Grant Wang but is included for completeness on the discussion of the full system in the wake of any publication for citation.

Fig. 2.9 presents a block diagram of the functionality of the basestation. A separate microcontroller (Nordic Semiconductor, nRF51822) sets an ASK/FSK transmitter, capable of generating low power signals in the range of 280 MHz and 450 MHz (Maxim Integrated, MAX7060), to various frequencies. A low noise RF pre-amplifier (Analog Devices, HMC636ST89)amplifies this output signal, and then an output RF power amplifier (RFMD, RFPA3800) amplifies the signal again with high gain. Next, a dual junction circulator passes the signal to both protect the power amplifier as well as couple reflected power to a third port. An RF log detector (Linear Technology, LT5537) converts this reflected RF power into a DC output as a function of the RF amplitude, and the microcontroller's on-chip analog-to-digital converter then measures this DC output.

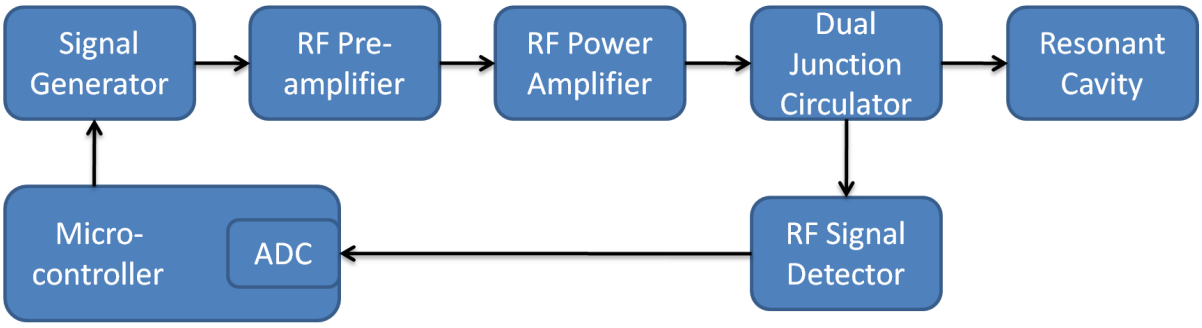


Figure 2.9. Block diagram of the functionality of the signal generation circuit on the basestation. A signal generator creates a waveform that is filtered and amplified before feeding the cavity. The reflected power is measured and a microcontroller updates the frequency of the signal generated as a result.

The algorithm implemented by the basestation's microcontroller is straightforward and presented in Fig 2.10; the user selects a starting frequency to program the signal generating circuitry with to start. The ADC then samples the reflected power and increases the driving frequency. The system samples the reflected power once again. If the reflected power decreased, this means that more of the power is delivered to the cavity, which indicates that the driving frequency is closer to the resonant frequency then previously. As a result, the basestation continues to increase the frequency until it measures an increase in reflected power, at which point the basestation will start to decrease the frequency. This feedback loop repeats approximately 20 times per second, which is quick enough to keep up with the normal motion of rodent. Fig. 2.6 demonstrates the frequency changes seen for various locations of an average sized rat (280-300g) at various radii in the cavity where the expected frequency change from the animal results in frequencies between about 340 and 346 MHz.

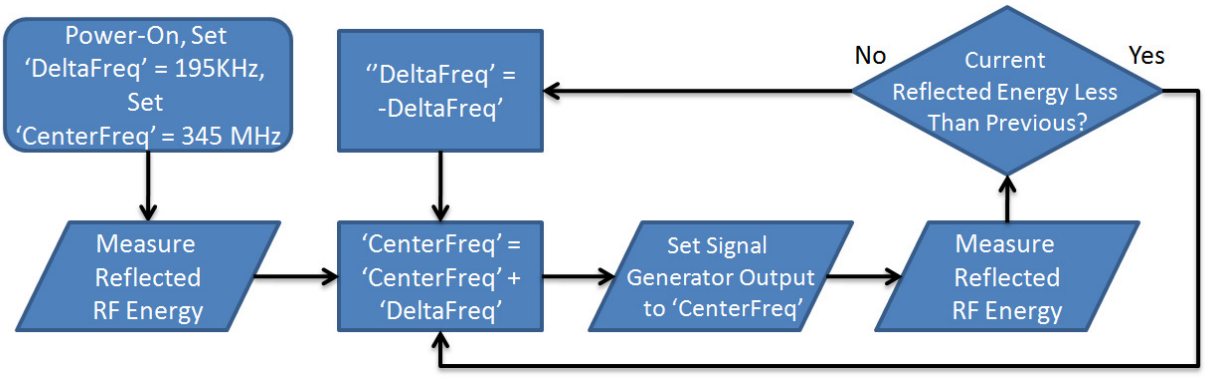


Figure 2.10. The searching and tracking algorithm performed by the base station to find the best frequency to drive the cavity resonator with.

2.5 Dynamic Impedance Matching Circuits and Elements

To account for changes in the frequency the cavity is driven at, the receive device's C_s and C_p ideally need updating with each frequency change. However, for the frequency ranges used and impedance of the implant used in this study, changes in C_p are a sufficient first step in helping increase PTE. Thus, as the frequency decreases, C_p must increase to compensate, and as the frequency increases, C_p must decrease.

Multiple options exist for dynamically varying capacitances, including varactors, miller capacitors, and multiplexed discrete capacitor tanks. Varactors require precise bias voltages to be established utilizing DACs, inductors, and additional diodes, which consumes additional area yet

is a potential solution. Miller capacitors using discrete silicon MOSFETs have speed limits lower than this frequency range and are not effective for this application as a result. Due to the presented constraints, we select a 5-bit multiplexed discrete capacitor bank (Peregrine Semiconductor, PE64102) to realize this circuit discretely. Fig. 2.11 shows a modified circuit of the receive coil and IM. The C_s and C_p discrete static capacitors are still present, but we add a series combination of the capacitor bank C_{pv} and static capacitor C_{pr} as an additional shunt element. The capacitor bank changes its value based on digital control signals from a microcontroller, while C_t decrease the variable capacitance range to the necessary values and desired fine step size.

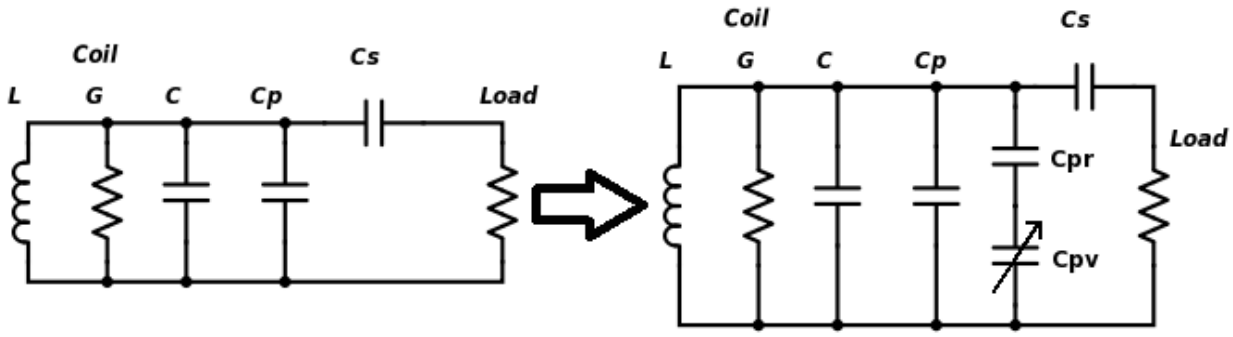


Figure 2.11. Transformation of static J-inverter impedance matching to include a parallel changing capacitive element to track with changes in f_o. The parallel capacitive network includes the capacitor bank as well as series capacitor to limit the capacitance seen to reduce step size and allow for finer tuning.

Fig. 2.12 shows the schematic of the updated Powernode. The Powernode is a circuit realized on a four-layer PCB and populated with discrete components. This circuit connects a coil and its respective tuning network and converts coupled RF energy into positive and negative DC supplies with respect to a center ground voltage using a full wave rectifier. The rectifier is voltage doubling and utilizes small forward drop, low reverse recovery time Schottky diodes to increase efficiency and reduce reverse leakage when switching in the 340 - 350 MHz range. In addition, each of the voltage rails generated by the rectifier has charge storage capacitors and notch filters with a center frequency of 345 MHz to reduce any of the RF signal from the coil that leaks through onto the DC lines and provide stable input voltages to regulators implemented from these rails. An 11Volt Zener diode prevents overvoltage damage to the later circuitry. The

two rectified DC output voltages are then down regulated to stable, accurate supplies for powering a microcontroller with on-chip ADC, capacitor bank, and Bionode device. We achieve this with positive 1.8V regulator and a negative 0.9V regulator.

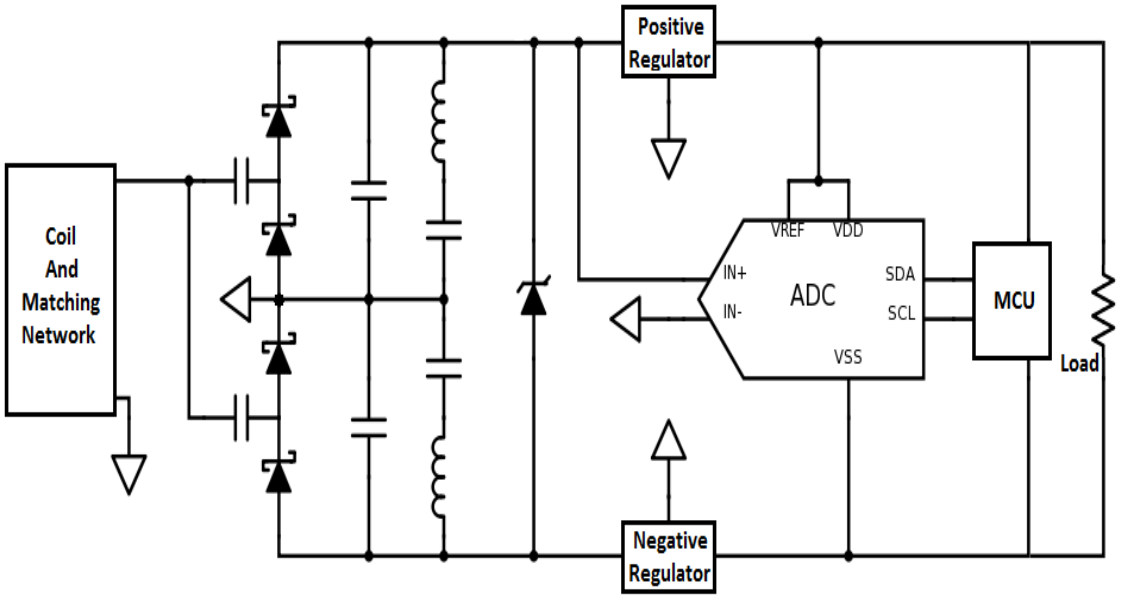
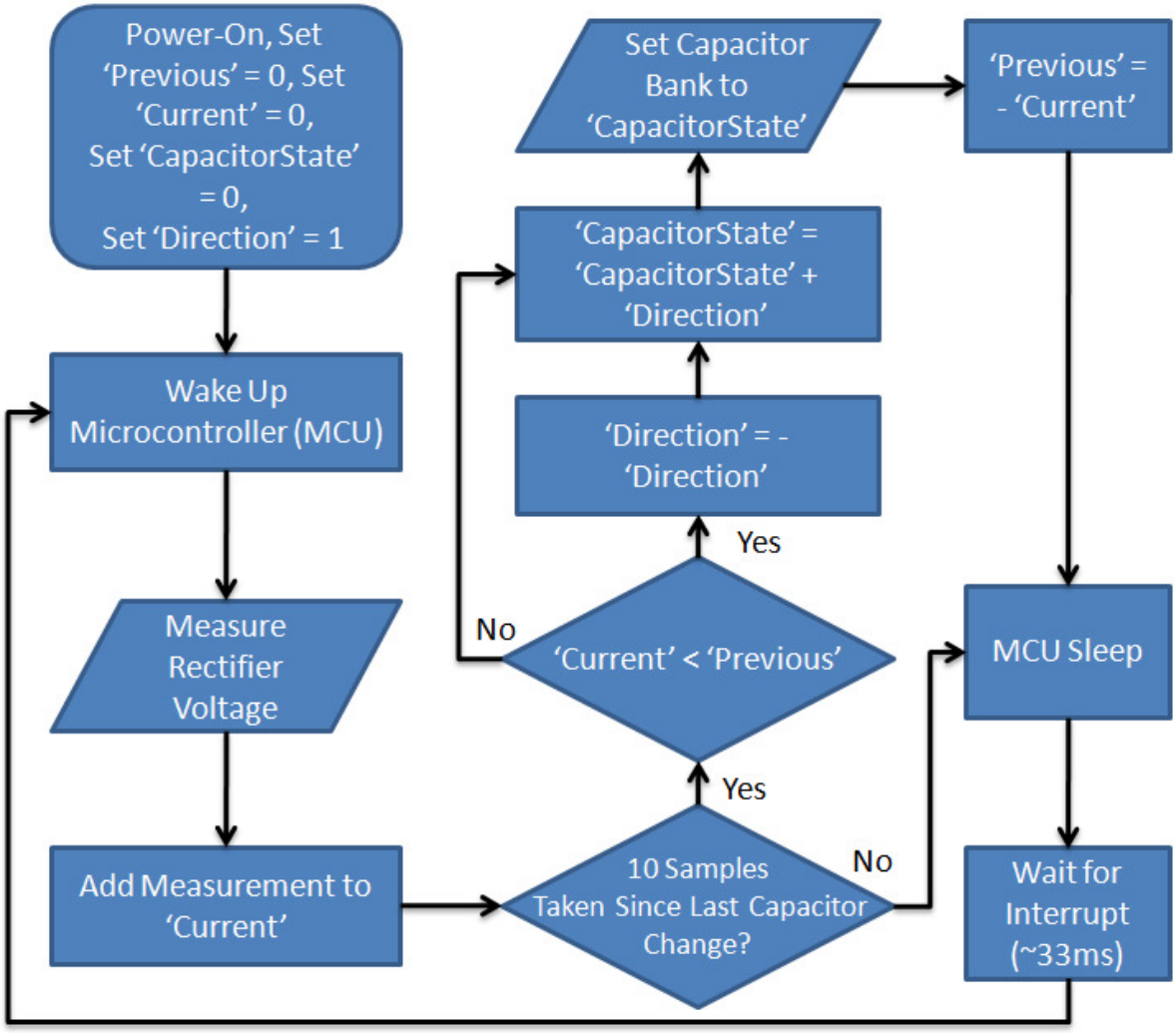


Figure 2.12. Circuit model of the Powernode for power management. The output of the coil and matching is rectified with a full wave doubler, filtered, clamped, and down regulated. A microcontroller with ADC samples the rectified voltage and adjusts the capacitor bank in real time to track f_o.

The microcontroller implements the dynamic IM algorithm as well as manages power consumption from the Bionode device powered by the Powernode. Most times, the microcontroller (MCU) is asleep and drawing little power. Every 33 milliseconds, it wakes up for approximately 5 milliseconds to perform the dynamic IM algorithm. For nine wake-up cycles, the MCU samples the positive rectifier voltage, stores the value, and sleeps. On the tenth wake-up cycle, the MCU samples again and then based on previous capacitance values selected, current 10-cycle voltage average, and previous 10-cycle voltage average, it decides whether the coil's parallel capacitance should increase, decrease, or remain unchanged. This results in the capacitance being able to change up to 3 times a second, which is quick enough to keep up with the motion of a small rodent in the resonant cavity being used. The averaging period of 10 cycles

is due to the dynamic nature of the power consumption of the Bionode device. During radio transmissions (every 1.6 to 40 milliseconds depending on sampling rate), the Bionode consumes up to twenty times the baseline power consumption when not transmitting data. As a result, the rectifier voltage instantaneously decreases some. In an effort to reduce errors in IM changes, sampling the rectifier over 330 milliseconds and averaging the result successfully represses quick changes in rectifier voltage as the sampling frequency and the transmission frequency differ. We keep the algorithm simple intentionally due to intermittent power loss of the implant. During power loss, all previous variables and information are lost. This is a result of the inability to write to flash memory when implanted, which is a direct result of the possibility of corrupting the flash memory and causing algorithm failure if power is lost during a write operation to the flash memory. The algorithm used in this application is diagrammed below in Fig 2.13.

Figure 2.13. The algorithm implemented by the Powernode microcontroller. The device wakes up for small increments to save power and measure the rectified voltage ten times. Next, the capacitance of the bank is increased. Ten more measurements are taken. If the rectified voltage is lower, the capacitance increment direction is flipped and the capacitance is changed in this direction. If the voltage is higher, the direction remains the same and the capacitance is changed in the same direction. After each set of operations, the device is put to sleep to save power.



The Powernode has a single coil for simplicity of initial measurements and ease of construction. The coil selected for this device, dubbed a "two-axis coil", is a rectangular coil with a 90-degree bend placed halfway along its longer dimension as shown in Fig. 2.14. This coil can capture large quantities of flux in both the directions marked "A" and "B" in the figure. As a result, the device should be implanted such that one of the "B" directions is parallel with the animal's spine, and the other "B" direction is parallel to the animal's sagittal plane. The animals tend to habit the cavity such that either their spine is parallel or perpendicular to the flux in the

cavity based on previous work done with chronic implantations in these cavities with aforementioned "keep-out-zones".

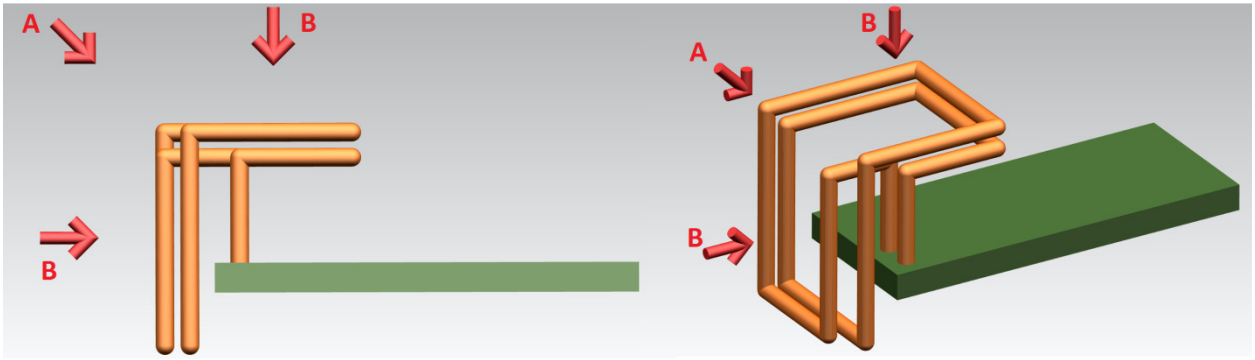


Figure 2.14. A model of the Powernode board and two-axis coil. The coil receives flux in large quantities in the marked directions, any direction between, or any direction opposite the aforementioned directions.

We fabricate a two-axis coil with 22 AWG magnet wire, and measure its electrical properties at 345 MHz with a 1-port VNA measurement. Then we do the same measurement for the cavity resonator. Then, the algorithm developed in [18]using the measured values determine the approximate value of the IM network. Using the IM values, we populate the tuning network on the Powernode with 0201 capacitors (Johanson Technology) -without populating the capacitor bank- and the resonant frequency is measured with the VNA.

Based on the previous measurements with loading the cavity with a rat phantom similar to a young rat weighing around 260g at the outermost radius of the cavity and with a rat phantom similar to an old rat weighing around 400g at the innermost allowable radius of the cavity, we determine the minimum and maximum resonant frequencies that the device must match to be 340 MHz and 346 MHz. After manually changing the C_p value and measuring the resonant frequency for each value, the minimum and maximum C_p values determined are 1.8 and 2.0pF. Because the capacitance range of the capacitor bank is 1.88pF to 14pF, we place a discrete 0201 0.8 pF in series with the capacitance bank to set the dynamically tunable element to range between approximately 0.56 pF and 0.75 pF. When placed in parallel with a 1.2 pF discrete capacitor, the total parallel capacitance varies between 1.76 pF and 1.95 pF, which are close to the necessary values for the desired frequency range.

2.6 Experimental Results

The purpose of the Powernode is to provide stable and adequate power to the Bionode as previously discussed. All of the on-board features come at the cost of power consumptions that vary based on the sampling rate of the device's data acquisition circuitry. The device being used specifically in this wireless power improvement study consumes an average of approximately of 8.1mWand 48.6mW for common total sampling rates of 1 kilosample per second (kSa) and 25kSa, respectively. Fig. 2.15 is an example of the Bionode system and basestation system used in this particular work.

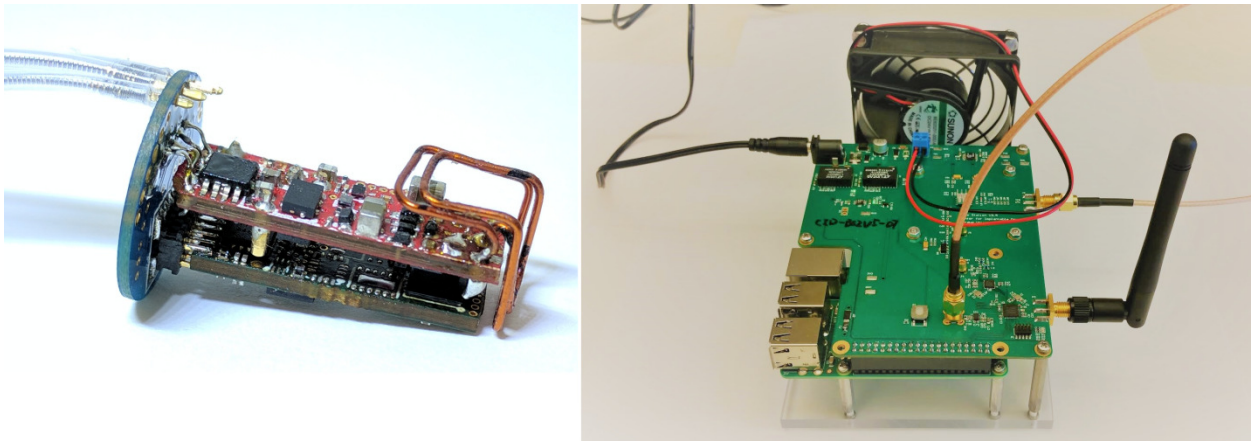


Figure 2.15. Picture of a full implantable device on the left and basestation on the right. The Powernode is the red board, and a two-axis coil is attached. The basestation has an attached antenna for data telemetry, an SMA connection for reflected power measurement, and an SMA connection to power the cavity with the generated waveform.

We test the complete system on the bench-top using a resonant cavity described above and a rat "phantom" - a combination of materials including TX-151 used to mimic magnetic properties of tissue - with properties similar to a 280-300g rat. We then place a full implantable device including Powernode, Bionode, and electrodes in the same orientation at various radii (with the rat phantom moving as well) in the cavity. The specific orientation is such that the flux lines in the cavity enter the coil in direction "A" shown in Fig. 2.14. An SMA cable then connects the basestation to the cavity. We measure the minimum power on the Basestation inputted to the cavity required to turn on the Bionode device for each of these locations for various cases.

The first test case uses the device without either the frequency tracking or dynamic IM and manually tuning the device to the average frequency (when the animal is at the middle allowable radius) of the cavity while also driving the cavity at that average frequency only for various locations of the phantom and device. This case shows the power transfer that can be expected from systems employing wireless power in a high-Q factor resonant cavity without any of the improvements presented in this paper. Next, we test the case where frequency tracking is employed for an implant that has been manually tuned to the frequency when the animal is at the largest radius in the cavity but does not have dynamic matching. Finally, we show the case where the system implements both frequency tracking and dynamic IM. Fig. 2.16 and Fig. 2.17 present the minimum input power to the cavity to reliably use the Bionode system at various radii in the cavity at two separate sampling rates. Due to saturation and non-linear effects from the power amplifier on the basestation when the outputted power gets in the range of 3.9 to 4 Watts, we mark all measurements in that range as 4 Watts in Fig. 2.16. and Fig. 2.17. If there is no mark for a measurement and given radii, it means that the device cannot operate with 4 Watts inputted into the cavity.

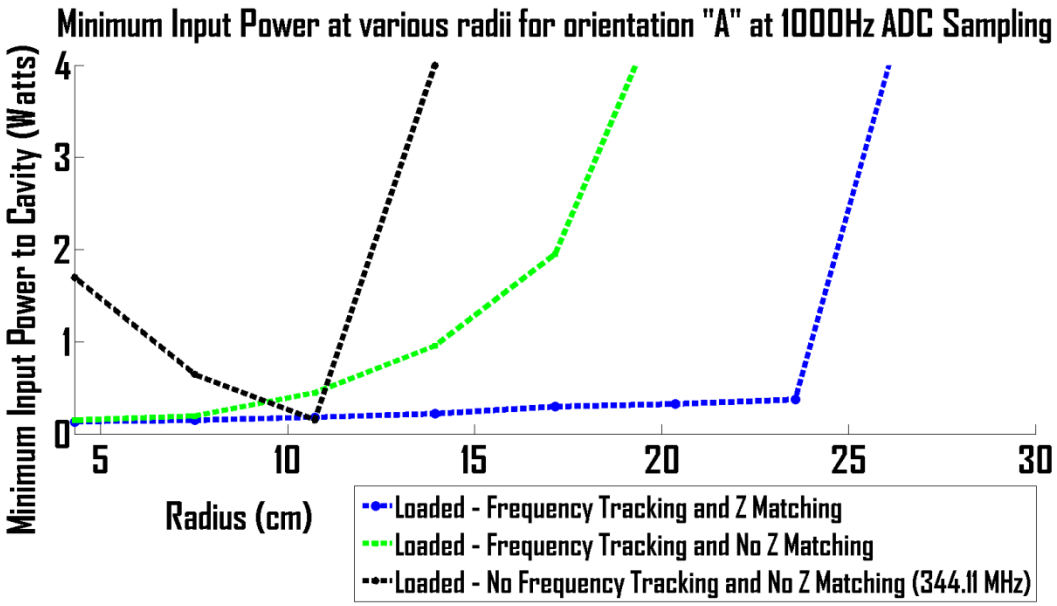


Figure 2.16. Plot of the minimum power to the cavity required to operate an implant that consumes 8.1 mW on average (not including AC-DC conversion loss) at various radii in the cavity in coil orientation “A”. The cases shown include with no improvements to the wireless powering, with just frequency tracking, and with both frequency tracking and dynamic IM (“Z Matching”).

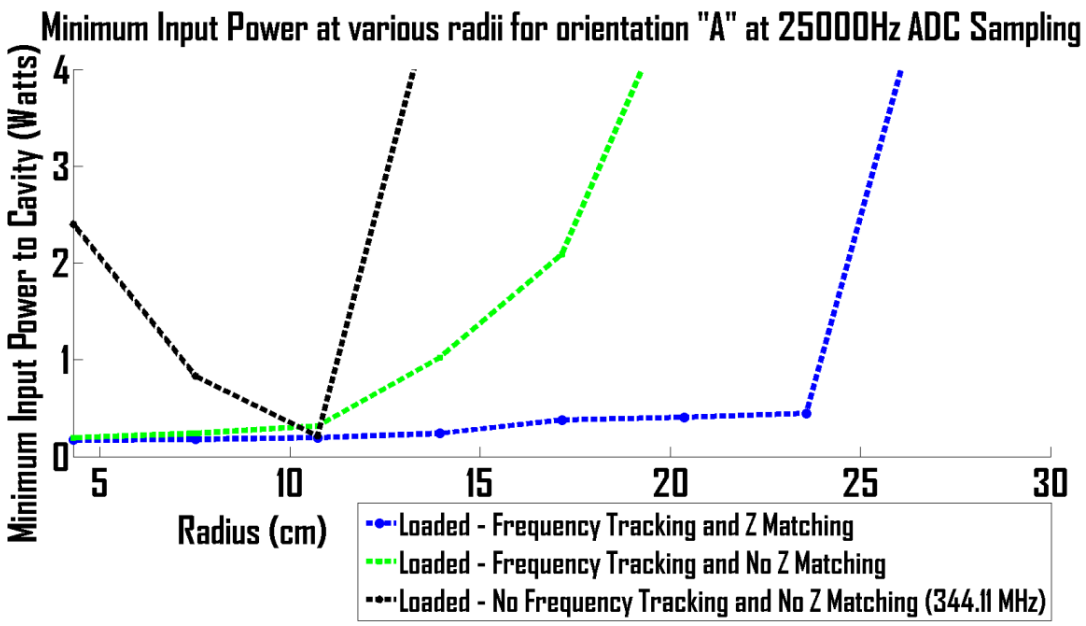


Figure 2.17. Plot of the minimum power to the cavity required to operate an implant that consumes 48.6 mW on average (not including AC-DC conversion loss) at various radii in the cavity in coil orientation "A". The cases shown include with no improvements to the wireless powering, with just frequency tracking, and with both frequency tracking and dynamic IM ("Z Matching").

Based on these measurements, for the orientation case of "A" and lowest power consumption case, the device with only frequency tracking shows modest improvements in both number of locations that the device could be operated in as well as the power transfer efficiency in nearly all locations. When combining the frequency tracking and dynamic IM, we see a drastic increase in number of locations the device can operated at as well as significant decrease in the amount of input power required in nearly all locations when adding in dynamic IM and frequency tracking. At the highest power consumption case, the improvements are even more apparent with the device with both dynamic IM and frequency tracking.

In addition to the minimum input power measurements taken, we directly measure S_{21} and calculate of PTE using a 2-port measurement with a VNA connecting to both the cavity and the output of the impedance matching network (the rest of the Powernode after the rectifier to the regulators was powered with a DC supply separately) for the same locations in the cavity. From

the S_{21} measurements from the VNA, we directly calculate the PTE percentage. The plots in Fig. 2.18 demonstrate the results of these measurements. Once again, we see improvements for all but the points where the frequency corresponds to where the device is tuned to statically. By taking averaging the difference between PTE for the frequency tracking and dynamic IM and the PTE for the better of the two measurements with no improvements, there is an increase of 10.38% PTE is found on average with the dynamic IM and frequency tracking.

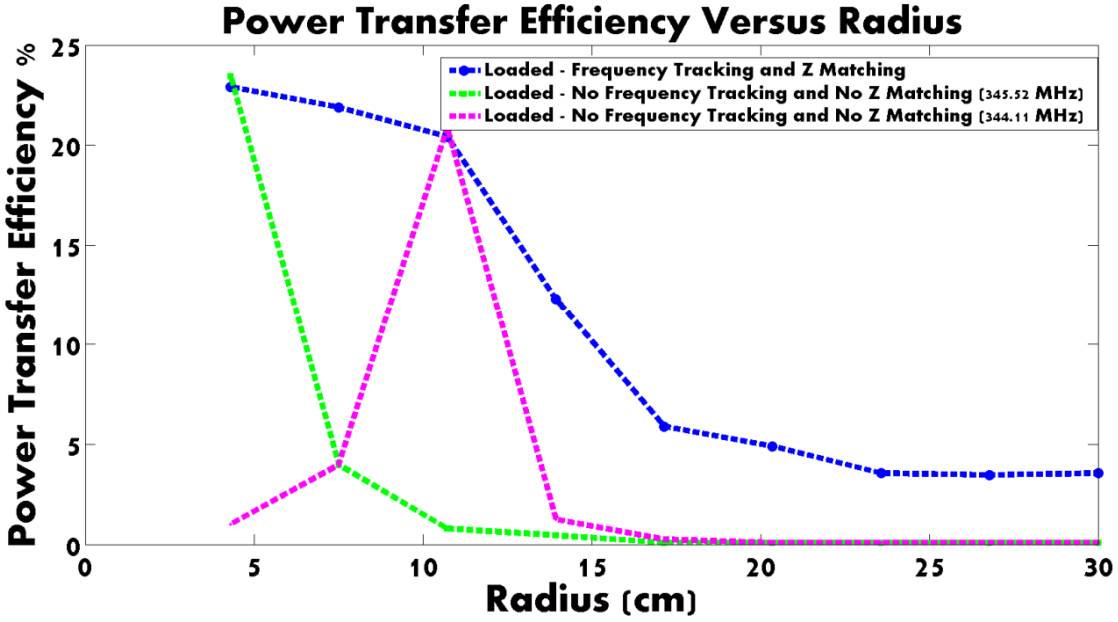


Figure 2.18. Plot of power transfer efficiency percentage for an implant positioned at various radii in coil orientation "A". The cases shown include when the device has both frequency tracking and dynamic IM ("Z Matching"), no improvements where the implant is statically tuned to 345.52 MHz, and no improvements where the implant is statically tuned to 344.11 MHz.

By simulating this High-Q cavity resonator in Ansys High Frequency Structure Simulator (HFSS), simulations of the magnetic field strength at each location in the cavity resonantor show that the the height at which the implant sits largely does not affect the field strength or PTE. Taking this planar spatial field strength data as well as the measured data from this work, we curve fit the two data sets. The PTE is non-linearly correlated to the field strength under the following reasonable assumptions: the impedance of the receive device is matched well to the implantable circuitry due to the dynamic IM, the cavity is being driven at f_o due to the frequency tracking, and the small rodent has a negligible effect on the field strength. After curve fitting, we extrapolate the measured PTE data points to the entire planar area (ignoring the height) of the

cavity. As demonstrated in Fig. 2.19, the presented improvements to this high-Q cavity resonator based system demonstrate drastic improvements in PTE throughout the entire area when compared to lower-Q cavity resonator work without the dynamic IM or frequency tracking [1]. A comparison between a low-Q cavity without dynamic IM and a high-Q cavity with dynamic IM is critical due to the necessity of having dynamic IM in the high-Q cavity for reasonable operation to be expected at all. From the HFSS simulation data, one clear outlier data point out of the 60 by 60 point grid generated for Fig. 2.19 is removed and instead replaced with a spatial average of its four immediately surrounding points The point is located approximately at x of 4 and y of 32.The data in each of the plots uses measured data where magnetic flux is normal to the coil in the optimal position (orientation "A"), but the coil used in the lower-Q cavity is a traditional "one-axis coil" of similar flux-capturing area [1].

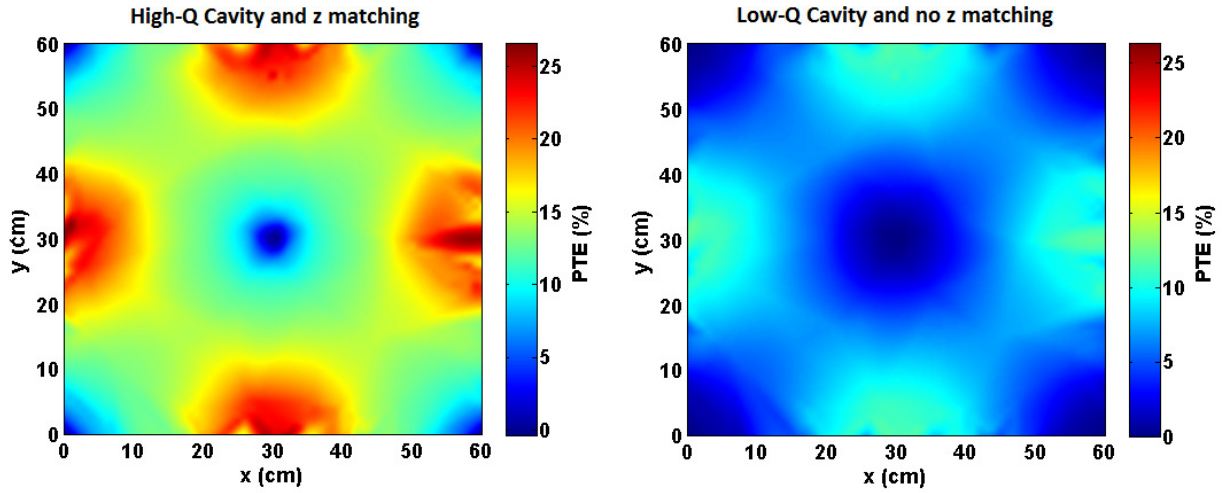


Figure 2.19. Plot of PTE for various spatial locations in the high-Q resonator using dynamic IM and frequency tracking created with curve fitting data to HFSS field strength simulation data (left). Plot of PTE for various spatial locations in a lower-Q resonator from previous work without dynamic IM [1].Both plots show data where flux is normal to the receive coil.

To verify functionality of the design, the device was implanted in a 280g rat. Because the two flux capturing coils do not account for the third axis which power may be received when the rat rears up on its hind legs, a rechargeable lithium ion battery was included similar to the Powernode in Fig 2.15 above. After implantation, the animal was placed in the resonant cavity during two separate recording sessions. In the first session of 6.4 hours, the cavity was driven with 4 Watts input with the frequency tracking and impedance matching active. The device's

battery was capable of delivering about 2 hours of power when not supplemented with any additional wireless power. The powering fidelity -calculated as the percentage of the total time that the device was on to the total amount of time the cavity was powered- during the session was 99.58%. For the second recording session of 2.77 hours, the experiment began with the batteries completely discharged at the beginning. The second session's power fidelity was measured to be 89.3% over 2.77 hours.

2.7 Summary

In this work, I designed, built, and tested a complete system capable of providing improved power transfer efficiency for implantable devices with high power consumption needs in resonant cavities with higher Q factors. The system presented can compensate for the changing resonant frequency of the resonant cavity due to animal growth and motion through both frequency tracking and dynamic IM. By driving the resonant cavity, measuring the reflected power back from the cavity, and adjusting the frequency in the direction of reduced reflections, we drive the cavity at the optimal resonant frequency. Utilizing a bank of capacitors and sampling the output voltage of the rectifier, we vary the impedance of the implantable receive device to adjust for changes in the resonant frequency of the cavity to improve wireless power. These improvements combined increase the average PTE by a minimum of 10.38% for the best case orientation of the receive coil. Finally, I propose and implant a modified system containing a battery back-up and recharging in a freely behaving rat demonstrating the ability of the device to provide near perfect power transfer when the batteries are not allowed to discharge.

2.8 Turn-On Transients Challenges

The frequency tracking system and algorithm make sizeable improvements for systems with and without the implantable dynamic IM system and can be used with success as is. There is a substantial drawback to the dynamic IM receive system, however. When the device initially does not have power, the capacitor bank does not have power and the switches used in the bank have no power. As a result, there are more added parasitic elements added to the capacitor that work to decrease the quality factor of the whole IM network when the device is in an off state. This directly causes an increase in required input power to turn on the devices in comparison to

devices without the dynamic IM network. In addition, the proper cavity operating frequency may be different than the frequency of the device utilizing the off-state parasitic-filled bank. This undefined off-state capacitance can present an even greater barrier to turn-on.

3. NOVEL COIL-TO-COIL TRANSIENT TURN-ON POWER REDUCTION SOLUTION

To effectively solve the turn-on transient, we present the concept of a two-coil receive system. We statically tune the first coil to have a low-Q, broadband response, which separately powers a digital system that only exists to dynamically match the impedance of the second high-Q coil. Next, the second coil powers the Bionode device with a high-Q impedance matching providing high power at one frequency. As a result, the first coil turns on at a wider range of frequencies and lower power when designed correctly, reducing the impact of the turn-on transient.

3.1 Potential Coil Configurations and Selection

In the receive two-coil system, two coils must be in close proximity and aligned in the same direction due to the constraints of implantable devices. This presents a challenge of reducing the two coils' effects on one another. To combat this, we consider a multitude of coil types, coil sizes, frequency bands, and coupling-reduction strategies. To reduce effects of the coils on each other, we explored and tested the three different setups shown in Fig. 3.1. Firstly, one transmit coil at one ISM band couples to one of the receive coils at the same frequency, and a second transmit coil at a second ISM band frequency couples to the second of the receive coils at the second ISM band frequency. Secondly, one transmit coil with a two-tone driving signal of two frequencies couples to two receive coils of the respective two frequencies. Thirdly, one transmit coil driven at a singular frequency couples with two receive coils at that singular frequency. Fig. 3.1 depicts these potential coil solutions. The first setups has issues with much of the power being wasted from coupling between the two large transmitting coils due to their spatial orientation. The second setup requires complex, restrictive, and inefficient two-tone generation and impedance matching methods on the transmit side as well as cross coupling between the two receive coils despite the frequency difference. The third setup suffers from high cross-coupling between the two receive coils and wasted power as a result. However, the third setup works if the two receive coils are coplanar and do not overlap in their windings so as to reduce coupling. This setup sacrifices the maximum achievable coupling and PTE as a result of

reducing the areas of each coil to place them side by side. Fig. 3.1 shows the two half-moon receive coils as well as the simple planar pancake transmit coil.

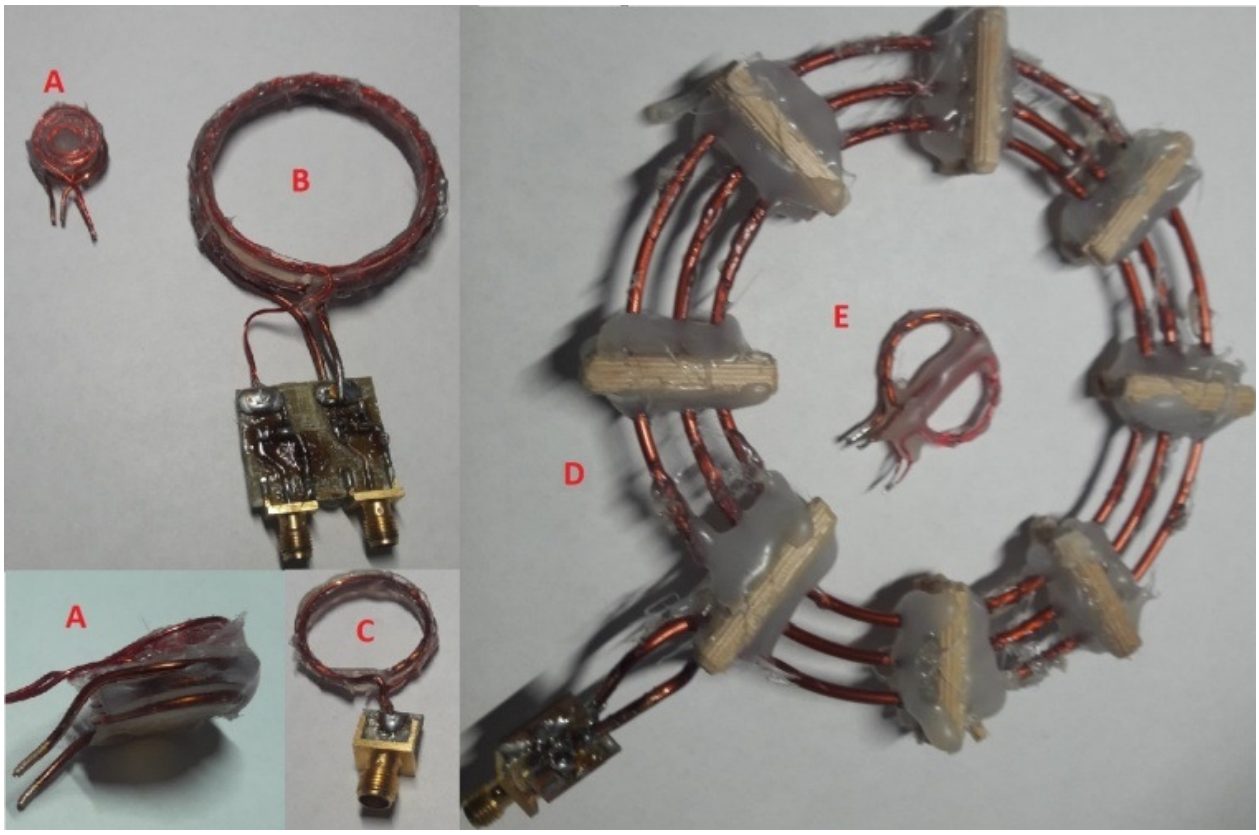


Figure 3.1. In the first test setup, transmit device B's two coils couple at different frequencies to receive device A's two coils. In the second test setup, transmit device D's coil couples at two frequency tones to receive device A's two coils, where A's first coil is tuned to first frequency, and A's second coil is tuned to the second frequency. In the third setup, transmit device D's coil couples to receive device E's two coils at the same single frequency. Device E contains two half-moon coils with one being a wider band, low quality factor coil, and the other being a narrower band, high quality factor coil.

3.2 Circuit Topology

Due to the issue of undefined capacitance in the capacitor banks during turn-on, we use varactors controlled by DACs for bias to vary capacitance for C_s and C_p for this work instead of banks. In addition, for the sake of further reducing interference between the two receive coils, the system utilizes the 13.56 MHz ISM band. The lower frequency results in less effect of the first coil's tuning on the second coil's tuning (and vice versa) when compared to the 345 MHz range of the cavity-based work. Two DACs and the ground voltage bias the two varactors through

inductors to help reduce RF leakage into or out of the DACs and ground. The updated dynamic impedance matching network and rectifier are updated from the previously modeled system and shown in Fig 3.2. An FPGA programmed with the same algorithm discussed in the cavity based receive device, controls the DACs and acquires data from an ADC measuring the rectifier as before. The FPGA searches for the optimal capacitance match for the highest rectified voltage. Fig. 3.3 demonstrates the circuit schematic for the system. The startup cycle involves the low-Q coil receiving enough power to turn on, powering the DAC, ADC, and FPGA to begin matching the impedance of the high-Q coil. Once the rectifier of the high-Q coil is at a higher voltage than the rectifier of the low-Q coil, a schottky diode allows the high-Q rectifier to begin powering the tuning circuitry and digital controls itself. Finally, the low-Q coil is intentionally detuned by shorting across the coil with a switch to further reduce the effect of the low-Q coil on the high-Q coil during steady state operation.

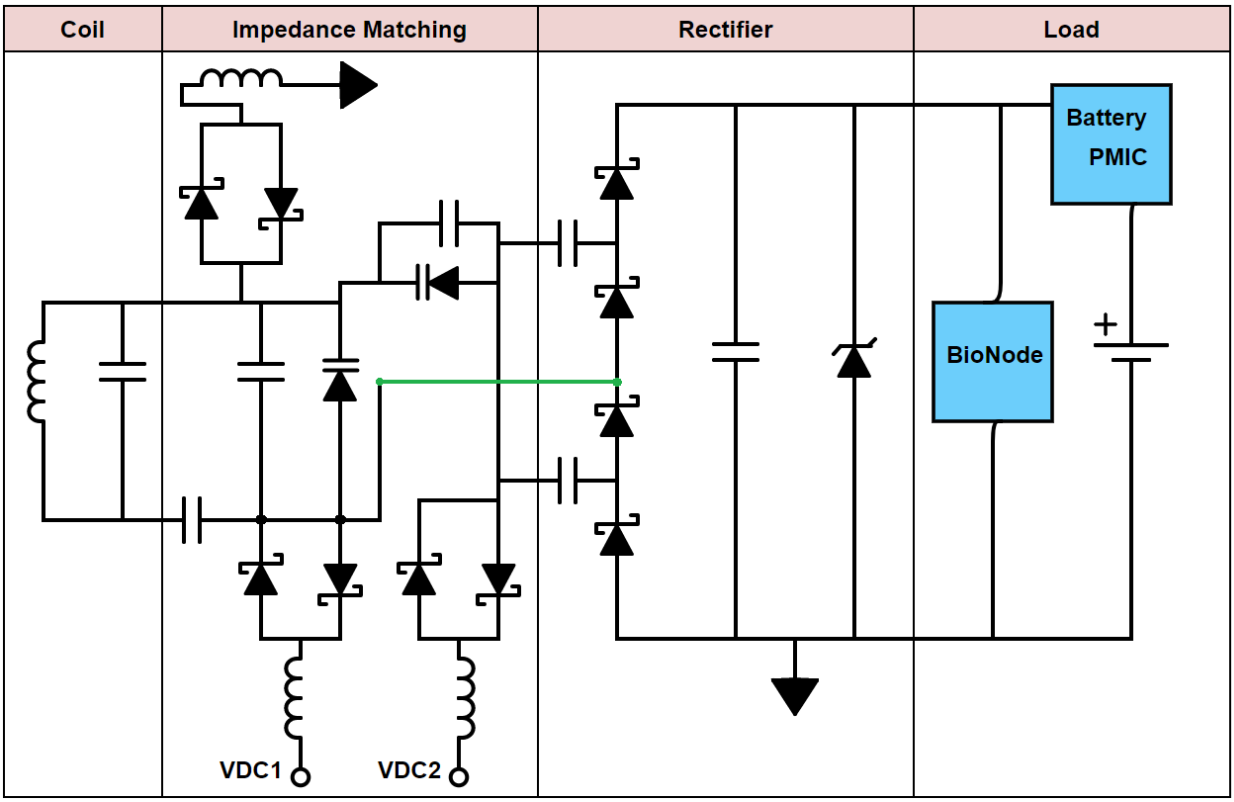


Figure 3.2. A schematic of the updated Powernode utilizing a similar circuit as before, but including two varactors as tunable capacitors. DC voltages applied to either side of the capacitors are AC-decoupled to prevent impedance contributions at high frequency. The LDO and switched capacitor circuits are omitted from this diagram purely for aesthetic purposes and readability.

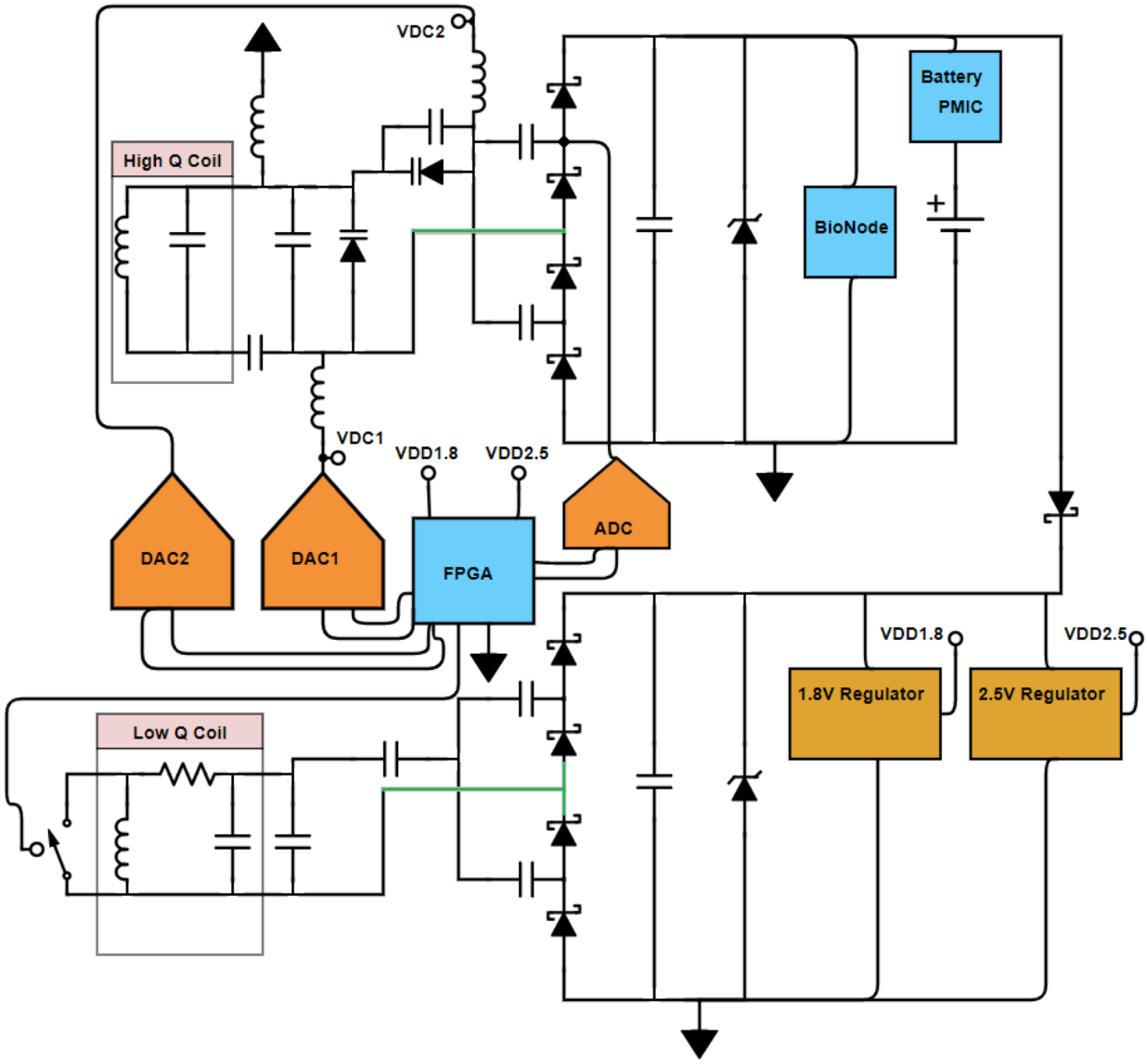


Figure 3.3. Schematic of the two-coil circuit design for improving turn-on transient in wireless powering. The low-Q coil power on first at a wide range of frequencies, starts to tune the impedance of the high-Q coil, and the high-Q coil powers the Bionode and eventually the tuning circuit itself.

3.3 Measured Results

We measure the PTE of the high Q half-moon coil and single pancake coil shown in Fig. 3.1e and Fig. 3.1d using a two port VNA measurement in the same fashion as the PTE measurements in the cavity-based work above. Additionally, we measure the PTE of the single full size coil and single pancake coil shown in Fig. 3.1c and Fig 3.1d. By statically tuning the full

size coil for the center frequency of 13.56 MHz and leaving the impedance the same for all different frequency measurements, we simulate what the static impedance case will be. This comparison is done to show the sacrifice of having half the flux area in the half-moon coil with dynamic impedance matching compared to the standard static case of having a single full size circular coil with no dynamic impedance matching. In addition, we allow the high-Q half-moon coil to be tuned for every frequency measurement by the FPGA on-board to simulate the dynamic impedance case. The transmit and receive coils are separated by 5.08 cm with the orientation of each lined up to maximize coupling. Fig. 3.4 demonstrates the PTE of the half-moon proposed coil compared to that of the single full size coil whose area is the same as the combined two half-moon coils. By inspection, the dynamically tuned half-moon coil sacrifices PTE at and near the center frequency of 13.56 MHz by reducing from 28% at max to only 16.6% at max. However, the dynamic impedance matching pays dividends on average by increasing the mean PTE from 8.83% for the static full coil up to a mean PTE of 14.83% for the dynamic half-moon coil over the displayed and measured frequency range of 12.51 MHz to 14.72 MHz. Thus, so long as the low-Q coil properly powers up the impedance matching hardware and algorithm on the FPGA, the two half-moon dynamic system is more robust and sufficient to provide power to an implant like the Bionode at safe input power levels. The low-Q coil's static impedance matching can be tuned to however wide of a band is required as long as power within that band of frequencies is sufficient to provide sufficient power to the ADC, DAC, and FPGA providing the high-Q tuning.

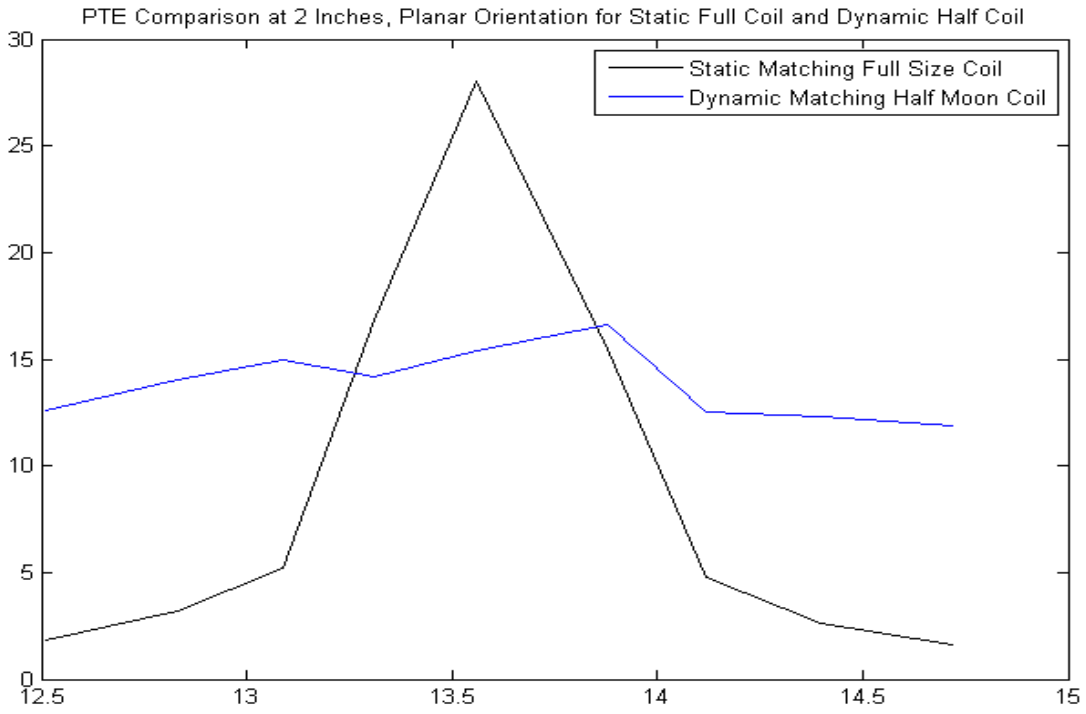


Figure 3.4. A plot of the dynamic impedance matching PTE for the high Q half-moon coil in Fig 3.1e versus the static impedance matching PTE for a coil in Fig 3.1c that is the full area of the low Q and high Q half-moon coils combined. Peak PTE drops as expected, but average PTE over a wide frequency range is much higher.

3.4 Summary

In this work, I address the shortcomings of the transient turn-on requirements of the cavity based dynamic impedance matching Powernode from the first section of this thesis. I propose and fabricate a two-coil receive solution for lower frequency coil-to-coil systems that increases the average PTE by 5% (additively) over the displayed frequency range at the cost of max PTE reduction of 11.4% (additively) at the center frequency of 13.56MHz.

4. ASIC FOR FLEXIBLE IMPLANTABLE DEVICES WITH BATTERY AND WIRELESS POWER

In implantable devices requiring the use of just one of battery or wireless powering, the power supply design of the device is rather straightforward. However, in the case of combining both power sources together in an efficient and enabling manner, more complicated and elegant solutions are required to gain more efficiency and allow for the device to operate a larger percentage of the time desired. In the following section, the various types of power supply and power conversion are discussed, as well as their end-use applications. Towards the end of the discussion, a suitable power converter for this power supply is selected and developed.

4.1 Power Conversion Topology Selection

In power supplies where voltages rails are slightly above the desired regulated level, a standard LDO can be used with great efficiency and minimal complexity. The efficiency of the regulator directly decreases as the input voltage rises further above the desired regulated output level. This relationship is expressed as:

$$Efficiency = \frac{V_{out}}{V_{in}}$$

where V_{in} is the input voltage, and V_{out} is the output regulated voltage. Because of this efficiency decrease at large input voltages compared to the output voltage, a different topology is necessary.

When voltage rails greatly exceed the output regulated voltage needed, a buck converter is useful in stepping down the input voltage to the output voltage seen in Fig 4.1. This is achieved through charging an inductor whilst increasing the output voltage of the converter and charging its output capacitor. Then, after charging the inductor, the input voltage source is switched out of the circuit, and the inductor discharges its charge to the output load. As the inductor and output capacitor discharge, the output voltage decreases. The cycle repeats, causing the output voltage to cyclically increase and decrease periodically. This ripple voltage generated generally must be held below a certain level to maintain proper noise reduction in the loading circuits of the implant. The output voltage of the buck converter is directly set by the ratio of the time spent charging the inductor to the time spent discharging the inductor expressed as:

$$D = \frac{V_{out}}{V_{in}}$$

where D is the duty cycle of the time charging the inductor to the time discharging the inductor, V_{out} is the output voltage, and V_{in} is the input voltage. This relationship is physically demonstrated in the amount of time that the pass PMOS device is on, which is the inverse of the amount of time per period that the shunt NMOS device is on. Taking a more practical view, the voltage drop across the non-ideal pass PMOS, the voltage drop across the non-ideal shunt NMOS, and the resistance of the inductor must be accounted for in the calculation of the duty cycle required, expressed as:

$$D = \frac{V_{out} + V_n}{V_{in} - V_p + V_n}$$

where V_p is the PMOS voltage drop in saturation, V_n is the NMOS voltage drop in saturation, and V_{ind} is the drop across the resistive portion of the inductor.

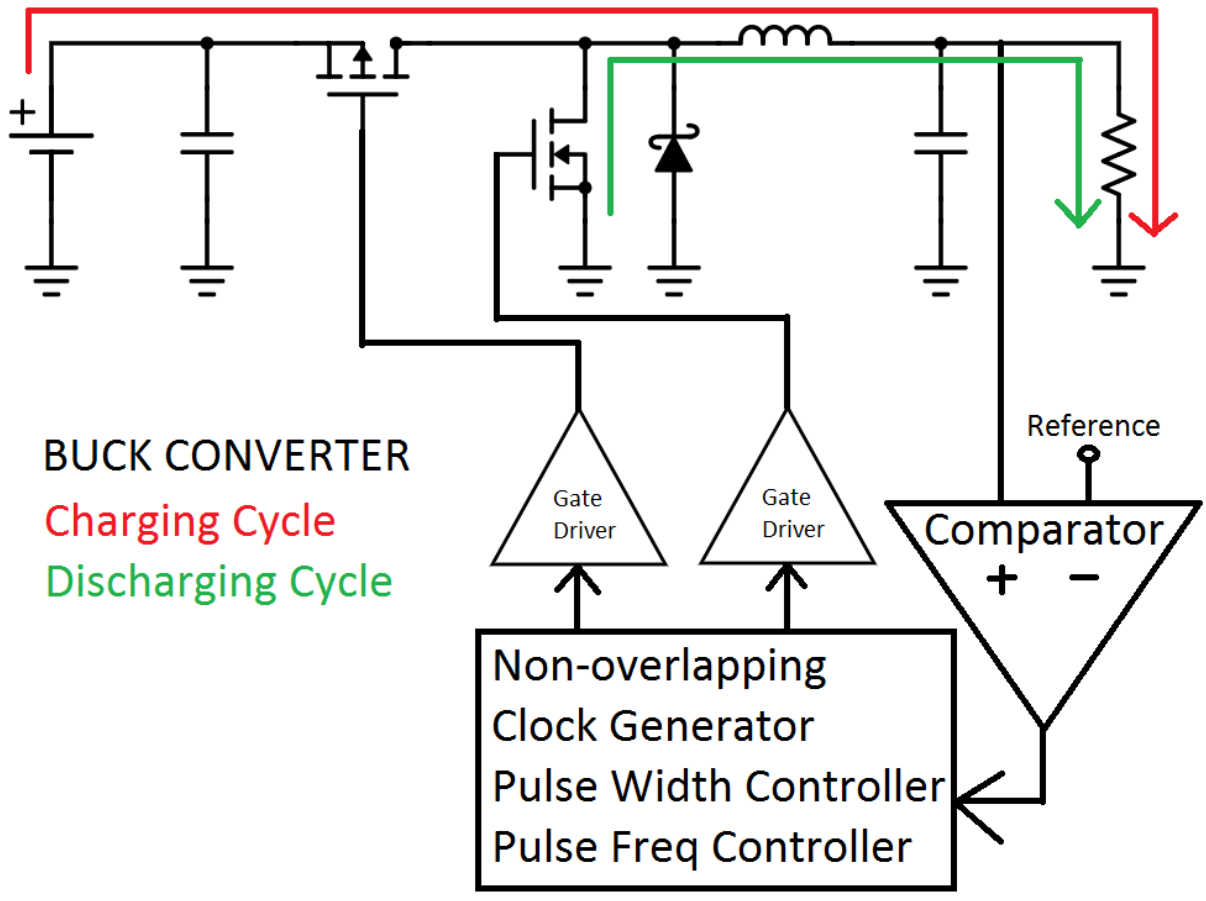


Figure 4.1. A standard synchronous buck conversion topology.

While the buck converter topology solves the step-down part of the problem, the cases where the battery is discharged, and the wireless powering is producing lower voltages than the desired regulated voltages must be addressed. This step-up conversion can be achieved through a boost converter topology seen in Fig 4.2. A boost converter operates similarly to a buck converter by charging and discharging an inductor periodically. Initially, the inductor is charged while the output voltage and capacitor are switched out of the circuit and isolated. After charging the inductor, the input voltage source and inductor are switched into a series configuration, pushing current forward into the output capacitor, which in turn increases the output voltage as the inductor discharges. Because the inductor and input voltage are in series, the two voltages add, resulting in a voltage presented to the output that is larger than the input. Next, the inductor is charged again by the input voltage source, and the output voltage and capacitor are switched out of the circuit and isolated. During this charging state, the output capacitor discharges into the output load while the output voltages decreases. This repeated charging and discharging cycle lead to a periodic decreasing and increasing output voltage, respectively. Similar to the buck converter, the output voltage is a function of the time spent charging compared to discharging, expressed as:

$$D = (\frac{V_{out} - V_{in}}{V_{out}})$$

where D is the duty cycle of the on time of the shunt charging NMOS. The relationship is physically demonstrated in the amount of time that the shunt NMOS device is on, which is the inverse of the amount of time per period that the pass PMOS device is on. Taking a more practical view, the voltage drop across the non-ideal components must be considered again, expressed as:

$$D = (\frac{V_{out} - V_{in} + V_p}{V_{out} - V_n + V_p})$$

where the variables are the same as in the buck converter case.

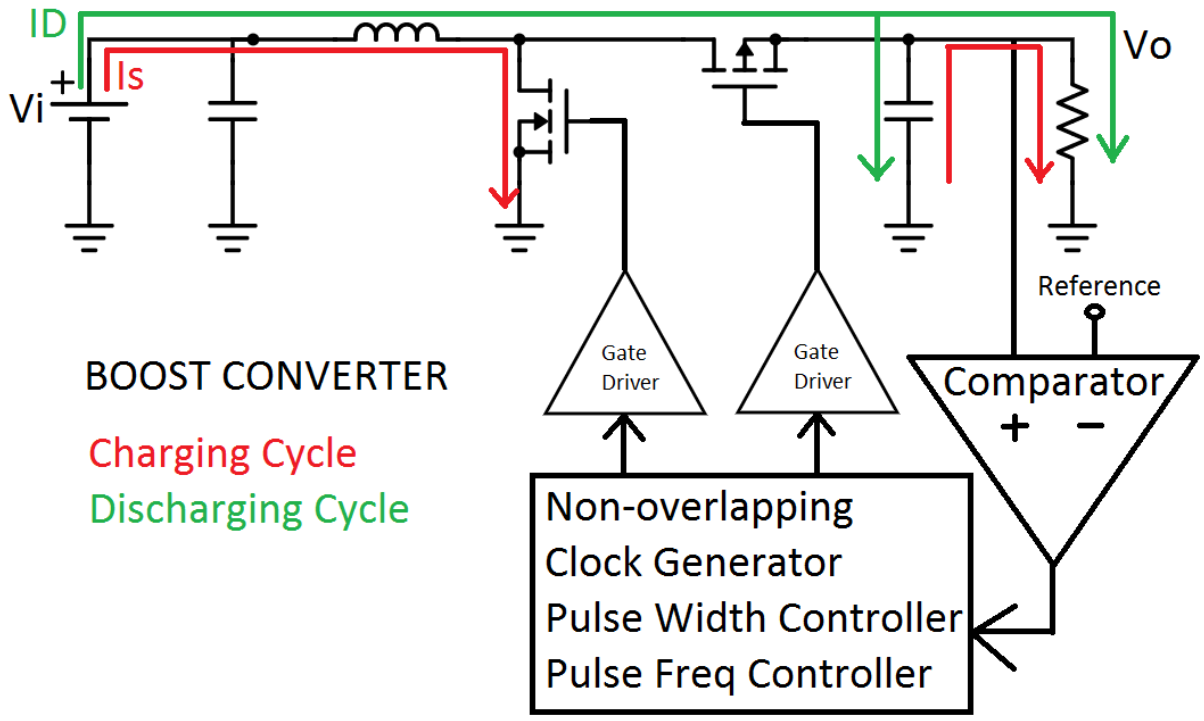


Figure 4.2. A standard synchronous boost conversion topology

To combine both of the functions of the boost and buck converters in an efficient way, there have been multiple topologies created, which include the single-ended primary-inductor converter (SEPIC), split-pi converter, buck-boost converter, switched capacitor converter, cúk converter, and non-inverting buck-boost converter (NIBBC). When selecting from these topologies, trade-offs include output polarity, number of inductors, number of capacitors, a need for bidirectional current, continuous or discontinuous output current, and efficiency at various stepping ratios. In implantable devices, space is limited to create less intrusive devices in the body, thus fewer inductors and capacitors is paramount. This eliminates the cúk, SEPIC, and split-pi converters as they require two inductors and multiple capacitors. Additionally, in this application, the output voltage polarity should be the same as the input voltage, which makes the buck-boost converter not applicable. Finally, the output voltage must be efficient at multiple voltages to maintain flexibility, which rules out the use of a switched-capacitor converter. Thus, the remaining converter is the NIBBC. This converter uses one capacitor and one inductor to provide step-up and step-down capabilities. Drawbacks of the converter include reduced

efficiency due to two pass PMOS elements, complexity of the control scheme, and additional power consumption of the controls for the converter compared to other similar topologies. The basic NIBBC is demonstrated by Fig 4.3. The duty cycle of the converter is mode dependent, and the buck duty cycle is expressed as:

$$D_{buck} = \frac{V_{out} + V_n}{V_{in} - 2V_p + V_n}$$

where the variables are the same as in the buck converter equation. The duty cycle of the boost mode is expressed as:

$$D_{boost} = (\frac{V_{out} - V_{in} + 2V_p}{V_{out} - V_n + 2V_p})$$

By inspection of the two duty cycles, the converter must contend with two pass power PMOS compared to the buck converter or boost converter topologies. As a result, the duty cycles are slightly different if designed well, and the power consumption of the converter overall is traditionally lower by default than the individual converters due to the extra PMOS power switch voltage drop, without mentioning the additional power required by the more complicated controller required for a NIBB converter.

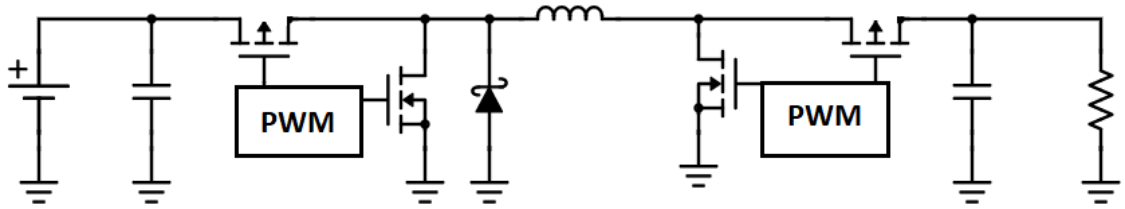


Figure 4.3. A standard PWM-based NIBBC topology.

4.2 General NIBB Converter Concerns

The NIBBC contains numerous required blocks to operate both effectively and efficiently. Of these concerns, the ability to use the highest voltage in the system to drive the gates of the power switches is paramount. In addition, proper body biasing of the power switches is of particular concern to reduce body diode conduction and erroneous operation. Additionally, at various loading conditions, power switch width may be reduced or increase to accommodate these conditions. When driving these various power switch sizes, different gate driving topologies that

quickly change the gate voltage while operating efficiently are also necessary. Another issue of note is the wide variety of voltage stepping ratios in buck and boost mode. To properly step to the right level, a variety of pulse widths and duty cycles must be produced to drive the power switch gates. After generating these pulse widths, the correct pulse width must be selected based on the ratio between the input and output voltages, the operation mode, and the current output required. Thus, the input and output voltage must be measured, binned into ranges, and then used to determine the proper pulse widths. To meet this goal, an ADC is used, and a low power, accurate, and fast comparator must be designed to create the comparisons between the voltages and expected ranges. Finally, because any ripple in excess of a few tens of millivolts can jeopardize signal integrity in biopotential acquisition circuits, an LDO must be designed to further suppress ripple at the output of the converter while having a low dropout to not further reduce efficiency by much. Each of these concerns are discussed below and circuits to tackle them are presented. The full block diagram of this work's NIBBC is presented in Fig 4.4.

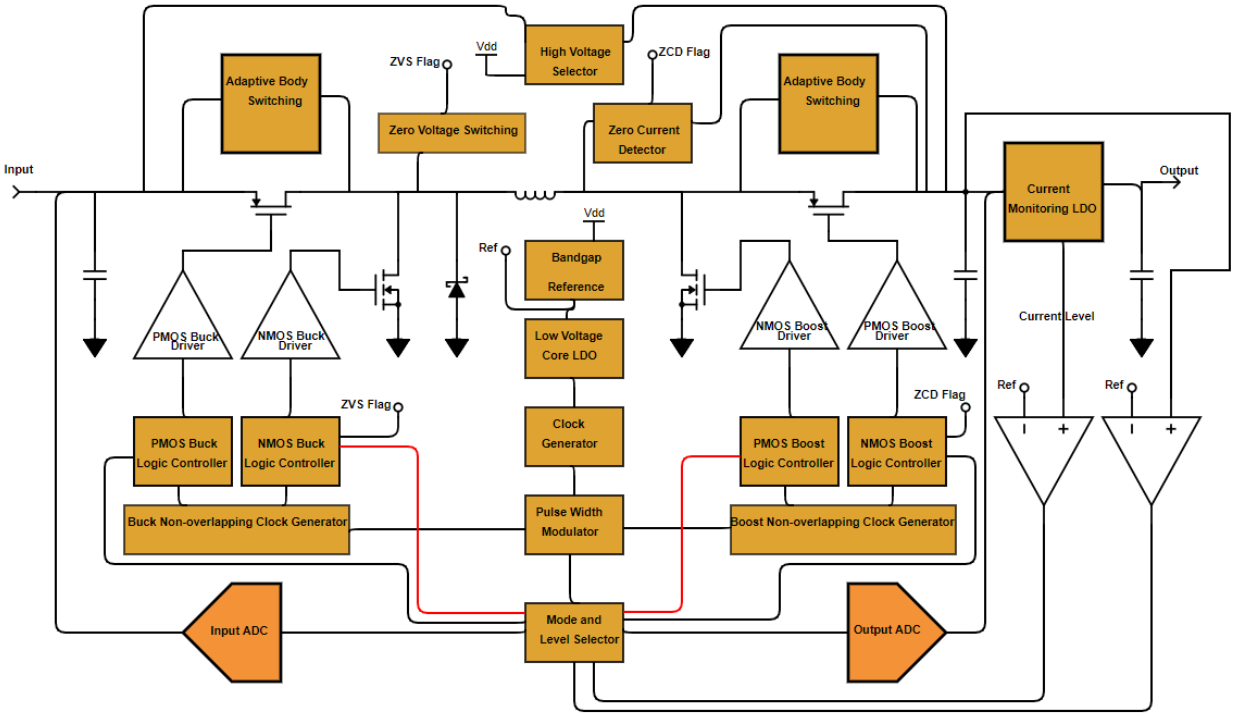


Figure 4.4. The top level block diagram and circuit schematic combined of this work's NIBBC design. Four power switches, an inductor, and a capacitor are the main NIBBC component seen in the converter diagram.

4.3 Power Switch Sizing and Driving

In power conversion, power switches of minimum length and extremely large width are placed in parallel in many times over to ensure low on resistance of the transistors when conducting high currents. In this work, currents as low as 1mA and as high as 30mA must be conducted through the switches with minimal resistance and loss. As a result, transistors of minimum length and 100um width are placed in parallel. The parallel multiplier of these transistors can range from 125 copies to 450 copies for the PMOS and can range from 30 to 100 for the NMOS. These ranges are put in place to allow for the digital core of the device to select how many PMOS or NMOS are needed in parallel to be driven at a time based on the voltage stepping ratio and output current required. In the case of very low input voltage and higher output voltage in boost mode, more gates are driven and used in the power switches to accommodate. Similarly, in the case of similar input voltage and output voltage in buck mode, more parallel power switches are used to quickly discharge the inductor at extreme duty cycles. Finally, if high output current is required, more power switches are used in parallel to provide the low resistance required.

To drive these gates, a gate driving topology is selected to quickly take a weakly driven input digital signal and provide a low impedance output driving source that is able to transition between the highest and lowest voltages in both directions. It is crucial in this design to minimize the amount of time that any wider transistors spend in the triode region to reduce transient losses. In the literature [22], a gate driver utilizing two small coupling capacitors is designed for this purpose. The gate driver is adapted for the specific speed and output impedance required in this application, and the ability to disconnect the input signal from the driver while shutting off the power switches during a power-on-reset (POR) is added in the form of transmission gates and pull-down and pull-up transistors as illustrated in Fig 4.5.

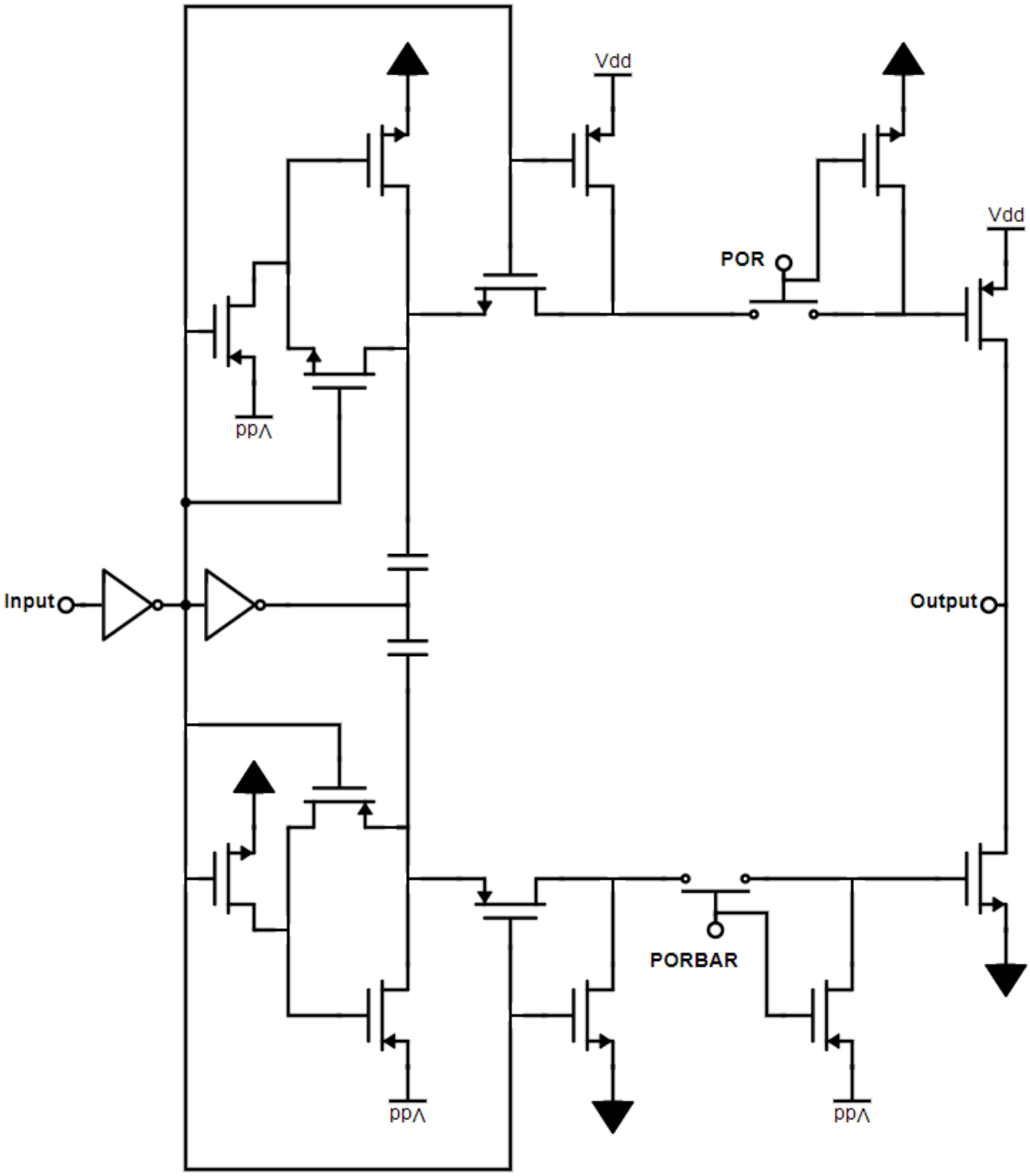


Figure 4.5. A gate driver topology designed to quickly transition a power NMOS or PMOS between cutoff and saturation with minimal linear region transition time. A POR circuit disable is added to the circuit for soft-starting.

4.4 Power Switch Body Bias

Due to the nature of the converter, the input voltage, output voltage, input side voltage of the inductor, and output side voltage of the inductor can all be the highest or lowest voltage at various moments of the converter's operations. As a result, the body voltage of the PMOS power switches in series with the inductor must be tied to the higher of its two channel connections. If this is not the case, the body diode conducts erroneously, leading to improper operation, loss of efficiency, and potentially inability to step to the right output voltage. To combat this, a cross-coupled, current limited differential amplifier is used to properly select the higher of the two channel voltages to tie to the body of the PMOS power switch as well as the body of all of the PMOS in the amplifier and selector itself. This body bias selector circuit must operate in real time, irrespective of the clock, as variations in the required body voltage change faster than the clock itself. Current is limited by the tail current of the amplifier's common NMOS. This type of circuit is not necessary in the case of the two NMOS as ground is always either the lowest voltage in the circuit, or in the case of the voltage placed on the input side of the inductor, a Schottky diode is placed in parallel with the power NMOS to allow for current flow up from ground when both the buck power PMOS and NMOS are in cutoff, preventing the power NMOS body diode from ever conducting forward current. This circuit is show in Fig. 4.6.

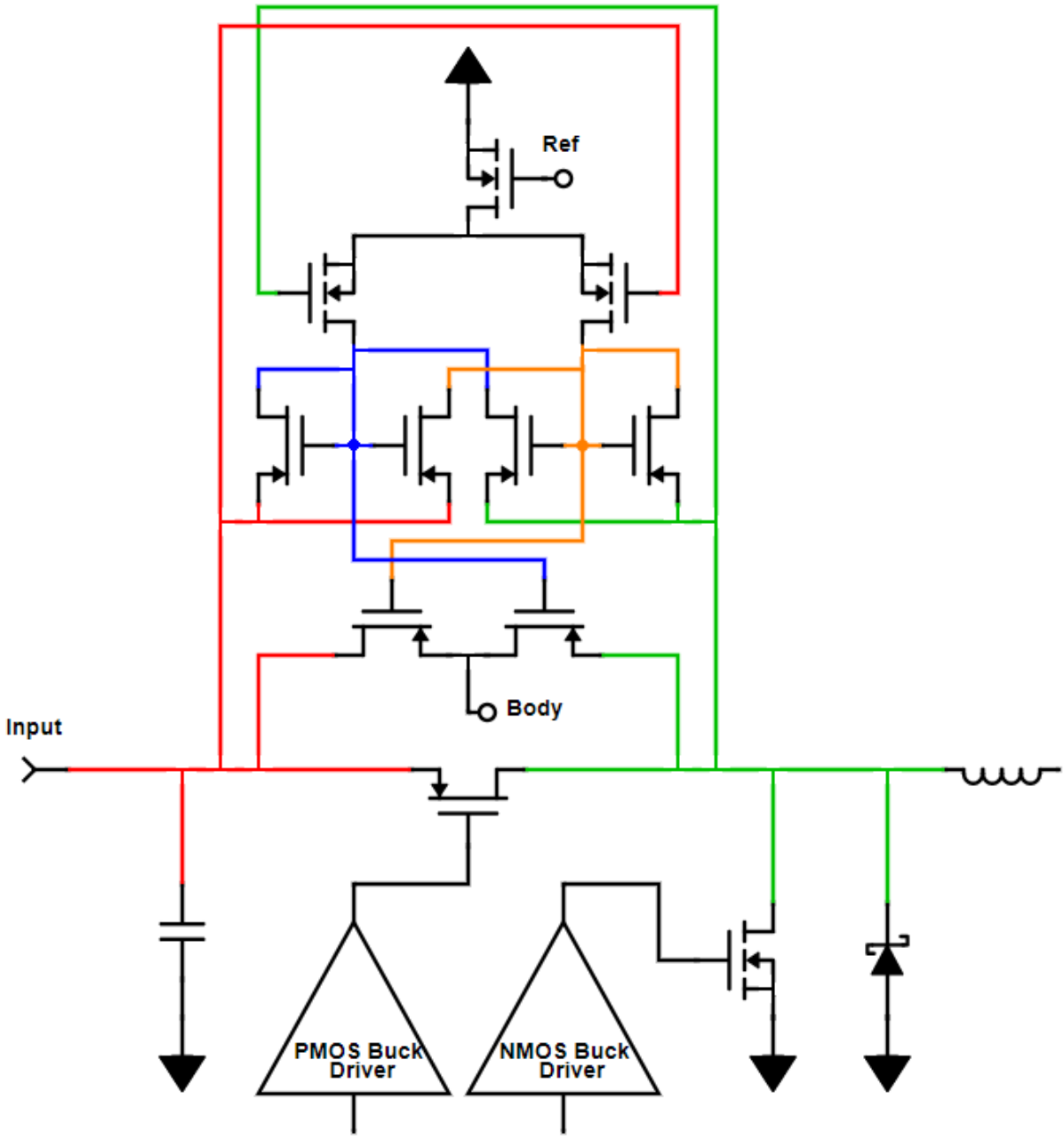


Figure 4.6. A circuit capable of quickly applying the higher of the two channel contact's voltages to the body of the power PMOS in the NIBBC. This prevents body diode conduction.

4.5 High Voltage Selection

In the NIBBC, either the input or output voltage of the converter can be the highest steady state voltage in the converter. In buck mode, the input voltage is higher; whereas in boost mode, the output voltage is higher. As such, the higher of the two voltages needs to be used to drive the power switches. In the case of the power PMOS, if anything less than the highest voltage minus a PMOS threshold voltage is used to drive the gate of the power PMOS, then the transistor will not be in cutoff and will leak current through at wrong times in operation, resulting in poor regulation, lower efficiency, or inability to convert to the correct output voltage. In the case of the power NMOS, it is not as critical to drive the gate with the highest voltage in the system so long as the gate voltage ensures that the NMOS is in saturation. However, using the highest voltage in the system will provide a lower on resistance in the channel of the NMOS and is desirable in achieving higher efficiencies in the conversion. To this end, a continuous time high voltage selector with the ability to robustly provide output current efficiently is found in the literature [23]. Based on this work, the circuit is adapted for the power and speed constraints of this particular converter, and hysteresis is added to prevent any scenario involving the input and output voltage being approximately equal. This would result in both pass PMOS to the output being turned on partially, leading to direct and resistive conduction between the input and output of the converter, ruining the conversion efficiency and jeopardizing the ability to properly convert. The updated circuit schematic is demonstrated in Fig 4.7.

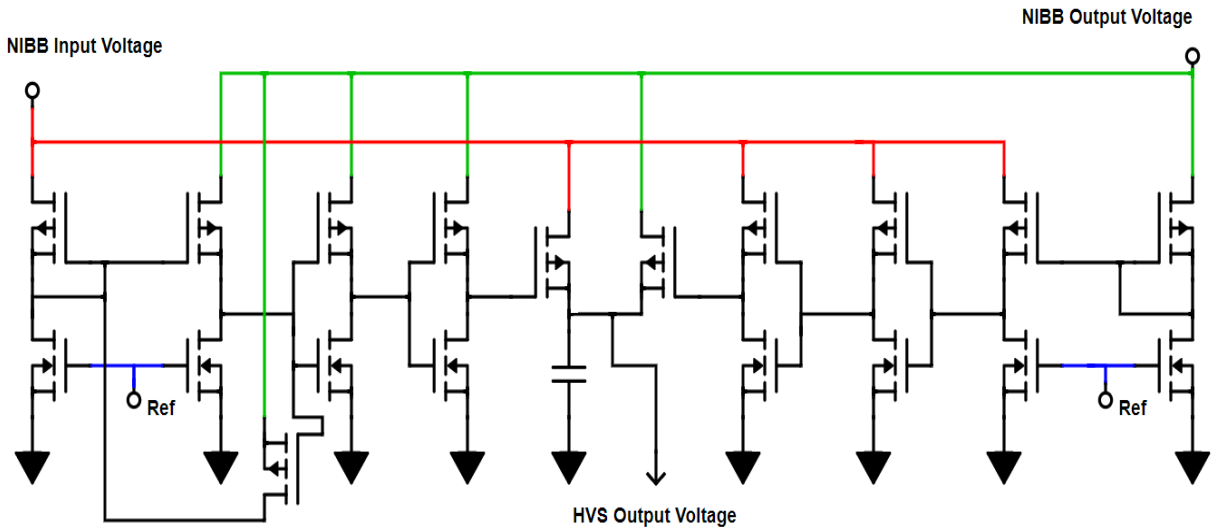


Figure 4.7. A high voltage selector circuit designed to use the higher of two analog voltages as the output supply, while presenting a high impedance to the lower supply voltage source.

4.6 Input and Output Voltage "Binning"

Generally, in analog continuous buck or boost converter, the output duty cycle is generated off a continuous time amplification of the difference between the output voltage and the desired output voltage level via an error amplifier. Based on this voltage difference, the duty cycle of the power switches is generated. In the case of this NIBBC, a digital approach is taken in how the duty cycle is generated. To select from these discrete duty cycles, the difference between the input and output voltage must be known. In addition, the output current required must also be factored in. To achieve these comparisons, the input voltage is divided down by various factors and compared against the BGR voltage. The output voltages, meanwhile, are selected at the PCB level by connecting three digital external pads to either digital low or high. This can allow for either static programming of the desired output voltage or for dynamic adjustments via a microcontroller or FPGA off-chip. The off-chip selection method is used in this chip due to the serious challenges involved in determining what is the correct output voltage range during regular operation. The problem lies in the transient nature of the output during operation. The only information known about the output voltage on-chip is whether or not it is

above the desired regulated output level or below the level. One could design a system where the first time that the output reaches this desired level, the output is sampled and stored to determine the bin it falls into. However, this method relies on the output not being close to the edge of two bins and rapidly increasing or decreasing into the neighboring and incorrect bin of voltages before a clocked comparator or ADC is able to properly measure the voltage. In the case of lighter loads and smaller output capacitance, this corner case happens quite regularly in that sort of proposed one-shot output measurement system and consistently produces the wrong bin measurement. As a result, the system has been designed with off-chip selection instead.

The input and output bins and voltage ranges are presented in Table 4.1 below. To accommodate the measurement of these ranges, five buffered comparators are used in parallel. However, to save on power consumption, two comparators at maximum are actively sampling at any given time. Initially, the input is determined initially to be in the lowest bin, thus the comparator checking for the lowest level is the only comparison being performed. If the level is determined to be above the lowest range, then the next clock cycle will require that the lowest level comparison be checked again, but the next higher level will also be checked. In this manner, every clock cycle will allow for checking if the input voltage bin should move up by one, drop down by one, or remain the same. This approach saves on power by preventing more than two comparisons per clock cycle. However, the sacrifice is that for large steps in input voltage level, the correct level may take at most five clock cycles to determine. This will in turn result in the wrong duty cycle or operation mode being used for at most four clock cycles, which will cause increased ripple during the incorrect operation mode and duty cycle. This approach overall was deemed to be preferable to the inclusion of a full ADC due to the large power requirement of a delta-sigma ADC or the additional area, complexity, and faster clock than the overall system clock for a SAR ADC.

Table 4.1. The description of the operation mode and duty cycle for every input and output voltage bin case.

Input Voltage Range (V)	Output Voltage Range (V)	Operation Mode	Charging to Discharging Time Ratio
0-1.6	0-1.9	boost	low
0-1.6	1.9-2.2	boost	medium
0-1.6	2.2-3.3	boost	high
1.6-2.2	0-1.9	boost	low
1.6-2.2	1.9-2.2	boost	medium
1.6-2.2	2.2-3.3	boost	high
2.2-2.5	0-1.9	buck	high
2.2-2.5	1.9-2.2	short	not applicable
2.2-2.5	2.2-2.5	boost	low
2.2-2.5	2.5-2.8	boost	medium
2.2-2.5	2.8-3.3	boost	high
2.5-2.8	0-1.9	buck	medium
2.5-2.8	1.9-2.2	buck	high
2.5-2.8	2.2-2.5	short	not applicable
2.5-2.8	2.5-2.8	boost	low
2.5-2.8	2.8-3.3	boost	high
2.8-3.1	0-1.9	buck	low
2.8-3.1	1.9-2.2	buck	medium
2.8-3.1	2.2-2.5	buck	high
2.8-3.1	2.5-2.8	short	not applicable
2.8-3.1	2.8-3.3	boost	low
3.1-3.3	0-1.9	buck	low
3.1-3.3	1.9-2.2	buck	low
3.1-3.3	2.2-2.5	buck	medium
3.1-3.3	2.5-2.8	short	not applicable
3.1-3.3	2.8-3.3	boost	low

In addition to determining the pulse width, the output and input bins help determine how many gates in parallel are used in the power switches as well as the operation mode used. In general, if the input bin is lower than or the same as the output bin, boost conversion is used. If

the input bin is one higher than the output bin, the PMOS power switches are turned on, and the NMOS power switches are turned off, resulting in a near short circuit between the input and output - called "short" mode henceforth. If the input bin is more than one higher than the output bin, buck mode is used. One additional wrinkle in the operation is that if the input exceeds the output voltage but the two are in the same bin, the converter operate as if it were in short mode but with the ability to quick switch back to boost mode should the input dip. The determination of the modes is shown in the previous Table 4.1.

4.7 Comparator Selection and Design

To perform the comparisons for the voltage bins, a low power, reasonably fast, and accurate comparator is required. To achieve the lower power, a clocked and latched comparator is a must to prevent continuous current draw of the differential amplifier used. To achieve speeds required, the comparator topology needs to include transiently large current draw. However, this time that this current draw is required must be minimized. Finally, to increase the accuracy across a variety of input voltages, a rail-to-rail topology is selected with complimentary NMOS differential and PMOS differential amplifiers being combined with current mirroring [24]. This topology is modified to include a different power saving technique that allows for the amplifier to only be sampling as soon as the clock rises, but to stop sampling once a comparison result is achieved and is presented in Fig 4.8.

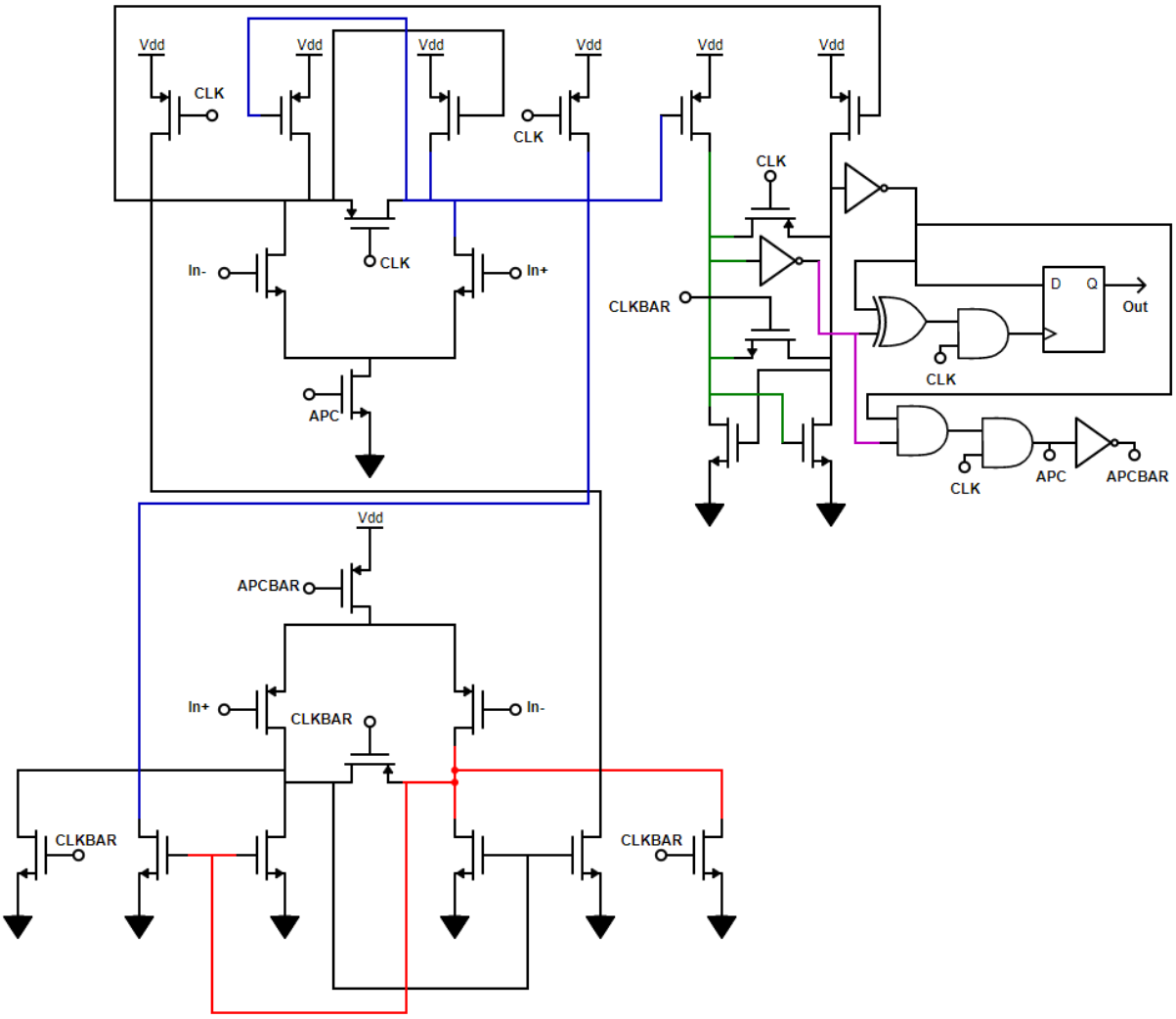


Figure 4.8. A low power, rail-to-rail comparator designed to minimize the amount of time that the comparison is computed during, thus reducing power consumption.

4.8 Start-up and Soft Start

During the start-up portion of the converter's operation, the output voltage is close to zero, the capacitors are discharged, and an input voltage source above 1.5V is applied. At this time, without any precautions, the input PMOS power switches would be open, and huge transient currents could pass through the converter's power switches to charge the low impedance uncharged capacitors. These high currents can lead to damage to the power switches as well as prevent start-up by presenting too low of an impedance to the input voltage source, causing the input voltage to fall below the appropriate level. To help prevent this, the power PMOS switches

are held off as soon as the input voltage reaches a few hundred millivolts. Initially, the applied input voltage must rise to 1.5V to provide the proper headroom to start up the BGR, which in turn starts up the internal 1.3V LDO used to power all circuits on the chip, excluding the gate driver, logic shifters, and ZCD. While the digital regulator is powering up, a POR is asserted to prevent converter operation until the BGR and LDO voltage are at appropriate levels. At this point, the POR returns low, allowing the chip's digital operations to begin. Next, to further prevent high currents during initial charging of the output capacitors, a smaller PMOS power switch width is used to limit current, and the output LDO of the converter is turned off, preventing the output load from being in parallel with the uncharged capacitors' low impedance. Finally, the converter always uses the boost conversion mode on start-up until the output reaches the appropriate desired regulation level. Once the converter's output reaches 1.8V, a start flag is asserted, and once the output reaches the desired regulation level for the first time, a power good flag is asserted. The power good flag will be reset to low is the output voltage of the converter ever drops below 1.8V. Once the power good flag is asserted, the start-up cycle ends, and the all of the converter's modes of operation can be used, allowing for boost, buck, and pass operation. A diagram of this start-up detection circuit is shown in Fig 4.9.

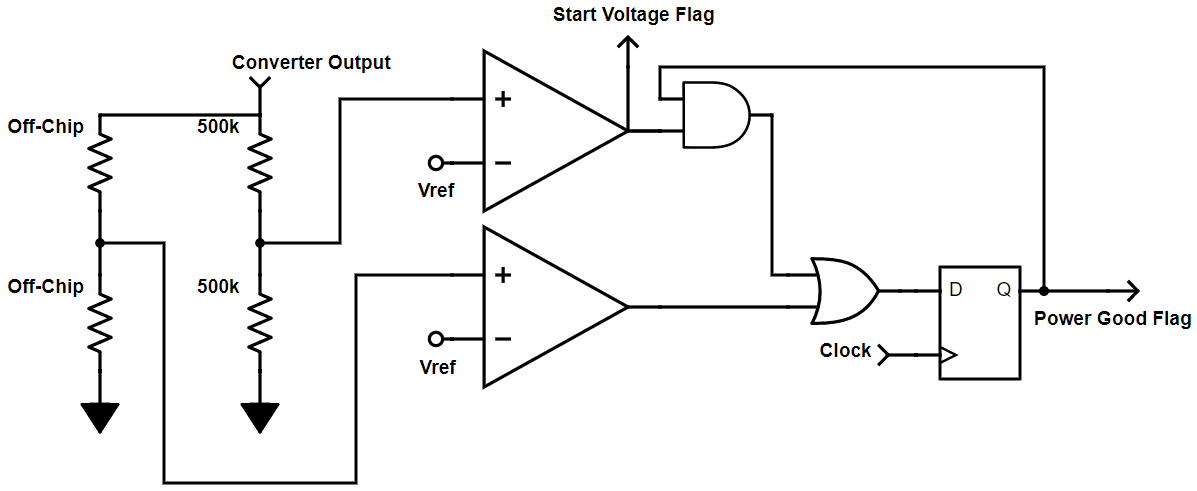


Figure 4.9. The diagram of the start voltage flag being thrown upon the converter's output reaching 1.8V, and the power good flag being thrown upon the output reaching the desired regulated level for the first time after the start voltage flag is thrown.

4.9 Output LDO

As discussed in previous sections, the output of the converter has ripples around 50 millivolts at lighter loads and larger converter stepping ratios. The inclusion of an output LDO is done for two major reasons. Firstly the LDO combats this noise and prevents injection of ripple into the sensitive measurement circuits of the biopotential recording implant. Secondly, the implantable end uses of the converter require very stable start-up during wireless powering applications, and any initial spike or jump in output voltage on start-up can result in shocks being provided to the animal. These unexpected jolts in charge delivered to the animal can cause injury or discomfort to the animal, which, aside from being morally unacceptable, can cause complications in the animals habits and behaviors during sensitive studies. Using the LDO allows easy and safe start-up by turning of the LDO initially to isolate the Bionode and animal from the NIBB converter while the output of the converter charges up to a stable level. This regulator is designed to have low dropout in particular to prevent additional loss of efficiency in the drop across the converter. The dropout at the maximum current output of the converter and lowest input voltage is approximately 47mV. This ensures minimal additional efficiency loss via drop across the pass PMOS in the LDO. The speed of the regulator's feedback loop needs to handle ripple at frequencies between 1 MHz and 2 MHz. The current draw of the regulator's non-pass elements is 65uA to 125uA, depending on input and output voltage, and the common LDO topology is presented in Fig 4.10.

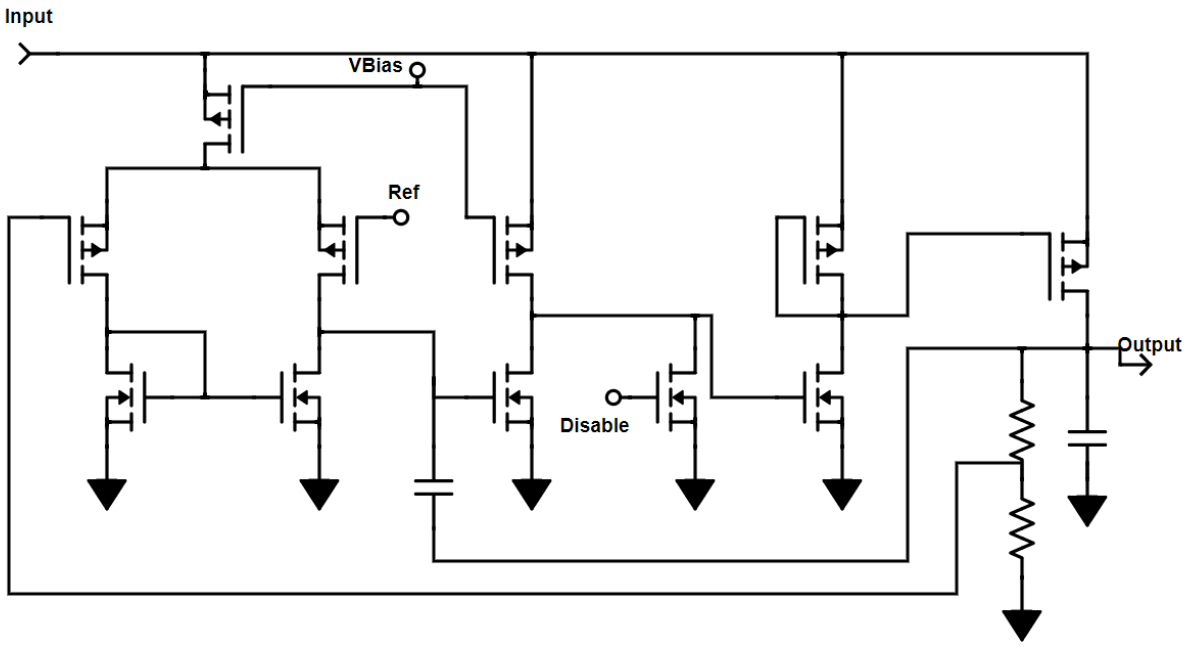


Figure 4.10. A common topology for an LDO with additional feedback capacitor and disable option for soft-start in the NIBBC.

4.10 Combining PWM and PFM

In power converters, two of the popular main operation modes for regulation are pulse width modulation (PWM) and pulse frequency modulation (PFM). PWM involves varying the pulse width of the power switches, thus leading to varying duty cycles of the charging and discharging. This in turn modifies the voltage conversion ratio at the output of the converter. PWM is done in the continuous analog domain as well as in the purely digital discrete domain. In the continuous analog case, an error amplifier compares the output signal to the desired regulated level and uses the amplitude of the amplifier's output to directly modulate the pulse width. Analog continuous PWM is specifically useful at high output currents or where tight regulation is required with minimal ripple [25]. This is due to the high current requirement to run the fast error amplifier as well as ramp generating circuit; the ripple and regulation directly corresponds to how much power is consumed in the controlling circuits, which is beneficial at high output currents as the controller internal currents do not scale up at the same rate as the output currents. In the discrete digital PWM case, the output can either be fed into an error amplifier in the same manner as the analog continuous converter or can be discretized with an ADC. The output level

or error signal then allows the converter to select from some predefined pulse widths to use for the power switches. This approach can be used when power needs to be saved in the converter's controller as this method does not need a high speed ramp generator or potentially a continuous error amplifier. These PWM strategies are generally employed at higher currents or where the minimum output current is not a small fraction of the output current range [26].

In the case of both lower power converters and cases where the lowest output current required is a small fraction of the range of output currents required, the converter can utilize PFM topologies. This strategy employs one pulse width, and modulates the output voltage by skipping pulses. Simply put, if the output voltage is higher than the desired level, the next pulse is skipped and the converter will continue to discharge from the inductor in the buck case or continue to discharge from the free-wheeling output capacitor in the boost case until the output level falls below the desired level. This type of converter is able to achieve higher efficiencies than PWM at light output loads but fails to maintain the low ripple or tight regulation that the PWM converters can provide [25]. As a result, an output LDO can be added to provide ripple reduction and further regulate at the output to compensate.

In this converter, a hybrid approach is taken. Three discrete pulse widths are selected from based on the input and output voltage bins. In addition, PFM is employed at low output current and light loading cases. As a result, the converter should have the benefit of operating at light load efficiently with PFM while maintaining reasonable ripple levels and regulation at higher output currents with PWM.

4.11 Digital Core And Signal Generation

As discussed in previous sections, the digital core of the chip includes a BGR, a POR, a 1.3V LDO for digital circuits' supply, and an oscillator for PWM signals. In this converter, three PWM pulse widths for buck conversion and three PWM pulse widths for boost conversion are required. To create these signals as well as keep all circuits on the chip synchronous that require it, a ring oscillator is used to create both the standard system-wide clock as well as the PWM signals. Because neither the frequency of the clock nor the PWM signals needs to be particularly accurate, a ring oscillator provides multiple phases of a clock signal in a reliable fashion with reasonably low power consumption. As a result of not needing the extra accuracy and not wanting any off chip components added, a PLL and LC oscillator were ruled out. Should the

clock have much error from its designed frequency, all of the PWM signals would also shift in frequency, but the relative duty cycles would still remain mostly constant. To combat any error due to PVT, a process compensating bias voltage source is used to correspondingly reduce or increase the current of all inverters to make up for PVT variations. To keep the power consumption low, the current is limited in the inverters via current starved PMOS with the aforementioned bias voltage.

To generate the various PWM signals, various phases of the clock from different inverters in the nine inverter ring are used. Two different phase signals are used as inputs to an XOR gate-based phase detector, producing an output pulse width that goes high when the first input signal rises and falls when the second input signal rises. The circuit uses a third signal from the inverter chain to reset the detector every cycle to prevent any issues where the detector erroneously detects the second signal rising before the first signal rising due to varying start-up conditions in the oscillator, resulting in a wrongly generated pulse width. Due to the particular pulse width needs determined from initial simulation, nine inverters were used to create the resolution necessary for the pulse widths. A schematic of the bias voltage generator, inverter chain ring oscillator, and two of the six phase detectors is shown in Fig 4.11. In addition to the aforementioned POR requiring the input voltage to rise to an appropriate level before falling, the POR also requires that the oscillator correctly starts up and requires 16 successful clock cycles to pass before it falls. This is accomplished with a 4-bit up counter circuit that asserts a flag to the POR when the counters bits all read logic high.

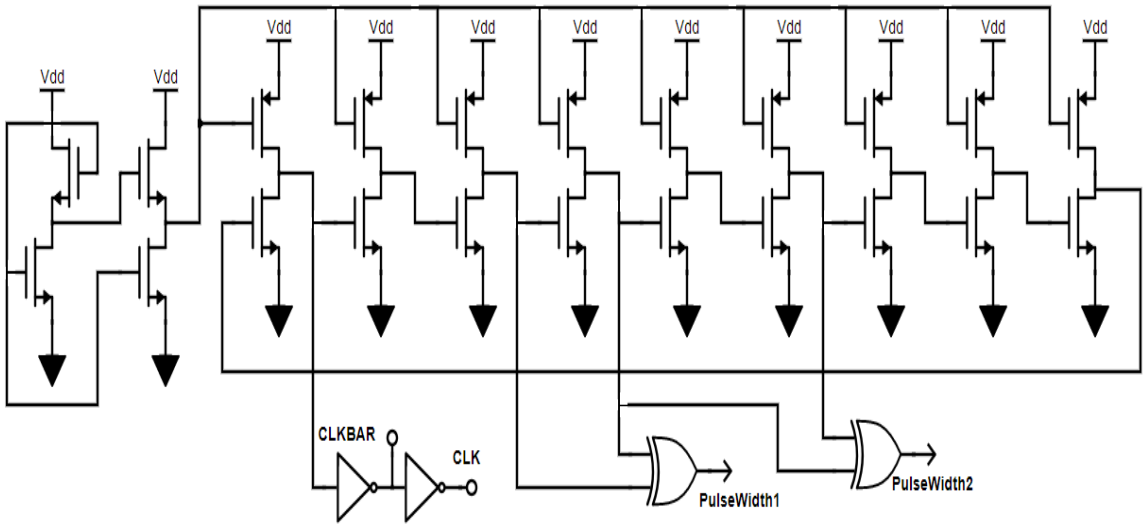


Figure 4.11. A 9 stage inverter-chain ring oscillator with example phase selector based pulse width generators.

4.12 Duty Cycle Determination

All duty cycles are generated by the six phase detectors in the ring oscillator circuit. However, based on the voltage binning circuits previously discussed, the most appropriate pulse width is selected. The pulse width with the minimum charge to discharge time ratio necessary to maintain proper regulation is desired in all modes and all states as this prevents the need to use PFM in all non-light load scenarios. In addition, the proper selection also keeps the converter from hitting zero current in the inductor during discharging, requiring a free-wheeling state to operate. Finally, the pulse width with the minimum charge to discharge time ratio will also produce the least ripple in the output and prevent as much overshoot in the portion of the cycle where the output increases. This is also a desirable outcome in terms of efficiency as the output voltage is not higher than required, which results in less input current necessary. Table 4.1 above provides the charge to discharge time ratio of each input and output voltage range. In the case of "low" ratios, the duty cycle of charging to discharging the inductor in both boost and buck states in relatively low. Conversely, the "high" ratio results in the duty cycle of charging to discharging the inductor in both modes is relatively high. In short mode, no pulse width is necessary and is labeled as "not applicable" in the table.

4.13 Non-Overlapping Signals

Once the pulse widths are generated, and the appropriate pulse width for the mode and conversion ratio is selected, the pulse is sent to a non-overlapping clock generator. This circuit, presented in Fig 4.12, takes the pulse input and generates two output signals of the same polarity and approximately same pulse width as the input signal. The caveat is that "PMOS OUT" signal in the circuit will rise before the "NMOS OUT" rises, and the "NMOS OUT" signal will fall before the "PMOS OUT" signal falls. An example simulation of the circuit shown in Fig 4.12 is provided in Fig. 4.13. This results in two signals where there is no time when the two are transitioning at the same moment. The reasoning for this is critical to maintaining proper regulation and efficiency in the converter. The power PMOS and power NMOS in the buck circuit or the boost circuit cannot both be in linear or saturation mode at the same time. Only one of the PMOS and NMOS pair can be in linear or saturation mode, and the other must be in cutoff. This prevents unwanted current being shunted to ground from the input in the buck conversion mode, and it prevents unwanted current being shunted to ground from the output in the boost conversion mode. In the non-overlapping clock generator circuit, the circuit is designed to make sure that in all cases, the power PMOS switch turns off prior to the power NMOS switch turning on, and the power NMOS switch turning off before the power PMOS switch turns back on. The generator is modified from the literature to provide the ability to have very small pulse widths with respect to the clock period as well as ensure a sufficient amount of off time for both power switches between turning either on [27].

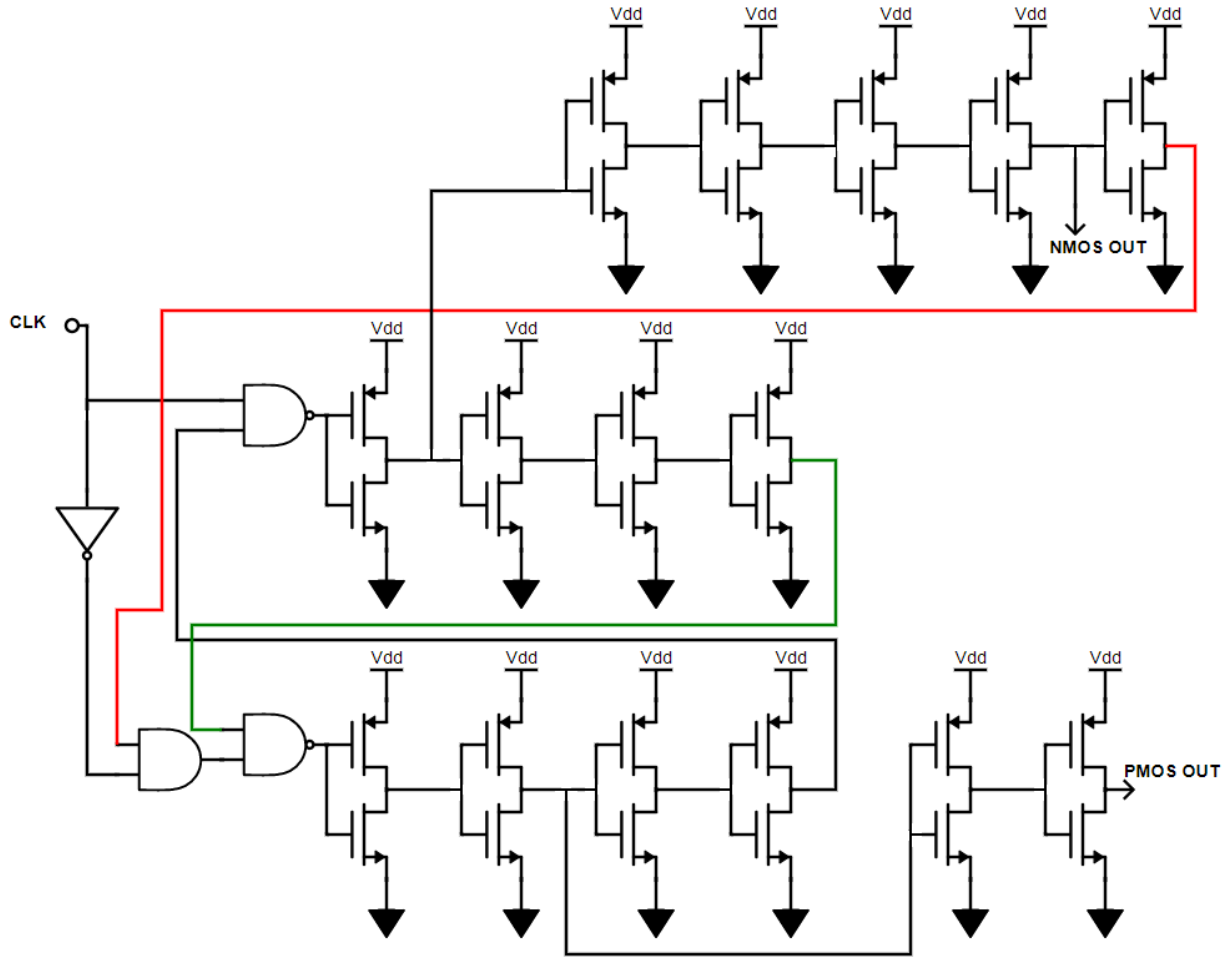


Figure 4.12. A standard topology for generating two non-overlapping clocks for the NIBBC to eliminate any time where the power NMOS and PMOS would be on and conducting at the same time. The clocks from this circuit drive the inputs of the gate drivers for the power switches.

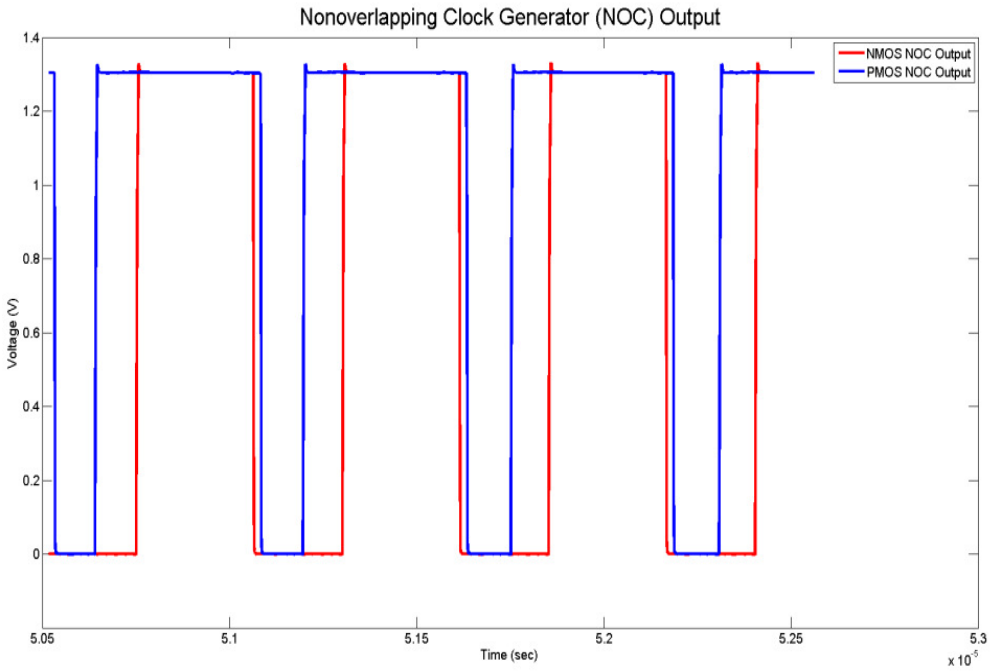


Figure 4.13. The simulated waveforms of the non-overlapping clock generator in Fig. 4.12. The PMOS Output signal rises first in response to the input signal rising before allowing the NMOS output to rise. Conversely, the NMOS output falls in response to a falling input before allowing the PMOS output to fall..

4.14 PFM

PFM converters specialize in light load conditions primarily due the ability to let the inductor completely discharge into the output capacitor of the converter if necessary, while waiting for the output voltage to return to the desired regulated level. This happens frequently at light output currents due to the minimum amount of charge from the inductor with each pulse width necessary to increase the output voltage on the capacitor to the desired level. As such, the voltage will overshoot by some amount but not have the time to settle back below the desired level prior to the next pulse incoming. In PFM , this state results in no pulses being sent to the power switches until the output returns to the regulated level. While in this state, in buck mode, the inductor discharges from ground to the output load as the output level decreases. In boost mode, the inductor discharges from the input voltage source to the output load as the output level increase. If inductor charge is expended, the output will decrease until the next cycle.

In an ideal scenario, the inductor completely discharges at the exact moment in time that the output level falls exactly to the regulated level, and another pulse is sent on the next cycle to

the power switches. However, this is rarely the case as the inductor may completely drain before the output has dropped to the regulated level. In this case, if left unaddressed, the output capacitor will begin to source current into the inductor in the opposite direction to ground in the buck mode or back to the input in boost mode. This reverse charge build up on the inductor must then be overcome before beginning to charge up in the next cycle, resulting in severe efficiency losses as well as potentially preventing proper regulation of the output voltage. To prevent this, a ZCD is implemented to detect this point at which current flow ceases to be positive in the inductor towards the output, becomes zero momentarily, and then reverses to have current flow away from the output. This zero point must be quickly detected, and then the output side power PMOS must be turned off to prevent the output capacitor from reverse charging the inductor. In boost operation, the voltage drop across the output side power PMOS is measured, and a ZCD is detected when this voltage crosses over zero, indicating a current direction change. In buck mode, the voltage drop across the input side power NMOS is measured, and a ZCD is detected when this voltage crosses over zero, indicating a current direction change.

4.15 ZCD Design

The design of a ZCD must contain a few key elements: low power consumption, quick detection speed, and PVT insensitivity. Because power consumption and detection speed are direct tradeoffs that must be decided up on CMOS design, a robust ZCD should be able to be scalable to the needs of the individual converter. While in PFM operation, this detection can be over the course of a longer period as the inductor slowly discharges during a period longer than a few clocks, as shown in Fig 4.14. In addition, if the converter is being pushed to its limits in terms of conversion ratio in a given bin or in terms of output current, PWM a ZCD must also operate effectively faster than one clock period, which is much faster than in PFM mode. This example is shown in Fig. 4.15. In lower power designs, the ZCD needs to consume less power at the cost of inefficiency loss in the ZCD detection speed, and at high speeds, more power consumption in the ZCD can be afforded to ensure quick detection speed. Many scalable designs include a high speed amplifier circuit to quickly detect zero crossings [28-31]. Many of these designs have high power needs and are less suitable to converters with both light load detection and pulse widths that are too long, like the presented work in this thesis. In addition to common amplifier topologies, some works utilize resonant switching [32]. These designs work well at

specific, known frequencies of operation to allow for the filtering and pass elements involved to operate. However, in converters like the NIBBC presented, the frequency component of the converter changes with operation considerably. If not at light load, the frequency component is relatively close to 1.8MHz, but when light load operation begins, the frequency is set more by the discharging rate of the inductor and output capacitor as the converter waits to begin another cycle. This can result in cycle periods lasting multiples of the base clock period. For this reason, resonant ZCD's are not considered. Additionally, topologies involving estimating the correct amount of delay between the inductor beginning to discharge and the zero crossing point are capable of eventually determining zero crossing with reasonably good speed and low power. However, these designs rely on having multiple charge and discharge cycles to search for and calibrate for this correct amount of delay, where the accuracy is related to the resolution of the search and delay elements. These designs have the shortcoming of assuming that both the input voltage, output voltage, and output load will all remain reasonably constant over the course of operation [25, 33-35]. In the case of the wirelessly powered implantable device, the output voltage and current demands can change on the order of microseconds, and the input voltage can change on the order of hundreds of microseconds based on the wireless power's rectifier settling times due to animal motion in the powering environment. As a result, these approximation schemes with delay calibration element are not considered either. In some designs, the ZCD circuits presented are only applicable in buck converters where much of the circuit could not be reused or shared with the boost converter's ZCD [36, 37]. Finally, there are a few designs based loosely around trying to combine amplifier topologies with power saving measures [29]. These designs are considerably prone to PVT variations as they rely largely on the input trip point of an inverter as the main detection method.

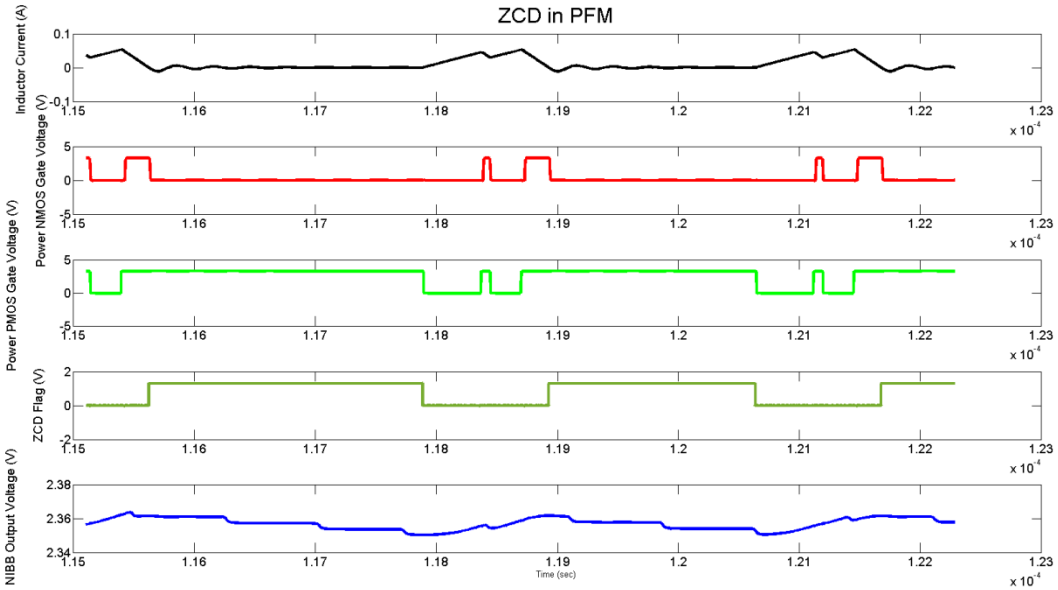


Figure 4.14. Proper buck operation of the ZCD in PFM mode. Upon two cycles of charging and discharging, the inductor is allowed to discharge to 0mA, prompting the ZCD flag to rise. The power NMOS is put in cutoff until the converter output falls to the desired regulated level.

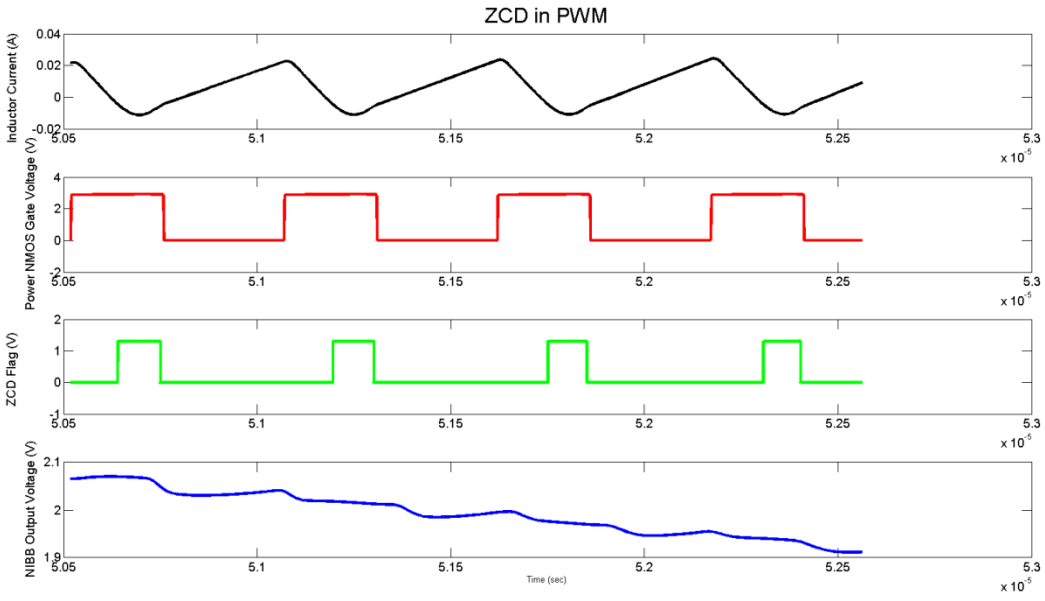


Figure 4.15. Proper buck operation of the ZCD in PWM mode. In each cycle of the charging and discharging, the inductor discharges completely, and a zero current flag is thrown.

With the aim of attempting to create a low power, high speed, process insensitive ZCD that also is able to detect zero currents in both buck and boost mode, a level-shifting amplification topology is designed. In the case of buck conversion, the input side of the inductor is compared against ground. Should this node's voltage rise above ground, a zero current is detected. For boost conversion, the voltage on the output side of the inductor is compared against the output voltage of the converter. Should the output side of the inductor ever have a greater voltage than the output voltage of the converter, a zero current is detected. Keeping the power consumption of the buck detection low is simpler than minimizing the power consumption of the boost detection as the buck detection is sensing a voltage near zero and can use the 1.3V LDO for its supply in the amplifier. However, in the boost detection, the highest voltage in the system, up to 3.3V, needs to be detected. This, in general, results in the output of the converter being used as the supply in detecting its own voltage, which presents power consumption and accuracy challenges. In addition, these two restrictions in each mode would require that two separate circuits be designed and used for the detection of each, which consumes more area and more power to run both circuits. In many works, the ZCD for both the buck and boost modes are the same as a boost converter's ZCD [39]. While this does save space by using most of the converter for both cases, aside from some logic and controls, this does consume more power, as the boost converter ZCD must compare much higher voltages and run of much higher supplies for at least part of the comparison. For this reason, it is desirable to have a ZCD that can reuse much of the circuit for both modes, while still being able to do the buck mode detection from the nodes at approximately ground voltage.

In an effort to save area by combining part of each circuit together as well as use the 1.3V LDO supply for both detection circuits, analog level shifting amplifiers are used. The buck detection level shifting amplifier translates the voltage near ground up to approximately 700mV, PVT dependent. The boost detection level shifting amplifier translates the voltage at the highest voltage in the converter down to approximately 700mV. After the two level shifting amplifiers, the outputs of each are multiplexed into a two state differential cascode amplifier and buffered at the output. In this manner, only one lower voltage, higher speed amplification stage is required for the two detection circuits. The circuit is presented below in Fig 4.16. The top left of the circuit is a common gate amplifier with current mirror to level adjust the boost voltage down; the

bottom left of the circuit is a common gate amplifier with current mirror to level adjust the buck voltage up.

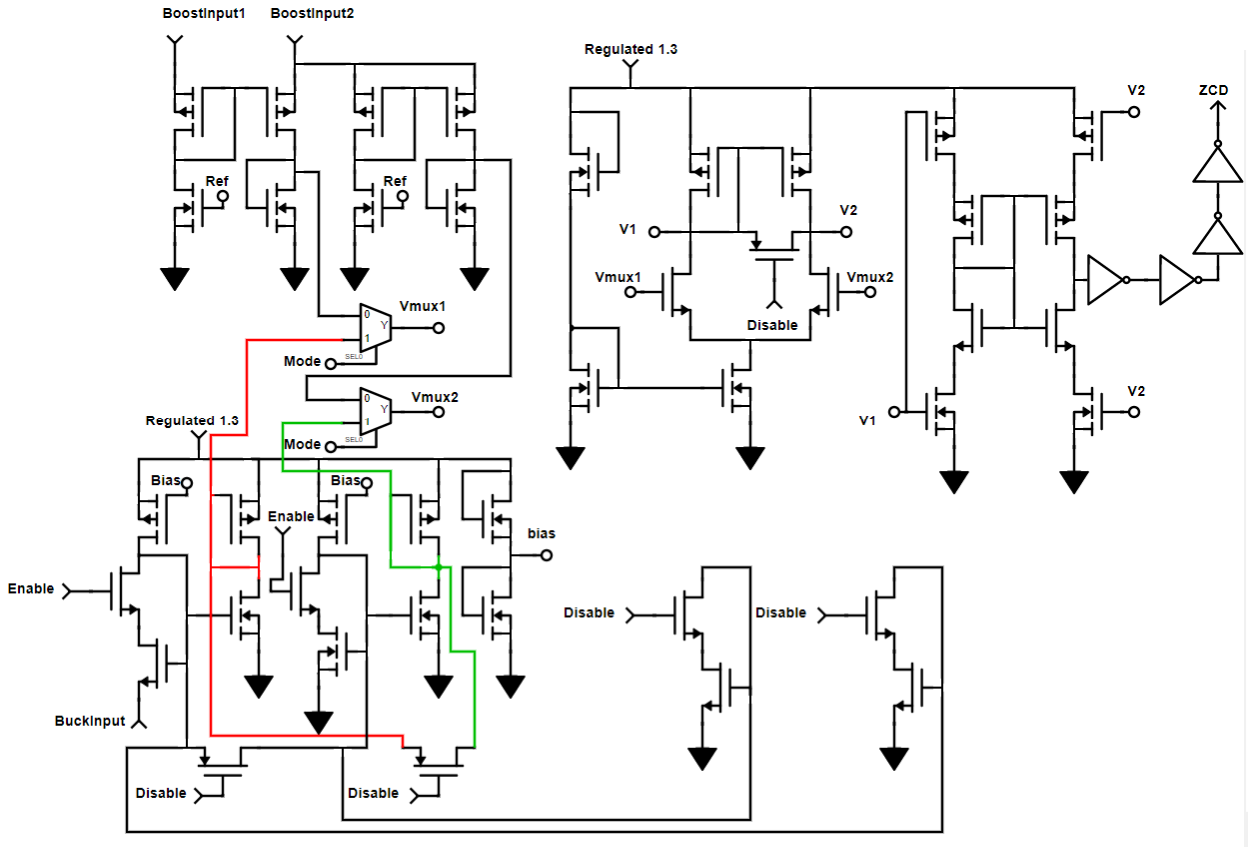


Figure 4.16. The full ZCD circuit for both buck and boost. The boost input is a common gate based level shifter, multiplexed with the common gate based level shifter for the buck input. The two circuits feed into a standard differential stage with cascode amplifier output stage.

In the buck case, there is a particular issue where extra complexity is required. Because of the non-overlapping clock signals discussed previously, there is a period of time when both the power PMOS and NMOS are off before the discharging cycle in the buck conversion, resulting in an inductor with no low impedance path with which to discharge to. This situation causes the inductor to force the input side of the inductor to have a voltage of hundreds of millivolts below ground in an effort to force current up through the schottky diode in parallel with the NMOS buck power switch shown in Fig 4.4. This quick drop in voltage transiently pulls the common gate output voltage of the buck shifter down, forcing the level shifted output (red node in Fig 4.16) up. This in turn quickly sends the voltage at node V_1 much lower and V_2 much higher than steady state. Normally, this would not cause an issue, but the amplifier's speed is

carefully designed to be just fast enough to respond to zero crossings and not drastic shifts in the common mode voltages anywhere in the amplifier input differential stage.

To reduce the effects of this overshoot during the power switch off time in buck mode, an NMOS is placed in series with the input common gate sensing NMOS that connects to the buck node on the input side of the inductor. During any period of conversion where the a zero current detection is not necessary, this NMOS is open circuited (node "Enable" held low during this period, and node "Disable" held high during this period). This reduces the overshoot by limiting the common gate's overshoot to only a result of capacitive conducting from C_{gs} of the sensing NMOS. To prevent the gate of the current mirror from being pulled to the 1.3V supply and also ruining the common mode of the differential amplifier, a same-sized NMOS as the sensing common gate NMOS to the buck voltage is connected in parallel with the common gate circuit. This circuit is only active during the period where zero current detection is not necessary and "Disable" is logic high. Finally, all differential nodes in the circuit are shorted together during the off time to ensure that any rapid changes resulting from the buck input voltage step do not cause the differential amplifier to have long settling times to steady state and causing transient delays in the zero detection.

4.16 ZCD Simulation Results

In this work, the simulated results of the ZCD demonstrate the overall robustness of the design in both buck and boost mode operation. Much of the area of the ZCD circuit is shared between the buck and boost detector via a multiplexer circuit. Each mode detection circuit has a level shifting circuit with minimal gain to provide the shared amplifier with the appropriate common mode voltage range for optimizing gain and power consumption in the shared amplifier. The total area of the two combined circuits takes up $0.00648mm^2$ of space, which saves space over all others work compared to in the literature in Table 4.2 below of same or greater process size. In addition, the detection response time for the amplifier is 7ns for buck detections and 6ns for boost detections, which is on par with the other works. The detection response time improves for fast-fast process corner in both cases, but slows down to 16ns and 19ns in the slow-slow corner for the boost and buck detections, respectively. This relative process insensitivity is done without the need for external trimming, compensation, or detection. In addition, the current consumption when actively detecting a zero crossing is 79uA and 88uA for buck and boost mode,

respectively. While the consumption is higher than the other selected works, the numbers are on the same order of magnitude, and can be reduced down when not actively in use to save power. The strength of this circuit over the others involved is the ability to detect both modes' zero crossings in real time, without the need for external process compensation and while saving on area used. Finally, the circuit is able to measure zero crossings for all input and output voltage ranges as well as all load currents, while instantaneously adapted to transients in the load and line. Many of the selected works utilize a popular method of "searching" for the best amount of time to delay until a zero crossing should occur, based on previous detections of the crossing point. These circuits are unable to adjust for a number of pulse cycles to the correct delay time when load or line conditions change. In addition, circuits utilizing the adaptive delay time may only be capable of calibrating for PWM based zero crossings or for PFM based zero crossings, but not both in many cases. This converter's topology allows for detection in both modes. A transient simulation of the ZCD in boost mode to a 6mV ramp and ZCD in buck mode to a 10mV ramp are shown below in Fig 4.17 and Fig 4.18, respectively.

Table 4.2. A comparison of state of the art ZCD circuits. *Estimated from micrograph

Tag	[37]	[40]	[34]	[28]	[41]	[42]	this work
process	0.13um	0.18um	0.18um	0.35um	0.18um	N/A	0.18um
Topology	Switched Capacitor Comparator	Unbalanced Input Pair Comparator	Adaptive Delay Time Calibration	Common Gate Based Comparator	Fine And Coarse Delay Time Calibration with 100x Clock	Adaptive Delay Time Calibration	Multiplexed level-shifting shared comparator
Current Or Power Consumed By Circuit	40uA	N/A	130uW	50uA	37uA	4uA	79uA buck / 88uA boost evaluating, 26ua buck / 62uA boost precharge
Response Time	10ns	1ns	2ns	20ns	1ns	5ns	7ns buck, 6.5ns boost
Instant Line Transient Response	yes	yes	no	yes	no	no	Yes
Combined ZCD	no	no	no	no	no	no	Yes
Area	.00372mm^2	.05mm^2*	N/A	N/A	N/A	N/A	.00648mm^2
PVT Sensitive	No	no	no	yes	no	yes	No, 2ns / 19ns : ff / ss

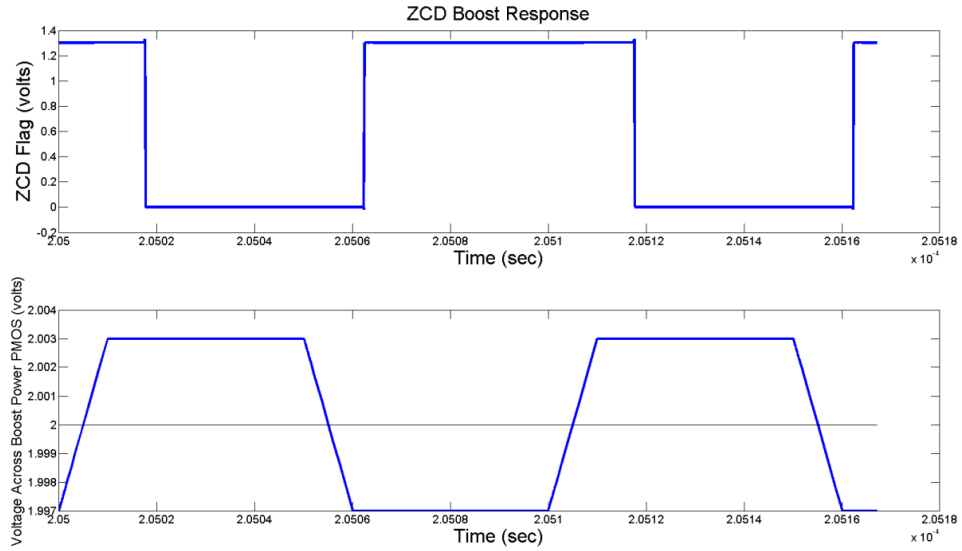


Figure 4.17. The simulated ZCD response to a 6mV ramp signal across the zero current point in a boost mode conversion in the NIBBC

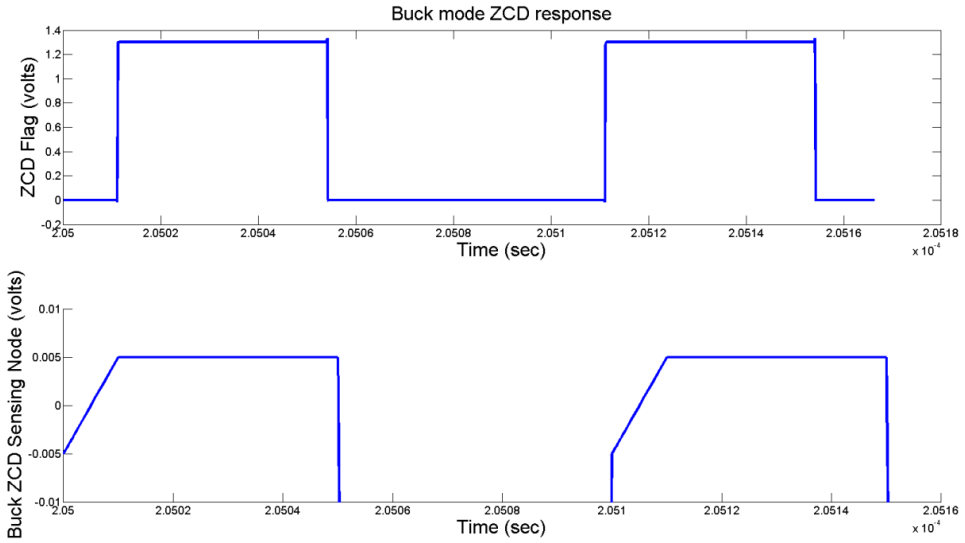


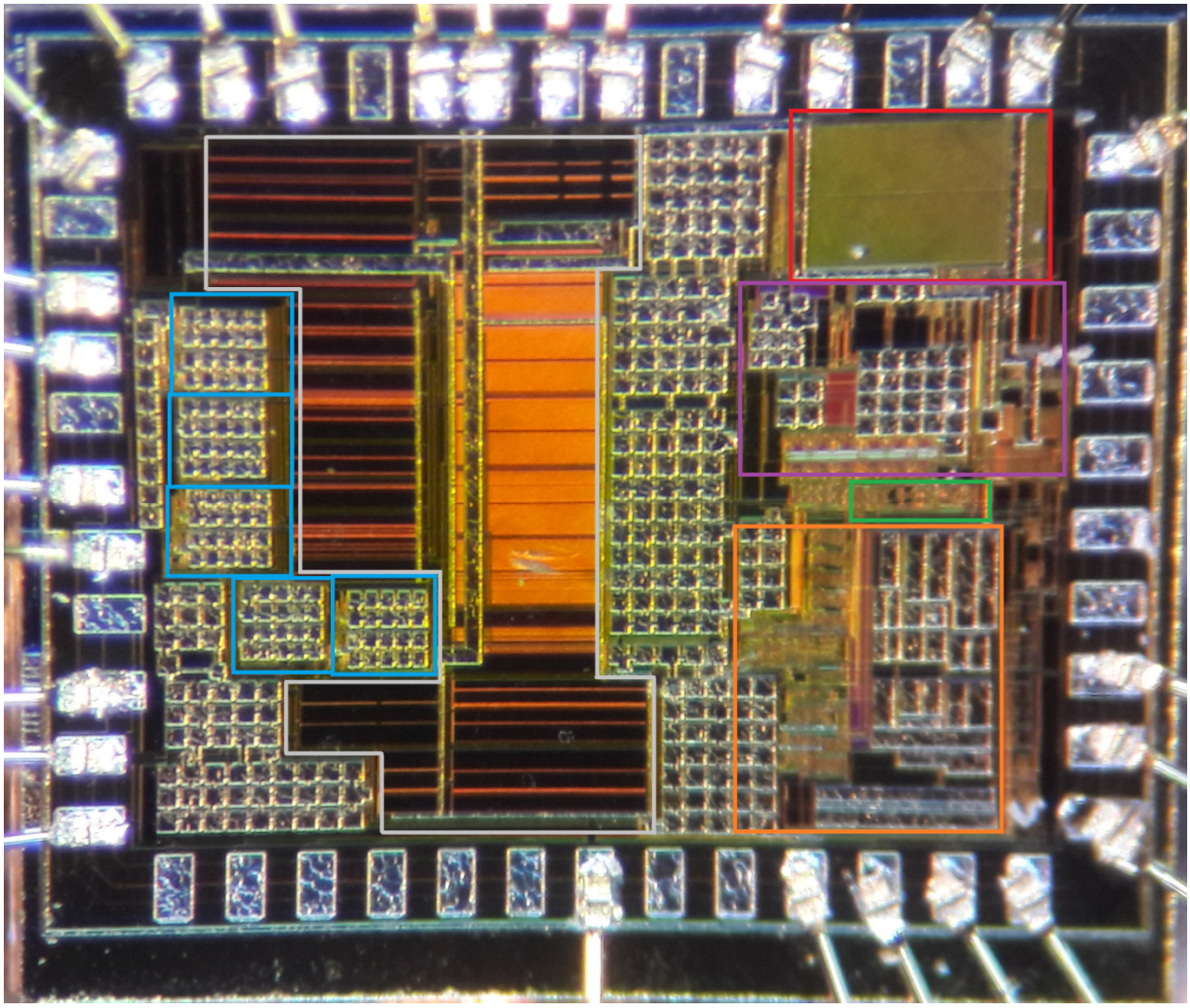
Figure 4.18. The simulated ZCD response to a 10mV ramp signal across the zero current point in a buck mode conversion in the NIBBC

4.17 Fabricated Chip and Measurement Results

The NIBBC IC was fabricated on TSMC's 0.18um MS RF G process and submitted through Muse Semiconductor's service. The physical chip is 1.66mm by 1.33mm in area, and

utilizes 6 metallization layers. Special care was given to placing all differential pair transistors in parallel physically close. The power switches and output regulator take up most of the space on the chip. Excess space on the chip is occupied by ESD protection circuits as well as MOS capacitors stacked with MIM capacitors above. This capacitance is used for the on-chip 1.3V LDO, bandgap reference, HVS supply output, and converter freewheeling capacitor. No capacitors were placed over power switches or sensitive digital circuits to prevent cross coupling. The micrograph of this chip is illustrated in Fig 4.19.

Figure 4.19. A micrograph of the fabricated NIBBC from TSMC's 180nm MS RF G process. The highlighted blue boxes contain the gate drivers, the white box contain the power switches, the red box contains the HVS, the purple box contains the digital core and oscillator and PWM, the orange box contains the input and output binning circuits and comparators, and the green box contains the ZCD circuit. The full chip dimensions are 1.66mm by 1.33mm.



The fabricated chips were tested on the benchtop using an Agilent DC power supply as well as Keysight oscilloscope. An input sensing resistor was connected in series with the input of the converter, and the voltage across the resistance was measured to provide input power measurements. The output of the converter and LDO were measured by the oscilloscope as well with a 2.2uH inductor and 2.2uF output capacitor off-chip. Each mode was tested individually to gather information about all aspects of the converter. The buck mode is tested for input voltages of 3.3V, 3.1V, 2.9V, 2.7V, and 2.5V are various load currents from 1mA to 27mA. These tests

were run with the converter set to output voltages of 2V, 2.2V, and 2.5V as sample operations. The output efficiencies are calculated as the ratio of the output power to the input power and reported as a percentage. These various tests produce efficiencies that are plotted in Fig 4.20, Fig 4.21, and Fig 4.22 below.

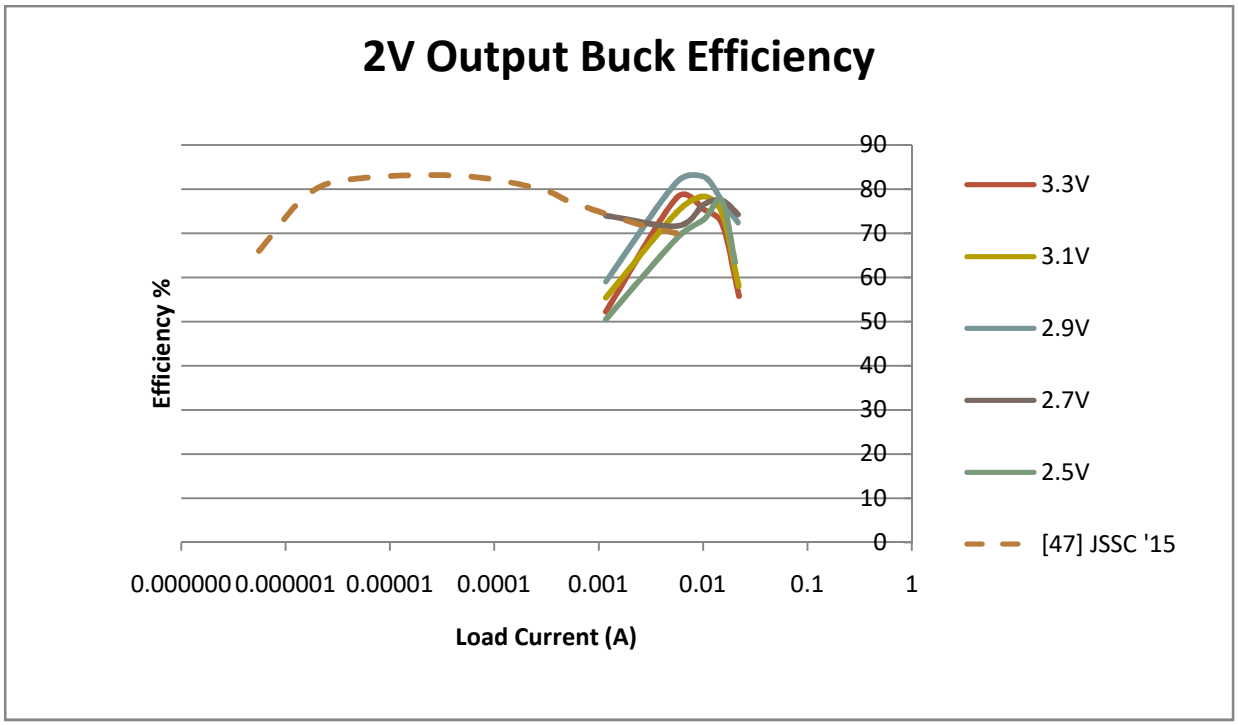


Figure 4.20. Plot of the measure efficiency for 2V converter output in buck mode for various input voltages.

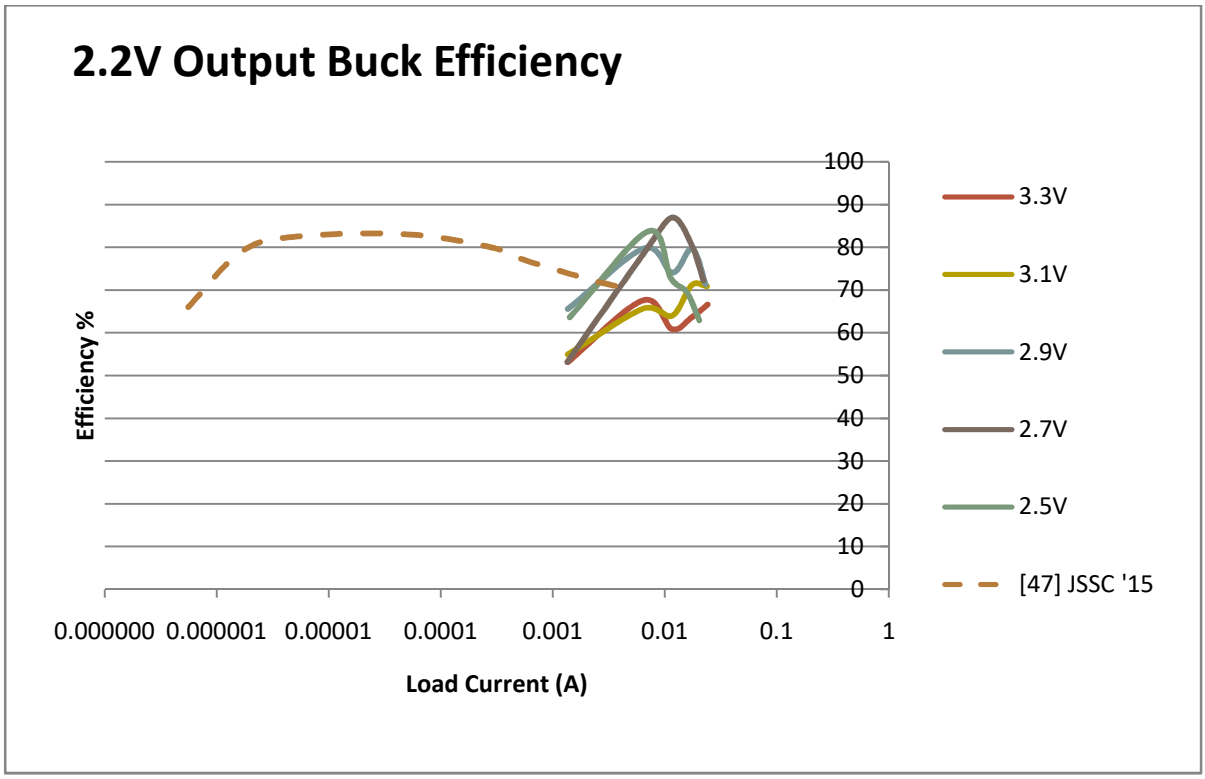


Figure 4.21. Plot of the measure efficiency for 2.2V converter output in buck mode for various input voltages.

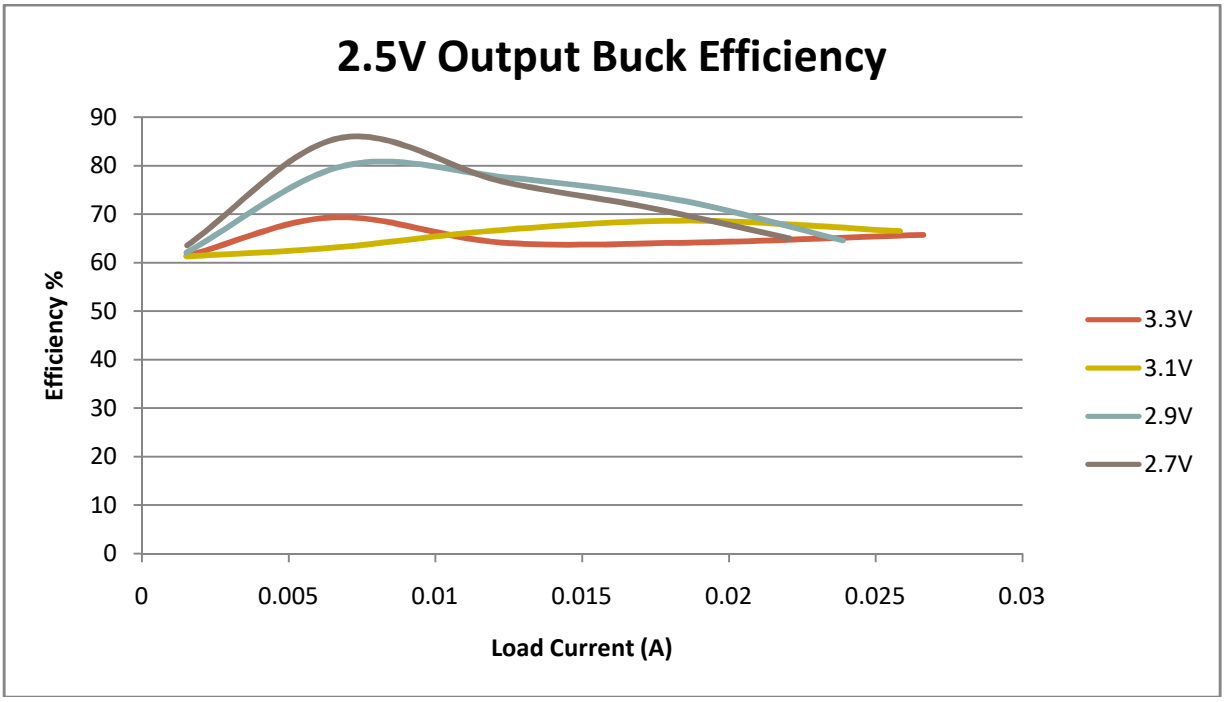


Figure 4.22. Plot of the measure efficiency for 2.4V converter output in buck mode for various input voltages.

The boost mode of operation for the NIBBC was tested in a similar manner for input voltages of 1.6V, 1.8V, 2V, 2.2V, 2.4V, and 2.6V for load currents between 1mA and 21mA. We run these tests with the converter's output set to be 2V, 2.2V, 2.4V, 2.6V, or 2.8V to test all of the operating ranges. These various efficiency tests are plotted in Fig 4.23, Fig 4.24, Fig 4.25, Fig 4.26, and Fig 4.27 below.

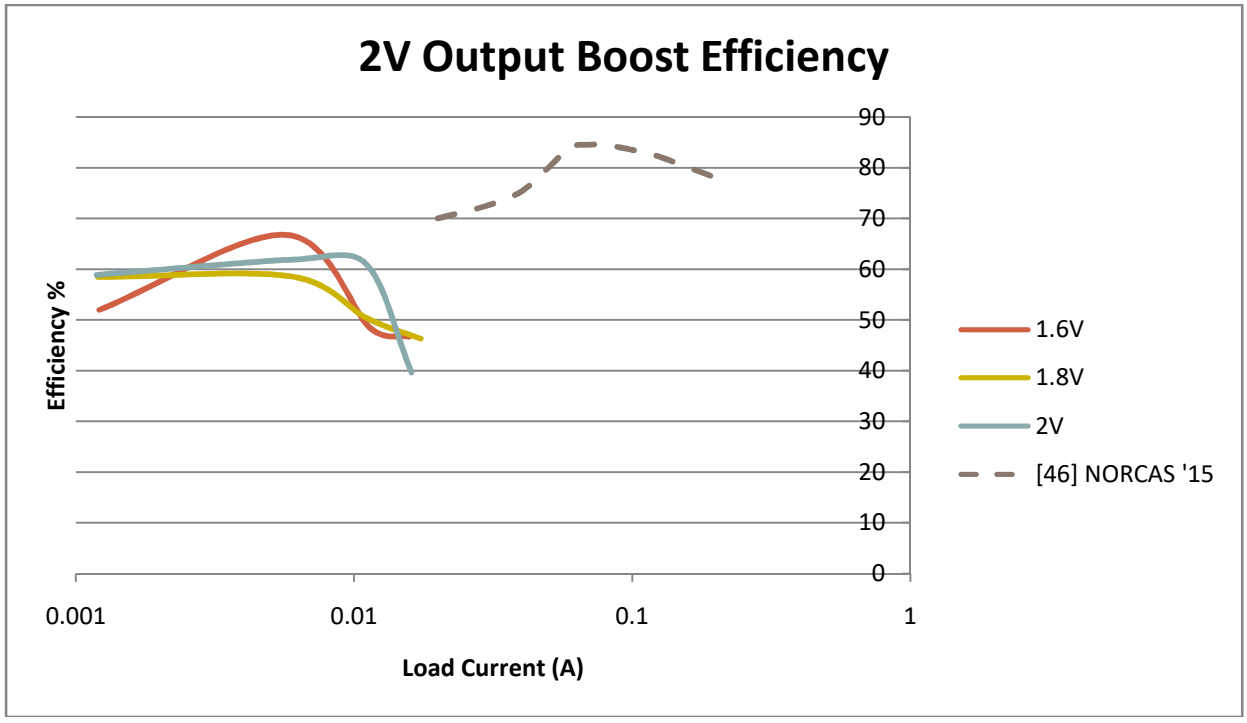


Figure 4.23. Plot of the measure efficiency for 2V converter output in boost mode for various input voltages.

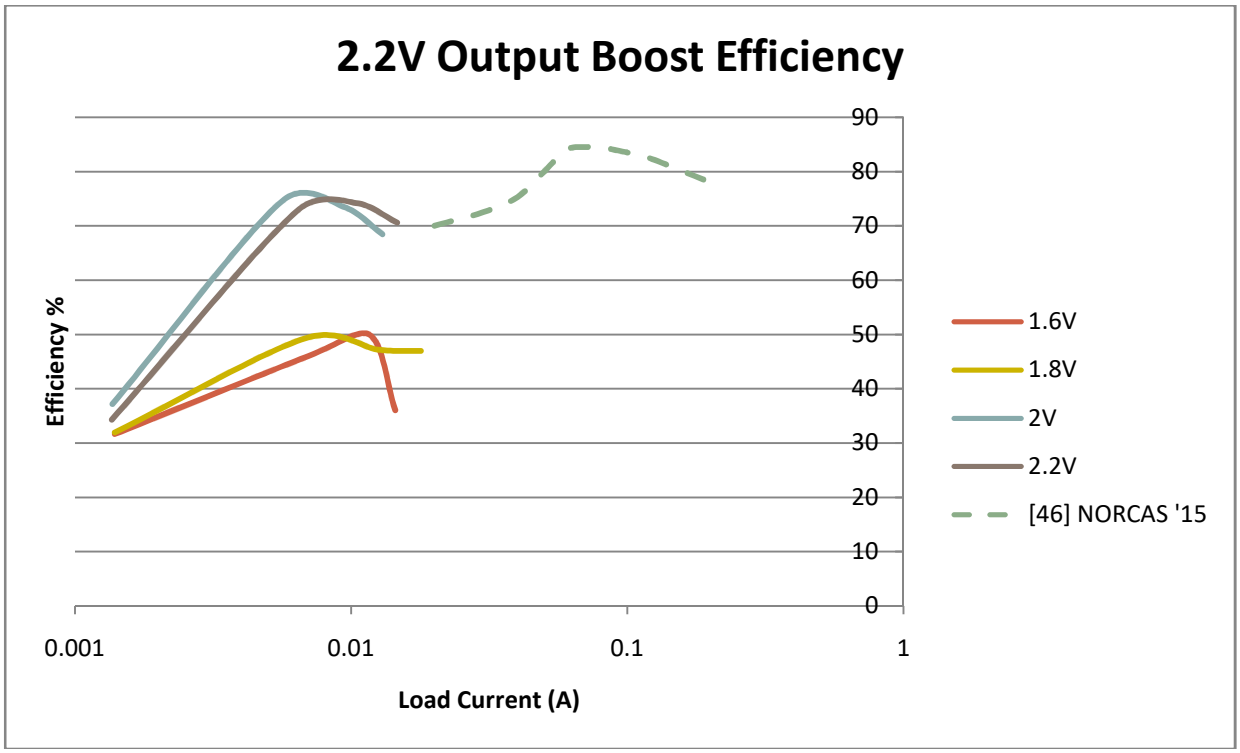


Figure 4.24. Plot of the measure efficiency for 2.2V converter output in boost mode for various input voltages.

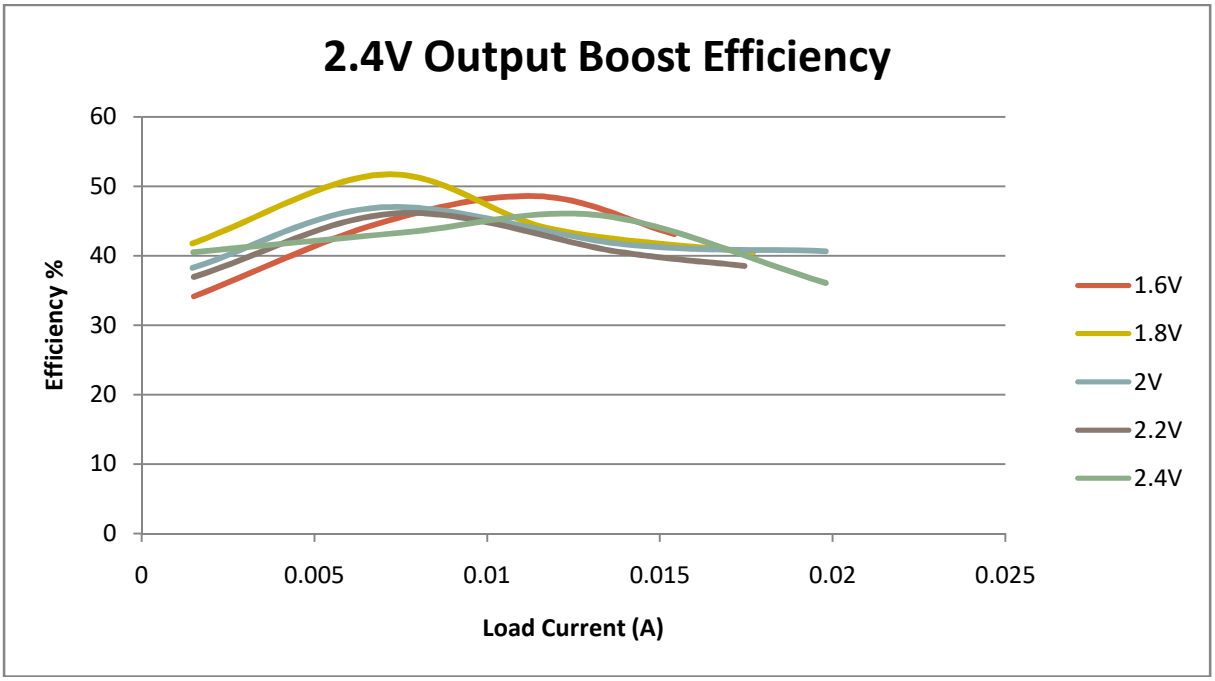


Figure 4.25. Plot of the measure efficiency for 2.4V converter output in boost mode for various input voltages.

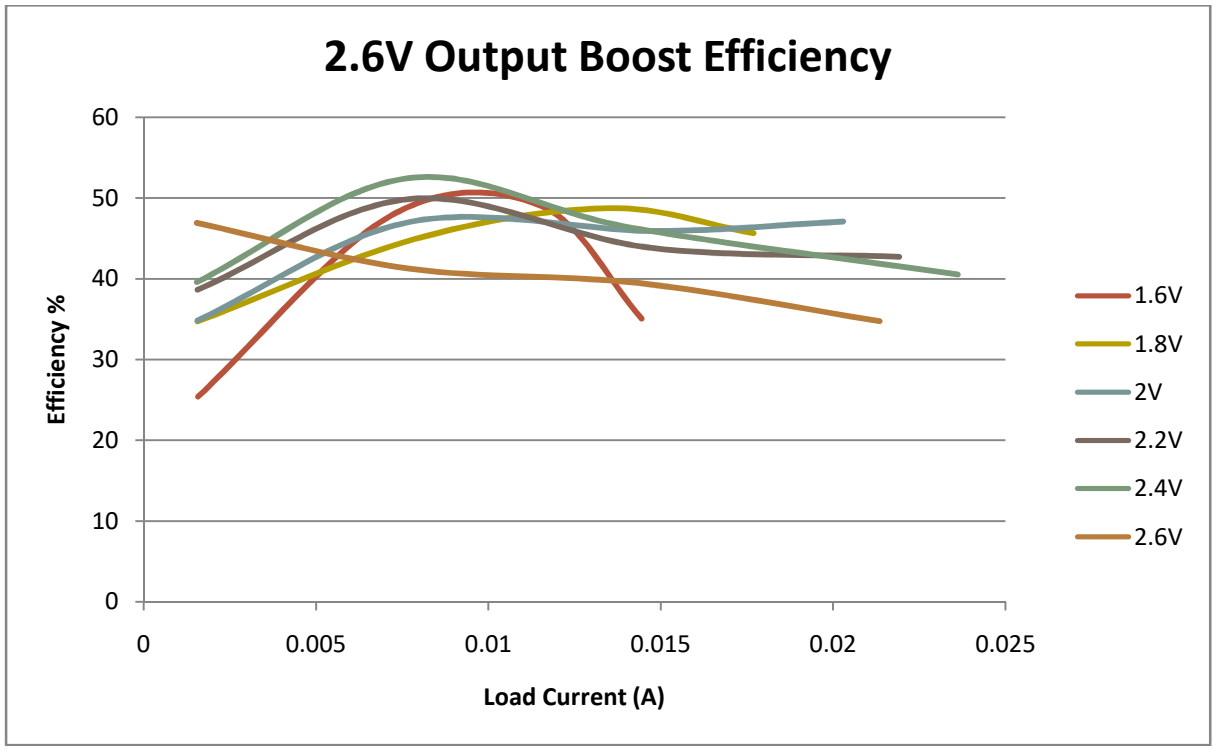


Figure 4.26. Plot of the measure efficiency for 2.6V converter output in boost mode for various input voltages.

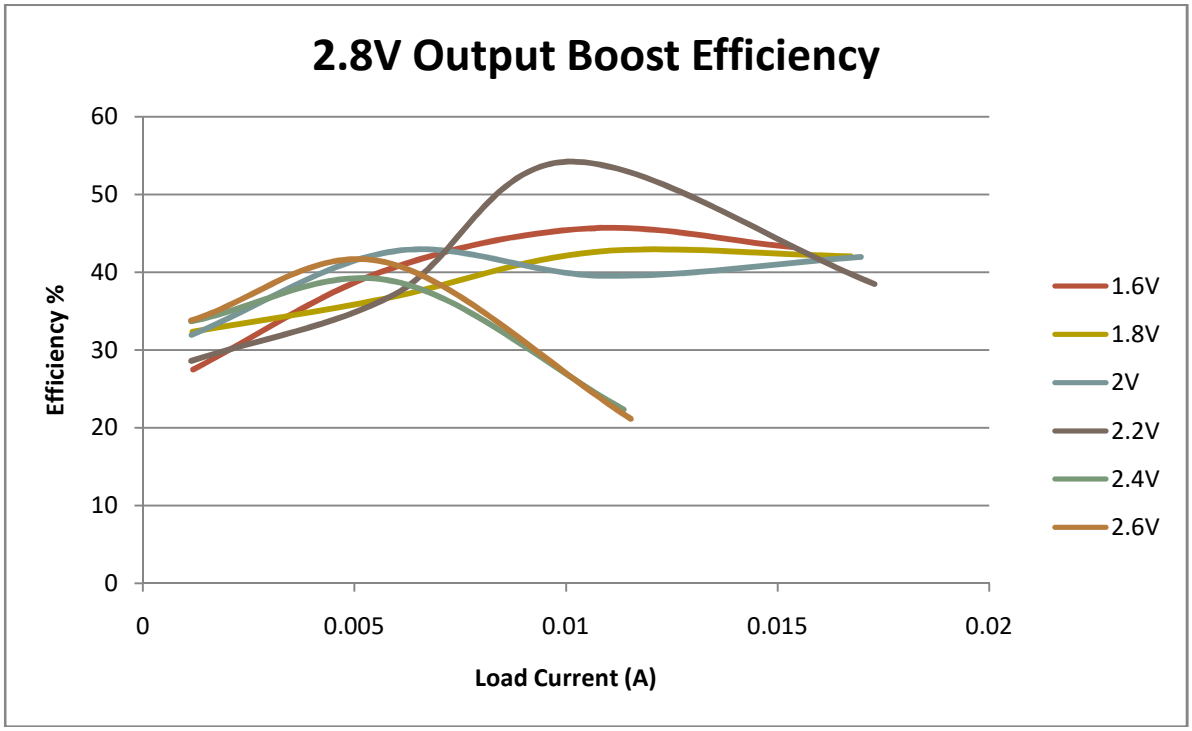


Figure 4.27. Plot of the measure efficiency for 2.8V converter output in boost mode for various input voltages.

The short mode of operation for the NIBBC was tested in a similar manner for input voltages of 3.3V, 3.2V, 2.9V, 2.7V, 2.6V, 2.4V, and 2.3V for load currents between 1mA and 20mA. We run these test with the converter's output set to be 2.1V, 2.4V, 2.6V, and 2.8V to test all of the operating ranges. These various efficiency tests are plotted in Fig 4.28, Fig 4.29, Fig 4.30, and Fig 4.31 below.

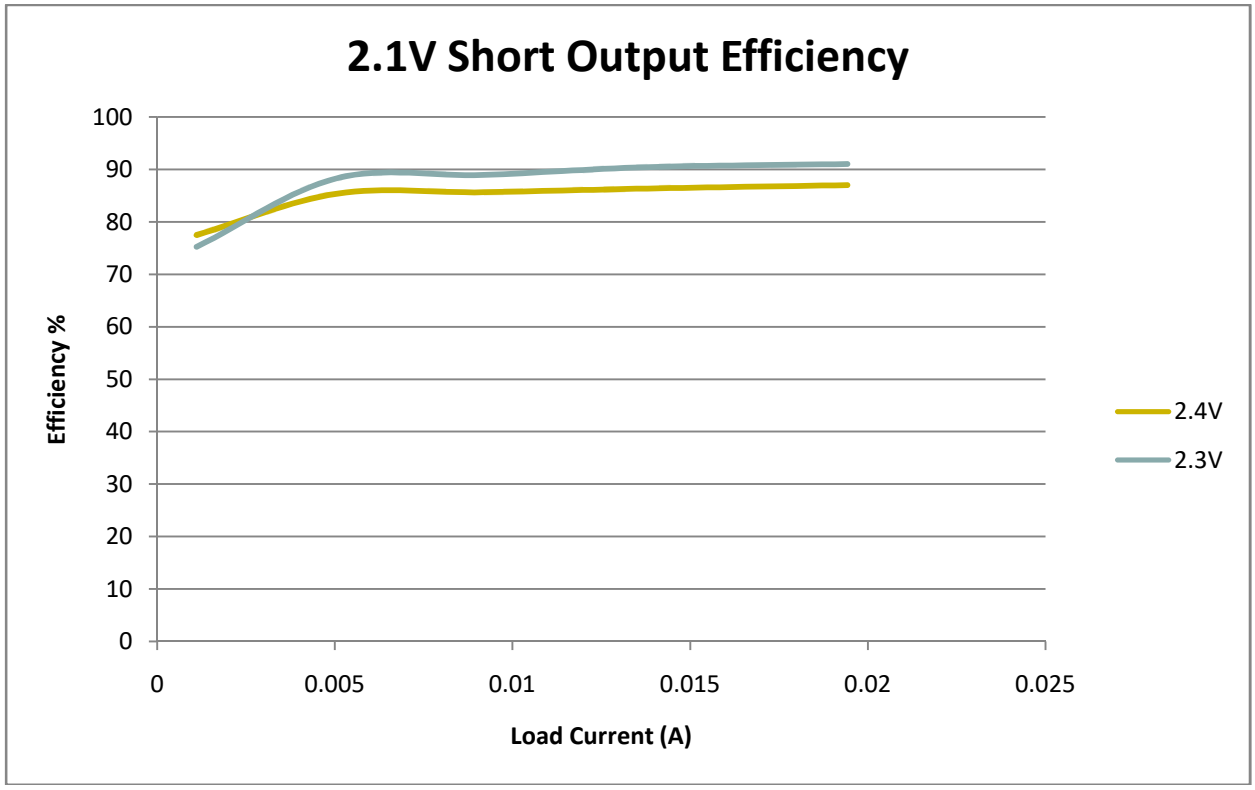


Figure 4.28. Plot of the measure efficiency for 2.1V converter output in short mode for various input voltages.

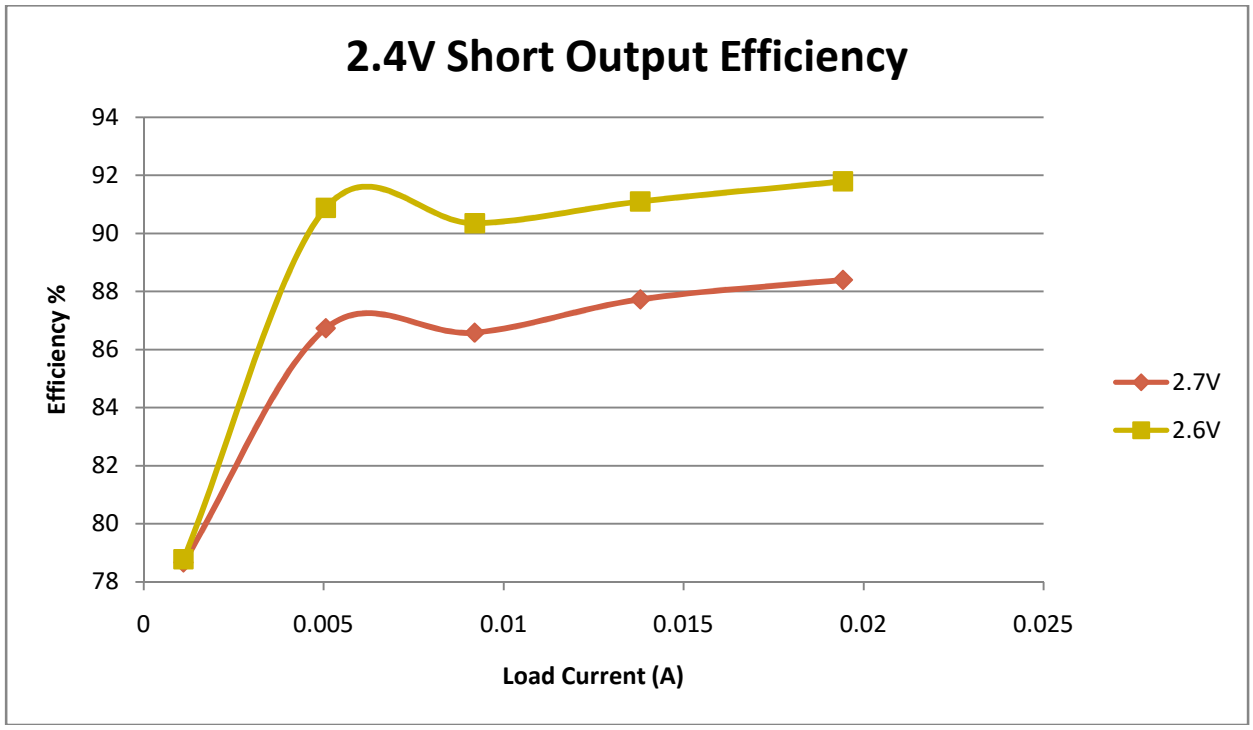


Figure 4.29. Plot of the measure efficiency for 2.4V converter output in short mode for various input voltages.

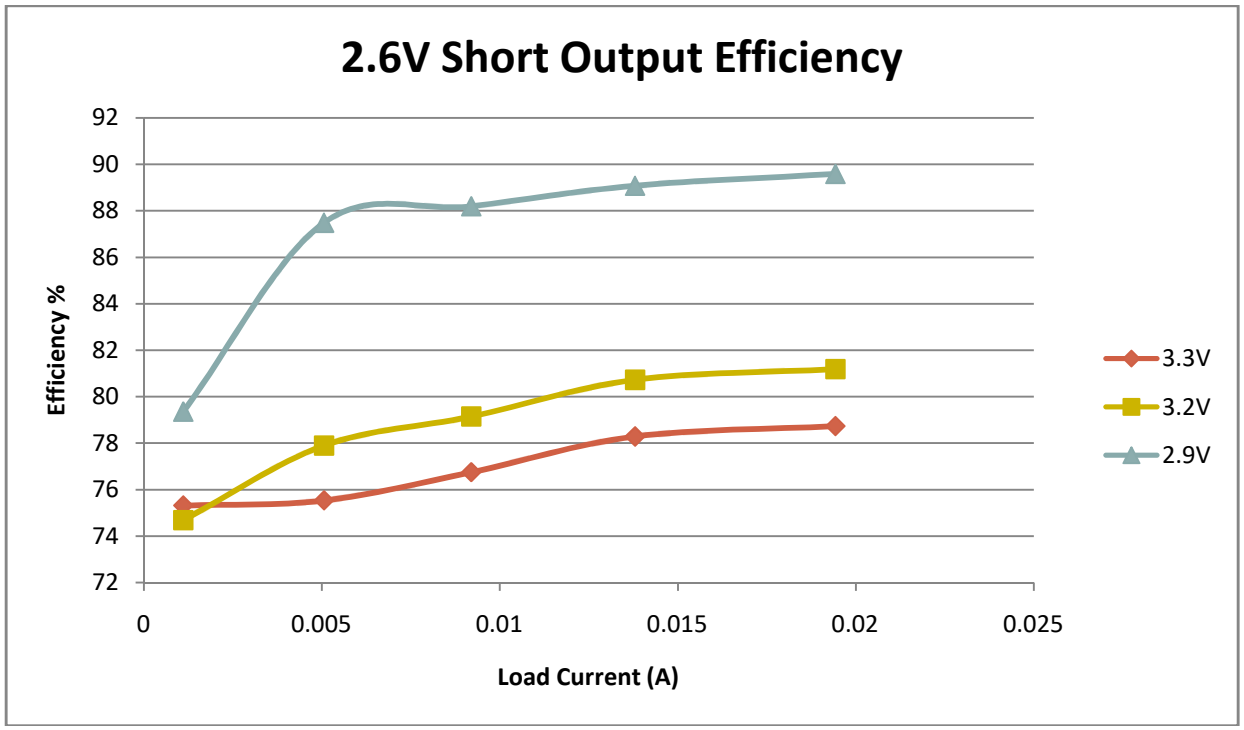


Figure 4.30. Plot of the measure efficiency for 2.6V converter output in short mode for various input voltages.

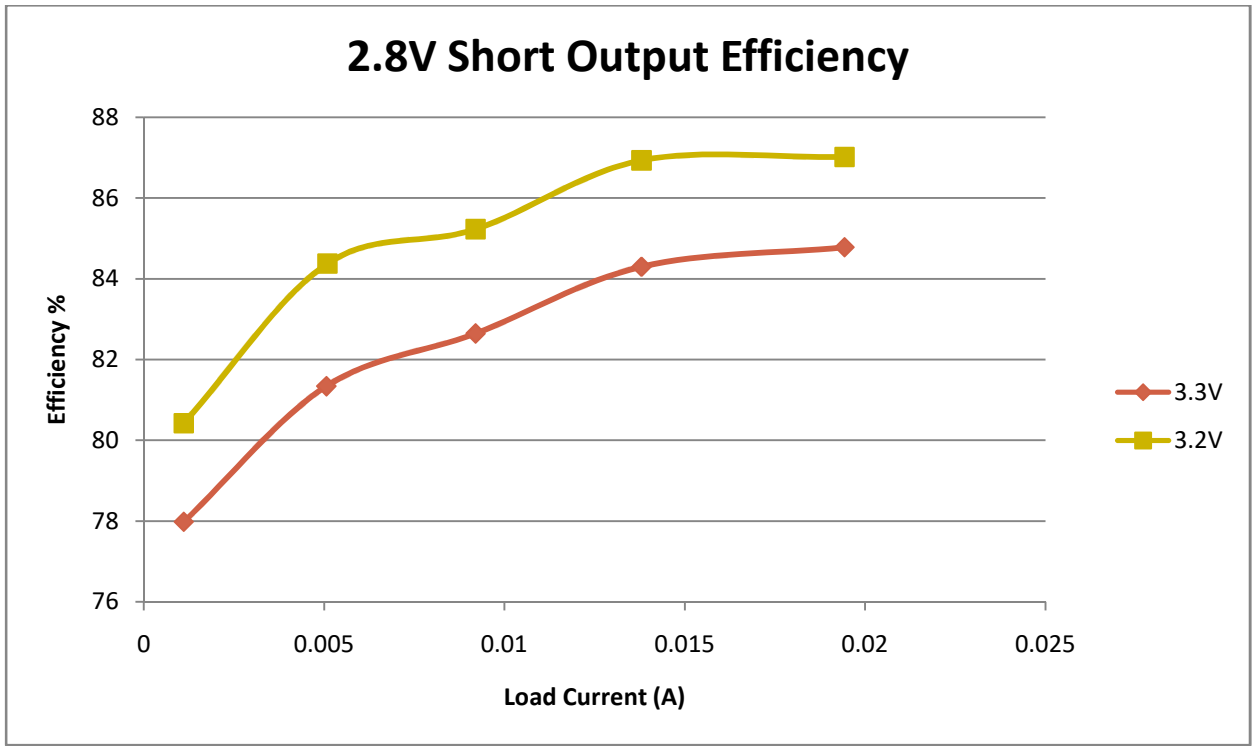


Figure 4.31. Plot of the measure efficiency for 2.8V converter output in short mode for various input voltages.

To test the dynamic ability of the converter and overall topology, a 200mV input step response from 3.3V to 3.1V is applied over 10us, and the output voltage pull-down is measured to be approximately 60mV. In this particular application, a 2.2uH inductor and 1uF capacitor were used. This measurement is obfuscated by the additional ripple and output error induced in the converter by the change in input voltage. If we consider the drop in average output voltage before and after the step response, the total pull-down on the output is no more than 10mV, and normal output regulation resumes within 10us of the step response. An example of this step response is shown below in Fig 4.32 with the step occurring at 395us.

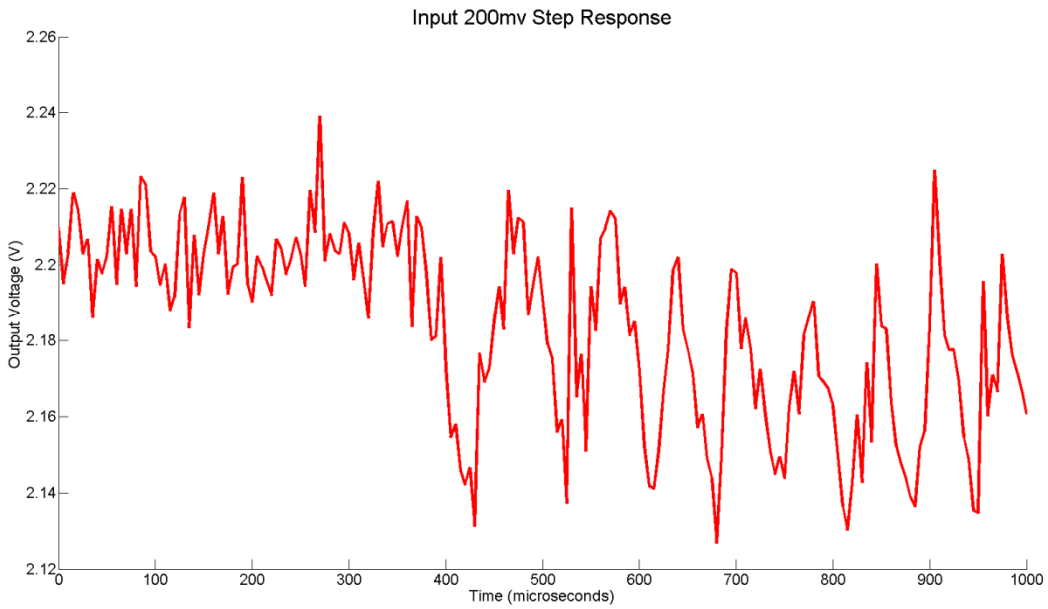


Figure 4.32. Plot of the output voltage of the converter in response to a 200mV step response from 3.3V to 3.1V over the course of 395us to 405us.

In addition to the input step response, the output voltage is measured for a 10us change from 1mA to 25mA in the output current delivered, which can be seen in Fig 4.33. The step produces a change of 50mV in the output voltage before recovering over the course of 5u. Both of the measurements were done with a 2.2uF capacitor. In the input step case, the pull down amplitude is within the actual ripple range of the steady state output voltage post-step, and could be improved if a larger output capacitor is used. In addition, the output step case produces an initial pull down that only exceeds the ripple of the steady state output voltage post-step by about 20mV, and could be improved if a larger output capacitor is used.

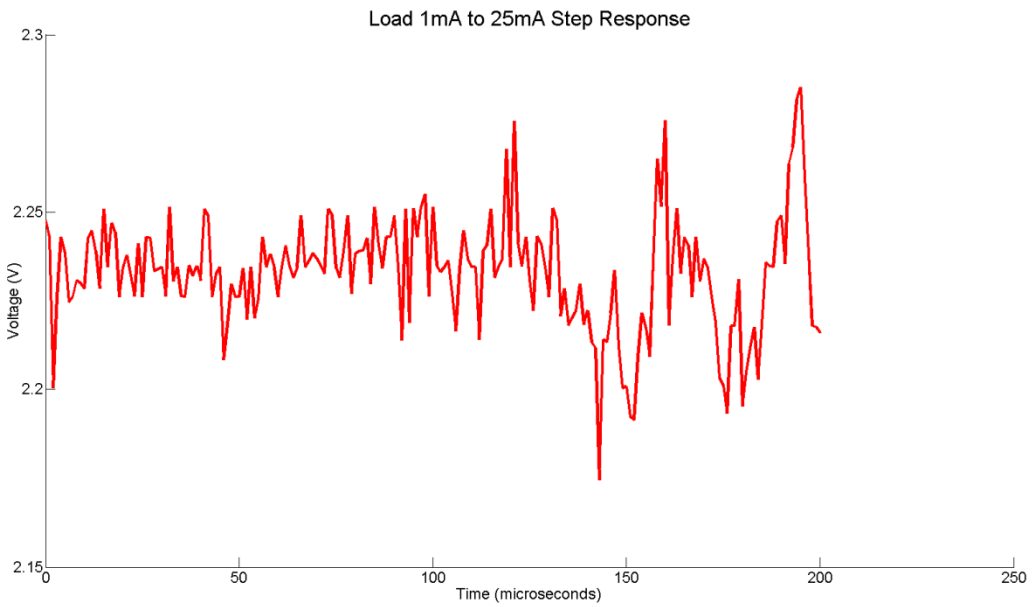


Figure 4.33. Plot of the output voltage of the converter in response to a 24mA output current step response from 1mA to 25mA over the course of 135us to 145us.

4.18 Discussion

The measured efficiencies are lower than in the pre-tapeout simulation results as well as the post-tapeout corrected schematic and layout simulation results across some of the operating modes and regions. The reason for this is a confluence of a few factors discovered post-tapeout.

The primary problem is the circuit's ability to select the optimal operating pulse width in some scenarios. Part of this is the lack of more pulse width options as well as inaccuracies new bin boundaries, which is likely a result of error introduced during the buffers placed between the binning resistor dividers and the comparators. The secondary concern in the circuit's loss in overall efficiency is the amount of body diode conduction during dead time where the inductor is being switched out of the circuit. In these periods of time, the inductor forces the input side node to very negative voltages or very high voltages above the supply in order to discharge through a few different body diode connections. In the post-tapeout simulations, a shunt switch to short out the inductor during these dead times has been added to reduce this effect. In future works, one could further improve the converter by implementing the aforementioned techniques as well as tightening the voltage bins and increasing the number of bins. Currently, due to reduced numbers of pulse widths available to the converter, overshoot of the regulated voltage in boost mode is

common in many operating modes and bins due to PFM operation being required. In boost mode in particular, the time spent in PWM operation compared to PFM should be increased if the cost to the area and power consumption of the ASIC are not increased by much.

Comparing to other NIBBC in the literature, there are few converters of this topology operating in the 1-100mW range. There is much work written on converters in the microwatt range and on converters operating over 100mW. Thus, direct comparisons shown in Table 4.3 below may be close to the range, but don't have substantial overlap. This work fares well in terms of controller size and converter size when compared to converters made on the same size process node or larger. In addition, the converter can handle light loads, while still producing respectable peak power conversion efficiency of 87% in buck mode and 74% in boost mode. In this most common use cases of this converter for a Bionode, the output range is 2.0V to 2.2V for middle current outputs, which is the most efficient operating range of this converter. The converter boasts a wide input and output range, suitable for a variety of battery uses outside of low voltages. Many of the converters below either have set output voltages only, thus limiting flexibility, or have input voltage ranges too low for many wireless implantable devices to operate on full time. A figure of merit (FoM) is generally defined for topologies of various types in integrated circuits and is useful for comparison between various literature works. However, in the works cited in Table 4.3 as well as other works in the literature for NIBBC's, FoM's are not common place, and a FoM is defined as:

$$FoM = (Peak\ Efficiency) * (Input\ Voltage\ Range) * (Output\ Voltage\ Range)$$

From this FoM, a measure of the converter's efficiency and overall flexibility across various inputs and outputs is available to characterize and compare across works. From this FoM, this work's converter is 5.3% higher than the nearest work's FoM, demonstrating the goal of creating a converter that has all of the required functionality, while delivering good efficiency for various input and output scenarios.

Table 4.3. A table detailing the state of the art in NIBBC topologies from various process nodes. *estimate from Photovoltaic cell range and LiPo Battery Range, ** estimate from specifications, *** estimate from micrograph, ****estimate from plots

Source	[43]	[44]	[45]	[46]	[39]	[47]	This Work
Process	0.35um	0.25um	0.35um	0.18um	28nm	0.18um	0.18um
Load Power	33mW-1320mW**	165mW-1650mW	600mW boost, 1200mW buck maximum	18mW-420mW****	1uW-60mW	1mW-10mW	1.8mW-100mW
Controller Area	2.32mm^2***	0.88mm^2***	1.6mm^2**	0.558mm^2**	.053mm^2	1.156mm^2	0.5mm^2
Total Area	3.86mm^2	3.14mm^2	4.108mm^2	2.31mm^2	0.5mm^2	4.62mm^2**	2.207mm^2
Peak Efficiency	98.1% heavy load / 80.4% light load	96% heavy load	92% heavy load	88% buck / 84.5% boost	89%	83%	74% boost / 87% buck
Input voltage	2.5-5	2.7-4.5	2.3-5	0.9-2.2	0.2-1	1,1.5,1.8,2.5	1.5-3.3
Output voltage	3.3	3.3	3.3	0.9-2.2	0.4-1.4	1,1.8,3	1.8-3.3
Output Ripple	20mV	10mV	40mV	10mV	15mV-30mV	30mV****	50mV without LDO
FoM	2.4525	1.728	2.484	1.0648	0.712	2.49	2.6622

4.19 *In Vivo* Test of Device

To confirm proper operation of the device for the intended application of bio-signal acquisition *in vivo*, an acute surgery on a 300g Long-Evans rat involving a patch electrode placed around the host's stomach. Electrogastrogram (EGG) signals were acquired with aforementioned bio-signal acquisition circuits on the Bionode. Regulated power was provided to the Bionode by the NIBB from this work. Five measurements were taken. The first measurement involved forcing the converter to operate in boost mode only while using wireless power from a near-field two-coil power transfer setup and rectifier. The converter outputted a regulated 2.1V, and the

plot of the electrogastrogram is demonstrated in Fig 4.34 below. To clean up the signal for proper characterization of stomach motility, a three second moving window average filter was used and presented in Fig 4.35. In addition, the NIBB was used with a wired wall power supply of 1.8V and the same measurements are plotted, shown in Fig 4.36. This was done to compare noise levels in the acquired signal between the wireless power application and a more stable supply. Similarly, the moving average filter was applied to the data and improved in Fig 4.37.

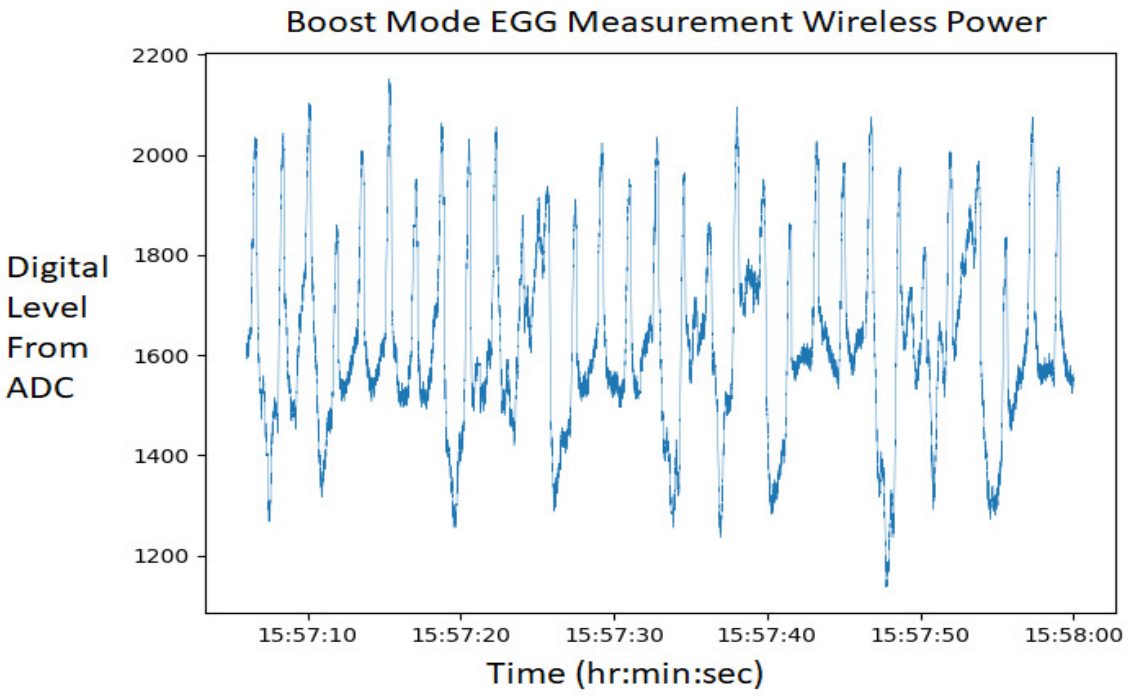


Figure 4.34. Plot of EGG in a rat with 12-bit ADC on Bionode operating from boost mode NIBB powered by wireless power.

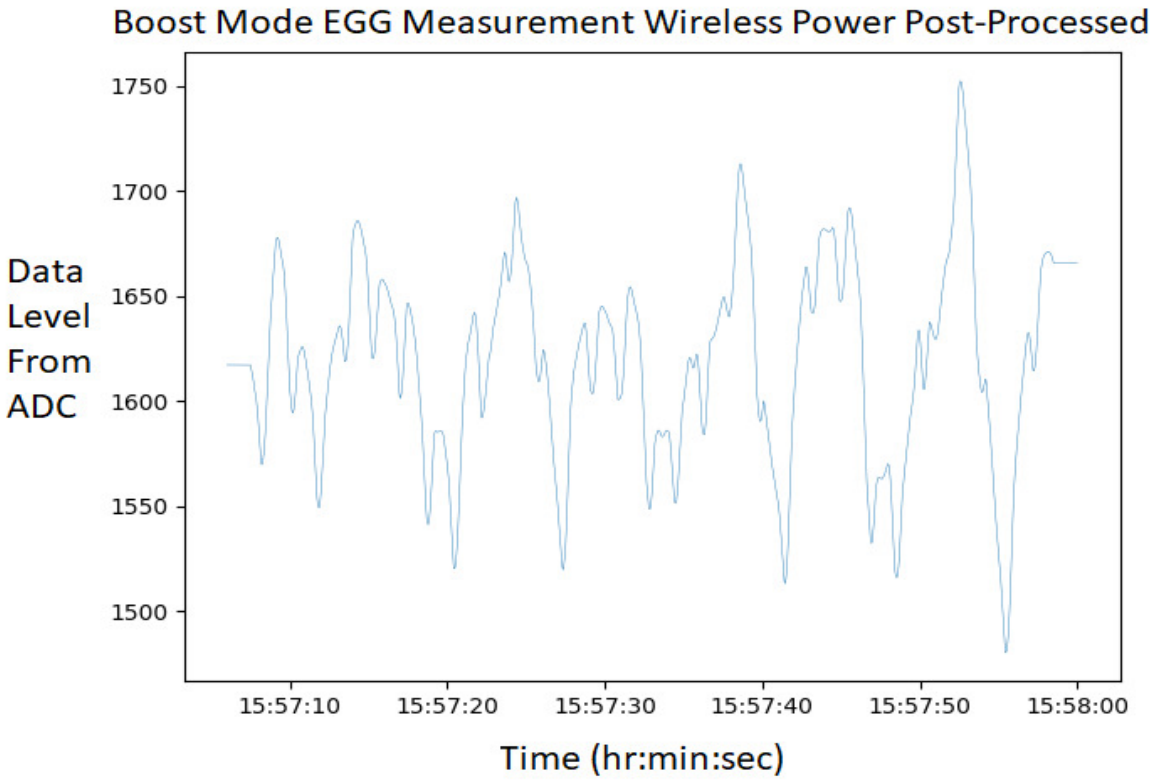


Figure 4.35. Three second moving window average filter of EGG from data in Fig 4.34.

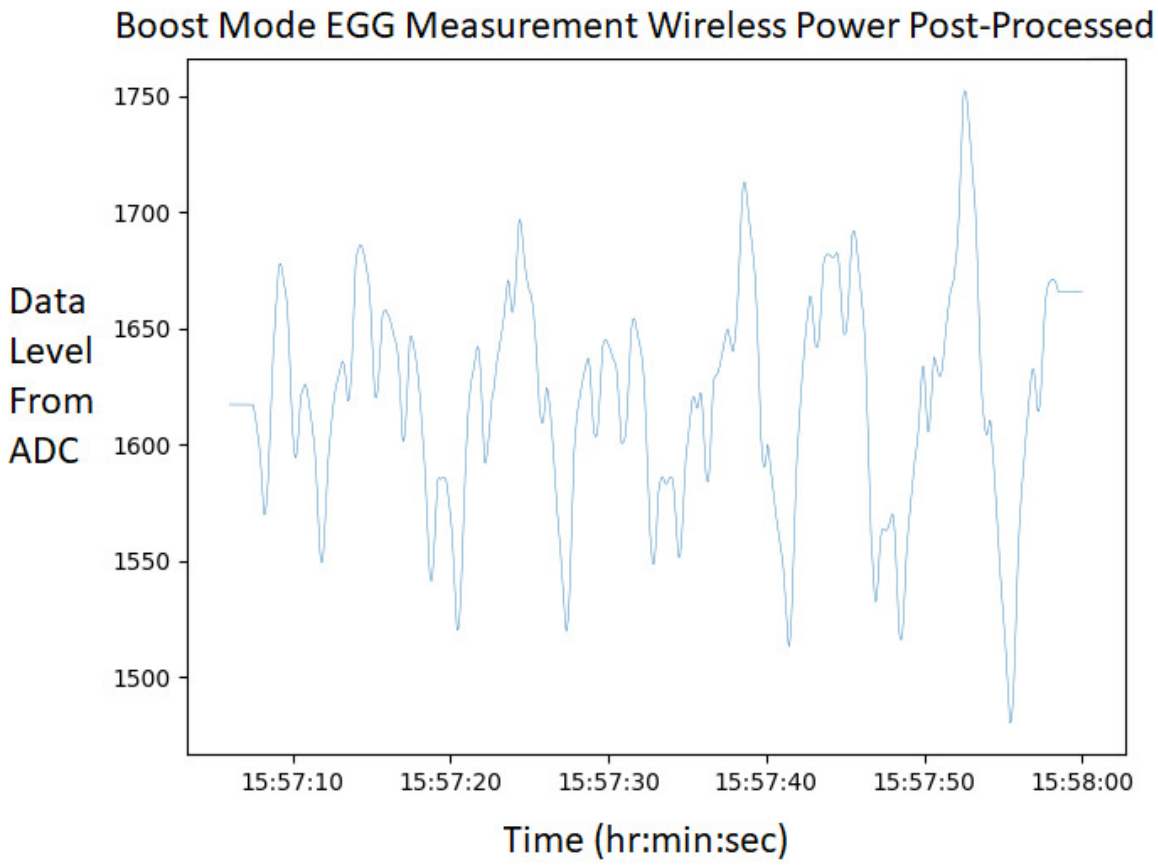


Figure 4.36. Plot of EGG in a rat with 12-bit ADC on Bionode operating from boost mode NIBB powered by wired wall supply power.

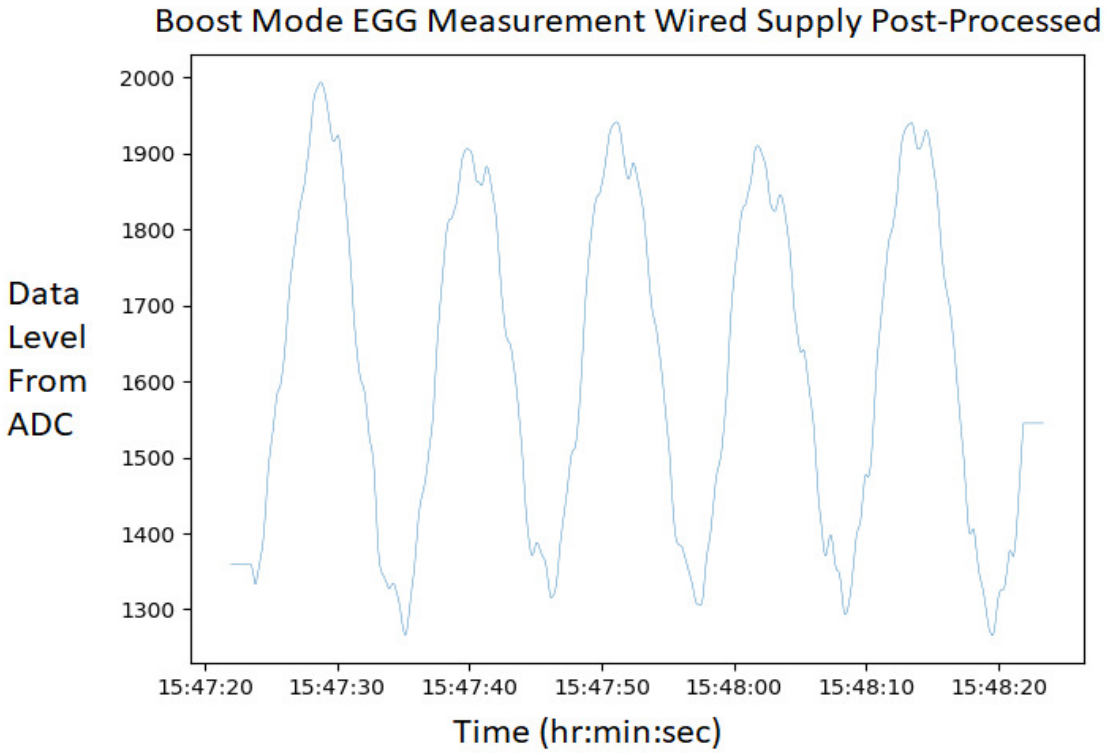


Figure 4.37. Three second moving window average filter of EGG from data in Fig 4.36.

To verify proper buck operation, the NIBB was then forced into buck operation only; the experiment was repeated with the NIBB operating from a 3V lithium rechargeable battery, and the data is plotted in Fig 4.38. As in the previous set of plots, a moving average filter is used to characterize the motility and demonstrated in Fig 4.39. Next, the measurement was repeated with the NIBB operating in buck mode, powered by a wired wall power supply of 3.3V, with the measurements illustrated in Fig 4.40. The moving window average filter is applied once more and plotted in Fig 4.41. For all of the measurements performed, a 2.2uH inductor and 2.2uF output capacitor were used off-chip with the converter.

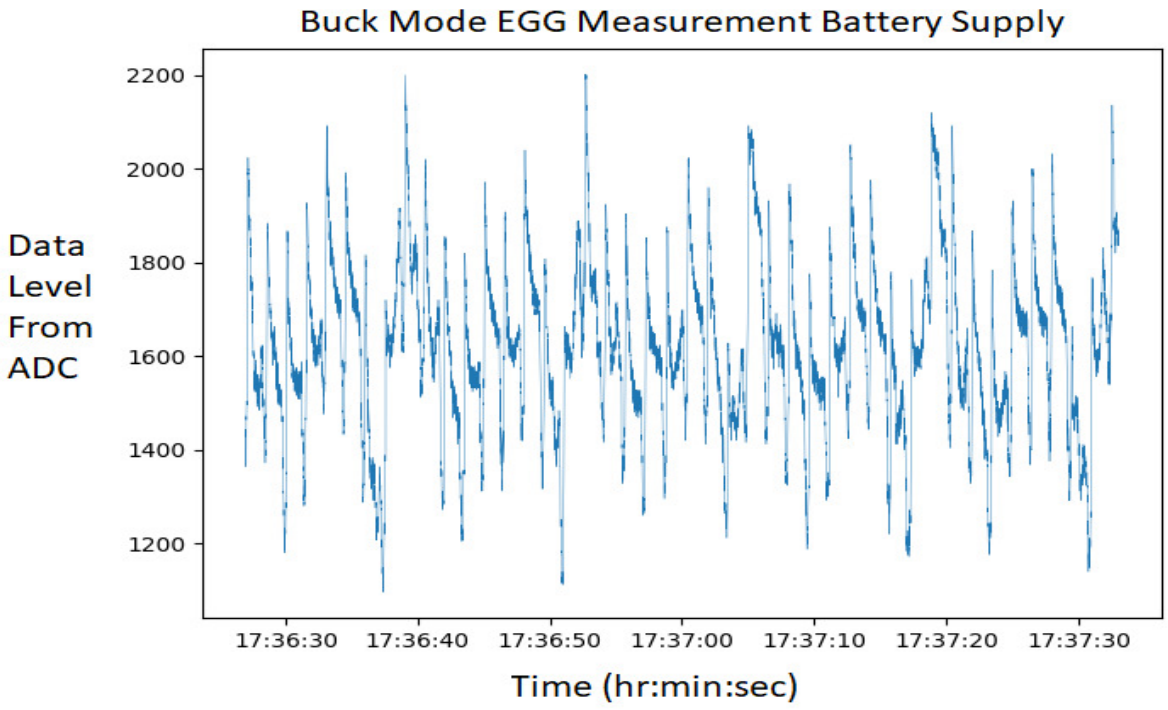


Figure 4.38. Plot of EGG in a rat with 12-bit ADC on Bionode operating from buck mode NIBB powered by a 3V rechargeable lithium battery.

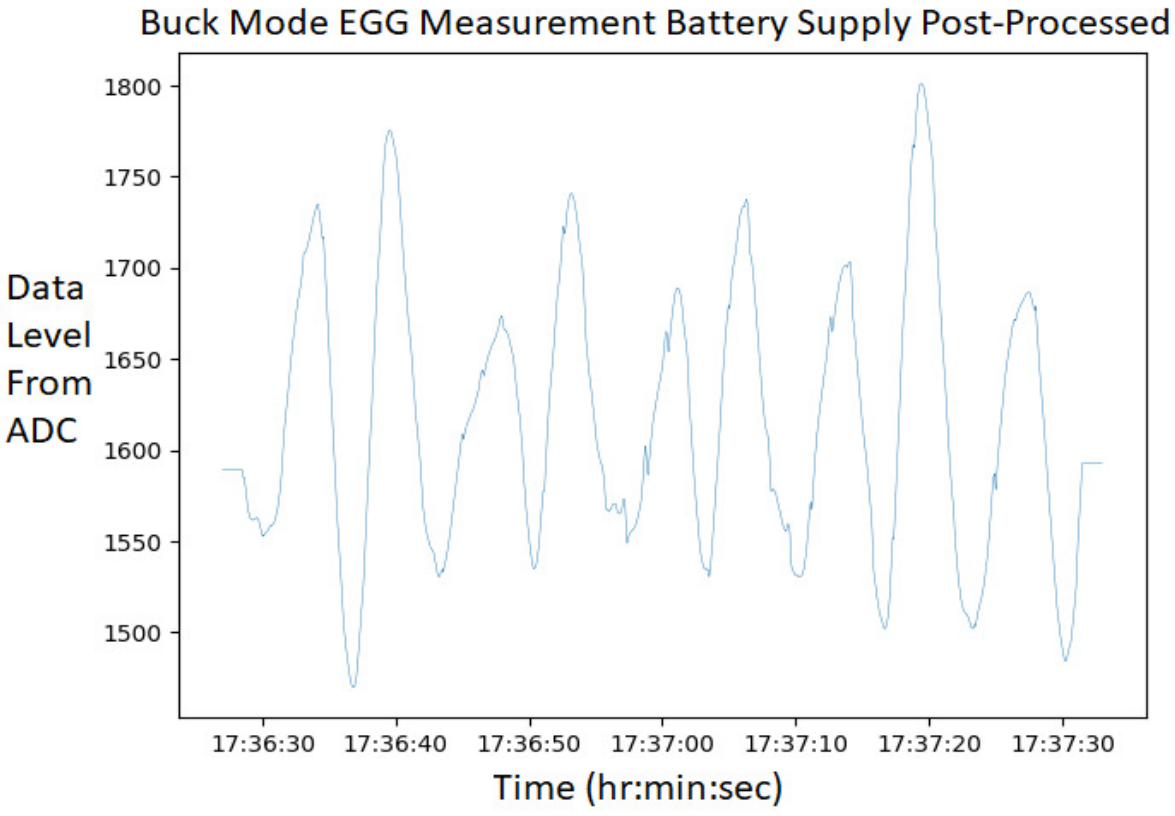


Figure 4.39. Three second moving window average filter of EGG from data in Fig 4.38.

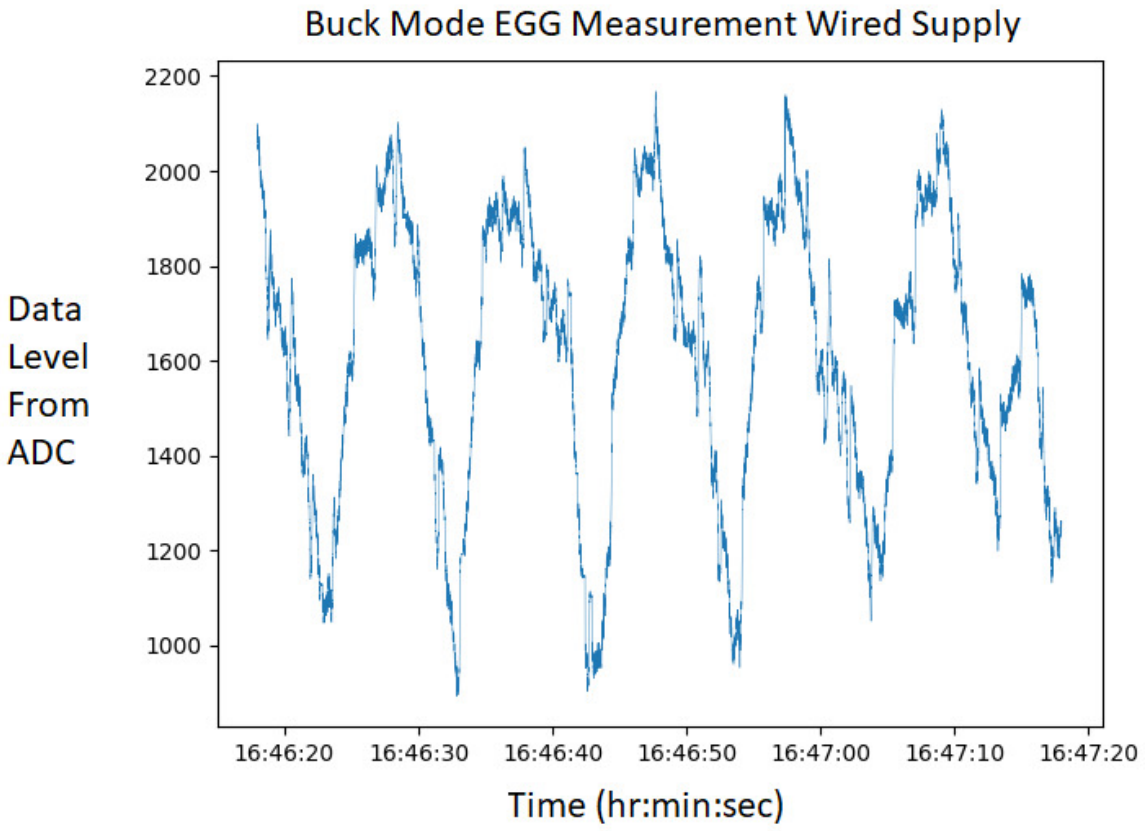


Figure 4.40. Plot of EGG in a rat with 12-bit ADC on Bionode operating from buck mode NIBB powered by wired wall supply power.

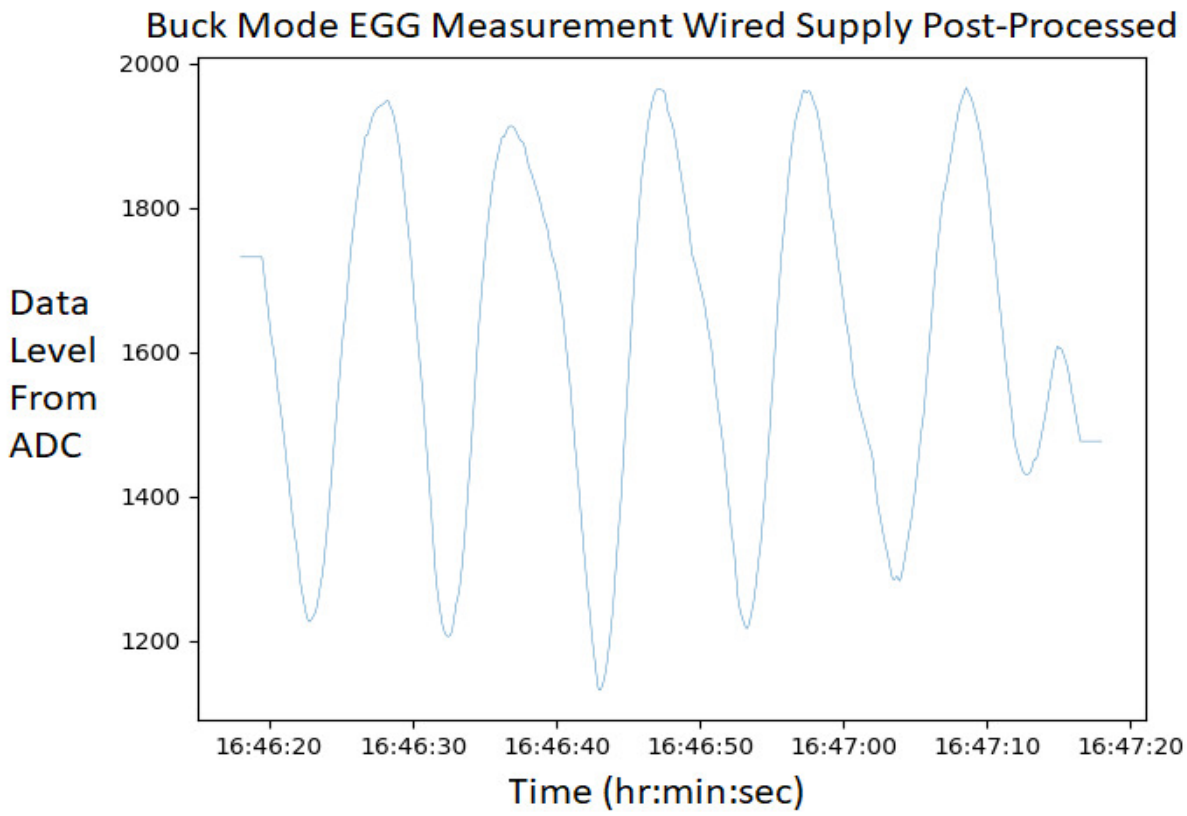


Figure 4.41. Three second moving window average filter of EGG from data in Fig 4.40.

The higher frequency peaks of noise in these four prior plots are all biological or environmental noise as this extraneous signal was found while measuring with a National Instruments Data Acquisition off-the-shelf unit as well. As a result, it can be surmised that the noise is power supply independent. Noting the width of the signal itself in-between the peaks, the noise contribution from the NIBB is very consistently minimal across all four measurements. In conclusion, an electrogastrogram signal of less than 0.6mV can be measured reliably with the NIBB and the regular stomach activity can be properly characterized and quantified utilizing this NIBB presented.

5. CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

This work presents a method to improve the PTE of wireless powering in a resonant cavity by an average of 10.38% over conventional static impedance matching and show 99.58% on-time in an implanted rat for a device capable requiring up to 75mW. In addition, this work demonstrates a two receive coil solution able to increase the average PTE by 5% across a standard operating frequency range compared to a conventional single coil solution, while decreasing the turn on transient power required to start the device up. Finally, this work develops the methodology behind, and steps involved in creating a NIBB converter capable of delivering a maximum conversion efficiency of 87% at the usual operating case of an implantable discrete system like the Bionode, while providing the most flexible input voltage range, output voltage ranges, and continuous output currents compared to the literature of similar converters in similar applications. The converter's novel ZCD allows the NIBB to operative effectively in both PWM and PFM modes for both buck and boost conversion, enabling the converter to work in design spaces that other chips do not. This work is the only NIBB converter capable of outputting voltages high enough for discrete implantable devices while providing output currents for both low power, slower bio-signal acquisition, and high power stimulation with fast signal acquisition.

5.2 Future work

This cavity-based system has the drawbacks of only having the Cp value being dynamic, while in the future the system should also be able to dynamically change Cs. The cavity-based system also suffers from requiring higher power to turn on the device than required for continuous operation. A system capable of dynamically tuning the cavity by changing the probe length real time to account for impedance mismatch when the driving frequency changes would further improve the PTE of the presented system. In addition, the lower frequency improved turn-on system sacrifices peak PTE, which could be improved upon by potentially having a way of switching the two half-coils out at steady state to switch in a full size coil to not sacrifice any PTE. Eventually, an elegant solution involving combining the lower frequency, low power startup solution with two receive coils, and the higher frequency cavity-based dynamic

impedance matching system will result in high PTE without sacrificing turn-on power requirements. Finally, various improvements to the two-coil receive system could be implemented, including the following: optimization of the size ratio between the two coils to provide for better peak PTE, multi-tonal power signal transmission to the two receive coils (now tuned to different frequencies) to decrease electrical coupling, and developing a way to combine the two coils into one or occupying the same space without sacrificing peak PTE or turn on transient power. For the improvement of the NIBBC, additional resolution in voltage binning and pulse widths would allow for more accurate PWM operation at higher loads and better efficiencies. Furthermore, clever methods of gating off circuits when not in use during converter operation would reduce the power consumption of the controller on the NIBBC. Additionally, various circuit elements and methodologies could be implemented to reduce the effects of the inductor forcing current through body diode connections and potentially wasting stored power or damaging sensitive transistors on the chip. Finally, a more elegant clock distribution system could be implemented to provide a higher speed clock for use by a SAR ADC for better voltage resolution, while maintaining low power consumption during the voltage measurement process.

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VITA

Chris Quinkert has attended Purdue University since 2010 and received his B.S. in biomedical engineering in 2015. After spending a year and a half away from school from 2012 to 2013 working for Biomet, Inc, Chris learned how much he enjoyed product development and research in an industrial setting. Upon returning to Purdue, he joined the Center for Implantable Devices in 2013, where he decided to focus on electronics for the remainder of his elective coursework as an undergraduate. Upon finishing undergraduate studies, Chris remained in the Center for Implantable Devices as a graduate student to pursue his PhD in the Electrical and Computer Engineering department at Purdue University. During his time as a researcher, Chris was a teaching assistant for BME 301 Bioelectricity for three semesters, winning the Magoon Award for teaching excellence one of the semesters.

Now that he has graduated, Chris has decided to return to industry to continue to work in product development and research aimed at integrated circuits in a variety of fields, while relocating to the Boston, Massachusetts metropolitan area. He eventually plans to teach physics or engineering courses at the high school level later in his career.